

Reducing the Size and Complexity of an Isolated Synchronous Gate Driver

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IDEA IN BRIEF

The traditional approach to designing an isolated dc-to-dc converter with synchronous rectification involves using optocouplers or pulse transformers for isolation and mating them together with a gate driver IC. This article will illustrate the limitations of optocouplers and pulse transformers and present a more integrated approach, which has higher performance and a much smaller solution size and cost.

PULSE TRANSFORMERS

Using pulse transformers to couple low level signals, isolate them, and drive power switches offers advantages, but it comes with some limitations. An advantage of the pulse transformer in gate drive applications is the pulse transformer can be used to step up from 3 V or 5 V logic level to the higher level voltages of 15 V or more needed to drive the gate of a MOSFET. Unfortunately, to drive high current synchronous rectifier circuits, a separate high current gate

driver IC may be needed. Another point to consider and a major disadvantage of pulse transformers in gate driver applications is that they do not handle well signals that have more than 50% duty cycle. This is due to the fact that transformers can deliver only ac signals because the core flux must be reset each half cycle in order to maintain a volt-second balance.

Another disadvantage of the pulse transformer is the efficiency loss. When a pulse transformer is used to drive the gate of a MOSFET, the transformer must be driven in a positive level, followed by a negative level, to maintain a volt-second balance. The energy used to drive to a negative level is not used to drive the gate of the MOSFET; the gate is charged only by the positive voltage level. For the typical application where the transformer is driven by a positive dc voltage, a dc blocking capacitor is connected to the transformer input, and the transformer is driven by a positive voltage that is $\frac{1}{2}$ the applied voltage. That means the negative voltage is also $\frac{1}{2}$ the applied voltage, so that the efficiency of the pulse transformer is reduced to 50%. If a gate driver is added to the transformer output, the overall efficiency of the transformer and gate driver will no longer be 50%, but there will still be at least 50% efficiency loss in the pulse transformer alone.

It has been shown here that the pulse transformer in a gate driver application has disadvantages of duty cycle limitation, poor efficiency, and larger solution size, which make it undesirable for high power, high density synchronous rectification applications.

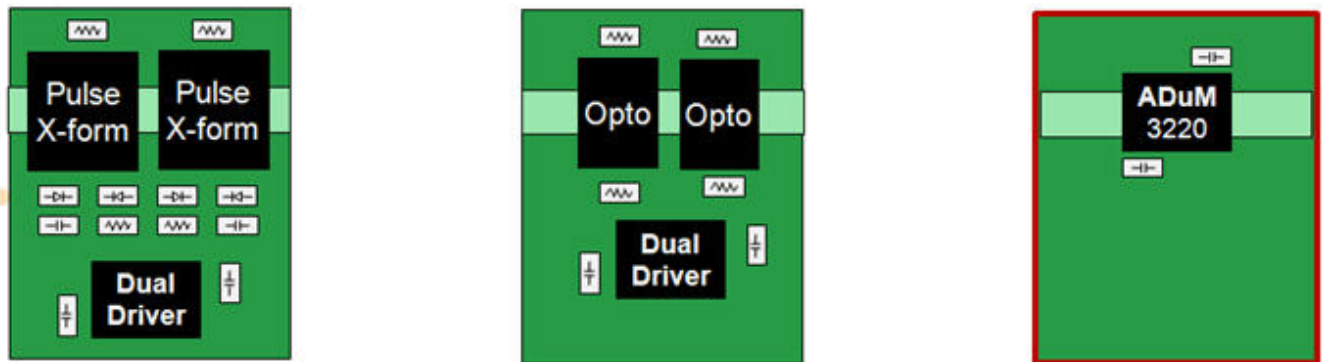


Figure 1. Pulse Transformer, Optocoupler, and ADuM3220 Gate Driver Solutions

OPTOCOUPERS

Using optocouplers as a gate driver for synchronous rectification can offer some advantages over pulse transformers, but the use of the optocoupler comes with its own challenges. The optocoupler does not need to maintain a volt-second balance like the pulse transformer does, so it does not have the same limitation on duty cycle that the pulse transformer has. But the speed of response of the optocoupler is limited due to the capacitance (60 pF typical) of the primary side light emitting diode (LED), and driving the diode to speeds up to 1 MHz can be limited by its propagation delay (100 ns max) and slow rise and fall time (30 ns max).

A main issue with using optocouplers for synchronous rectifier applications is the amount of variation in the timing between channels. Optocouplers are built as discrete devices in a plastic package, and the variation from channel to channel cannot be controlled like they can be in an integrated semiconductor process, so the channel to channel matching can be large (40 ns max). In a synchronous rectification circuit, the timing between channels needs to be tightly controlled to help reduce the dead time between one channel turning off and another channel turning on, otherwise the efficiency will suffer as the switching losses increase.

Designing with optocouplers can be challenging, due to the nature of the current transfer ratio (CTR), which defines the ratio of the amount of current that is seen at the output transistor over the amount of current that is needed to drive the LED. The CTR is affected by temperature and aging, so the designer needs to estimate the change in CTR over the lifetime and temperature range of the optocoupler. To maintain the CTR over operation conditions, the current needed to drive the LED can be more than 10 mA, which may be too much power dissipation for high efficiency designs.

In addition, resistors are needed to bias the LED and phototransistors, and a gate driver IC is needed to deliver the high peak currents that the optocoupler can't provide for high power synchronous rectifier supplies. For compact state of the art power supplies, the optocoupler solution size will become prohibitively large.

ADUM3220 4 A GATE DRIVER

The [ADuM3220](#) was designed to be used as a 4A gate driver in an isolated system for synchronous dc-to-dc conversion. Traditional solutions have used two isolators and a dual gate driver. As shown in Figure 1, a dual gate driver IC can be mated with two pulse transformers or two optocoupler channels to provide a fairly large solution size. Given that power supply applications require large amounts of power in a small area, the [ADuM3220](#), as shown in Figure 1, is a solution that is more than 50% smaller and is a more integrated solution for lower cost.

Synchronous rectification uses N-channel MOSFETs instead of diodes to reduce the conduction losses and increase efficiency in power supplies where many amperes of current are to be delivered. Implementing the synchronous dc-to-dc converter architecture requires synchronizing the switching of the secondary MOSFET switches with the primary MOSFET switches. Figure 2 illustrates the [ADuM3220](#) application circuit for an isolated synchronous dc-to-dc converter with unregulated output voltage.

The dc-to-dc controller sends the PWM drive signals to the primary and secondary switches. Primary switches Q1 and Q2 are turned on in a push-pull action with a break before make timing to drive the two primary coils of the transformer T1, as shown in Figure 2 timing waveforms. The secondary coil of T1 needs to be switched in sync with the primary coils by switching on Q3 when turning on Q1, and turning on Q4 when turning on Q2. Note, Q3' and Q4' PWM waveforms, if they were shown, would be advanced in time by the known propagation delay of the [ADuM3220](#) so that Q3 and Q4 appear in time as they should. The [ADuM3220](#) has a typical propagation delay of only 45 ns, which includes the digital isolator delay and the gate driver delay. By integrating the gate driver with the isolator, the specification of propagation delay is more precise, an advantage over discrete pulse transformer and optocoupler solutions.

When PWM switching is performed at a high frequency, the PWM control signals need very tight control. For example, when the PWM frequency is at the [ADuM3220](#) maximum switching frequency of 1 MHz and a duty cycle of 50% is used, the pulse width is at 500 ns. At this small pulse width, the matching between channels of the [ADuM3220](#) needs to be very good to deliver precise switching. The [ADuM3220](#) has a typical channel-to-channel matching of 1 ns, with a maximum of 5 ns over temperature. This precise matching between channels of the [ADuM3220](#) helps to prevent cross

conduction and protects the MOSFETs from damage, as well as allowing the minimum amount of dead time, to reduce switching losses and improve efficiency.

Next, we will consider applications where an isolated feedback is used to tightly control the output voltage, and the duty cycle will not be a fixed 50% but will vary to control the output voltage. In these applications, during the time that the primary switches are both off, it may be desired to allow the Q3 and Q4 switches to be on at the same time to prevent the body diodes of Q3 and Q4 from conducting, which would be less efficient. The application circuit for the ADuM3221 that is shown in Figure 3 is a 4 A gate driver that

is just like the ADuM3220 but does not have the nonoverlap control logic, allowing Q3 and Q4 to be on at the same time. Unlike the ADuM3220, the timing diagram for the ADuM3221 gate driver with regulated output shown in Figure 3 can allow the switches Q3 and Q4 to conduct when Q1 and Q2 are both off.

In summary, for isolated synchronous dc-to-dc applications, the ADuM3220/ADuM3221 have been shown to reduce the solution size by more than 50%, reduce the complexity of design through integration, and provide much improved timing performance over pulse transformer and optocoupler solutions.

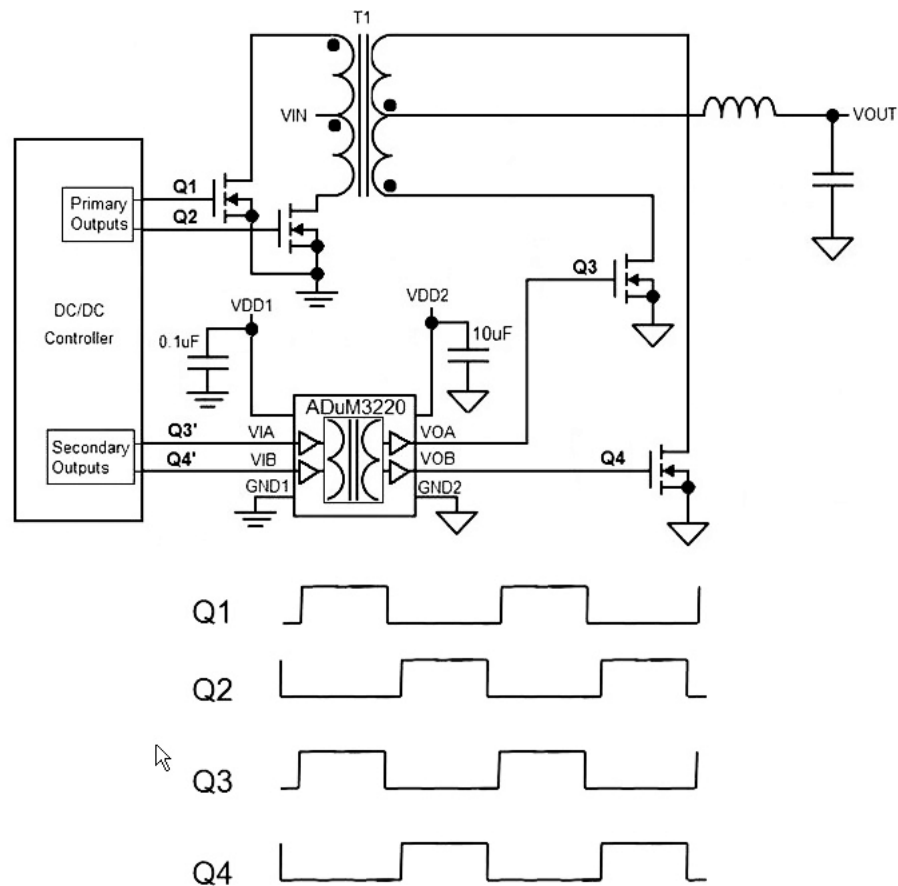


Figure 2. ADuM3220 Application Schematic and Timing Waveforms

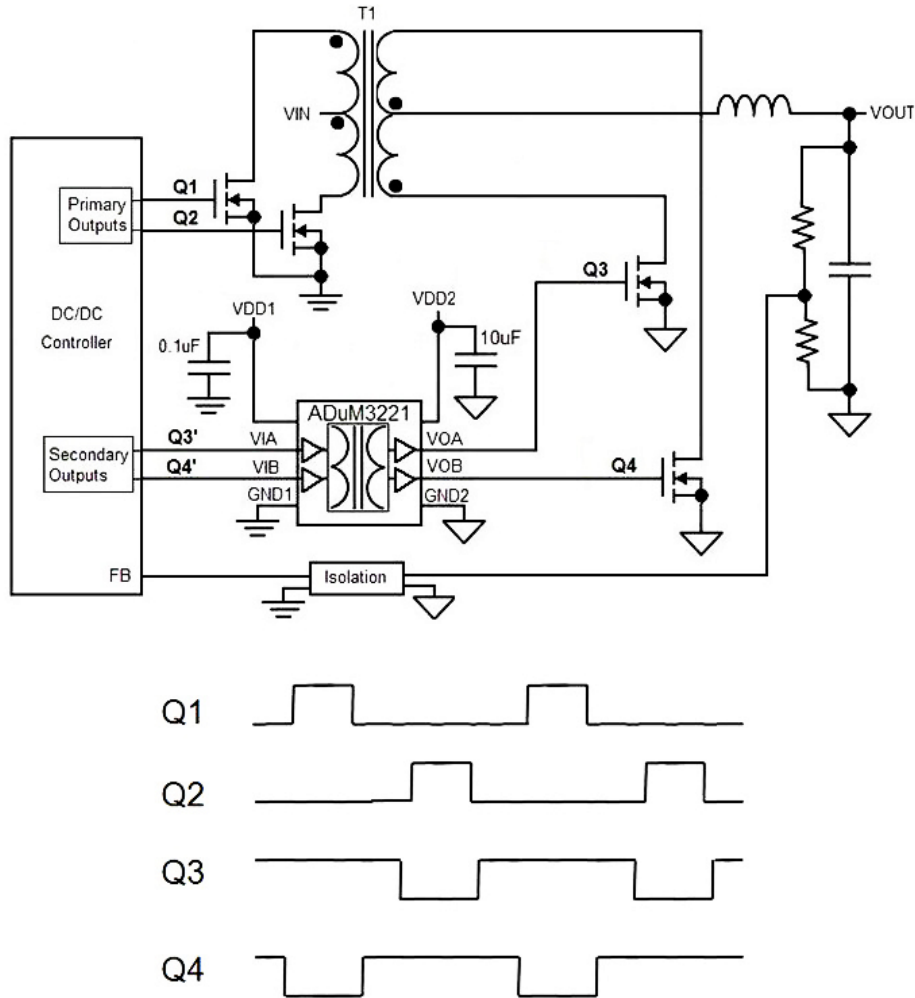


Figure 3. ADuM3221 Application Schematic with Regulated Output and Timing Waveforms

RESOURCES

For more information on digital isolators, visit www.analog.com/iCoupler.

Products Mentioned in This Article

| Product | Description |
|----------|---------------------------------------|
| ADuM3220 | Isolated 4 A Dual-Channel Gate Driver |
| ADuM3221 | Isolated 4 A Dual-Channel Gate Driver |

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