

Discussion Between CareFusion and Analog Devices: Optimizing Performance and Lowering Power in an EEG Amplifier

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IDEA IN BRIEF

For over twenty years, CareFusion Nicolet has been pioneering developments in the area of EEG diagnostic systems. EEG (electroencephalography) monitoring is used in neurological analysis for sleep studies, brain mapping, and ICU patient monitoring of cerebral activity. As continued breakthroughs in brain studies and EEG diagnostics are made, the EEG monitoring devices are expected to operate in new environments outside traditional clinical settings. These new environments lead to new design challenges—this paper addresses some of those challenges.

Harry (Op Amp Applications Engineer at Analog Devices):

Recently, Bill, Matt, and I had some discussions on the trade-offs in the first stage in an EEG front end design—the instrumentation amplifier (in-amp). We thought it might be useful to share it with other designers.

Matt (In-Amp Applications Engineer at Analog Devices):

That's right. Bill looked at a lot of in-amps in our portfolio but ended up creating his own instrumentation amplifier

instead. This is quite unusual in performance-driven applications, so we wanted to cover the thought process. Bill, can you give an overview of your design goals?

Bill Kolasa (Principal Electrical Engineer at CareFusion):

We currently have an in-amp based design that is performing well for us, but we wanted to optimize certain performance characteristics while decreasing power consumption.

As many designers of EEG and ECG devices know, the difference in half cell potential in the electrodes can create large dc offsets that the measurement system must be able to tolerate. Our current system was designed to handle up to ± 900 mV offsets. In order to deal with different electrode types and environmental conditions seen in the field, we wanted to increase the tolerance up to ± 1300 mV.

At the same time, we were contemplating a battery-powered design, so we needed to dramatically lower the power consumption of all the components, including the instrumentation amplifier. Our current power consumption is 28 mW per channel, and we wanted to lower this to 10 mW or less. We had the option to allow increased noise to get this power reduction.

Matt: We see this trade-off a lot with our ECG and EEG customers. For ECG and EEG front-end design, there is an inherent trade-off between noise, offset handling capability, and power consumption.

Most instrumentation amplifiers have a large noise component due to the noise of the subtractor stage. In high gain applications, it doesn't matter much since this noise stays constant at the output regardless of the gain. So when the noise is referred to the input, it is quite small.

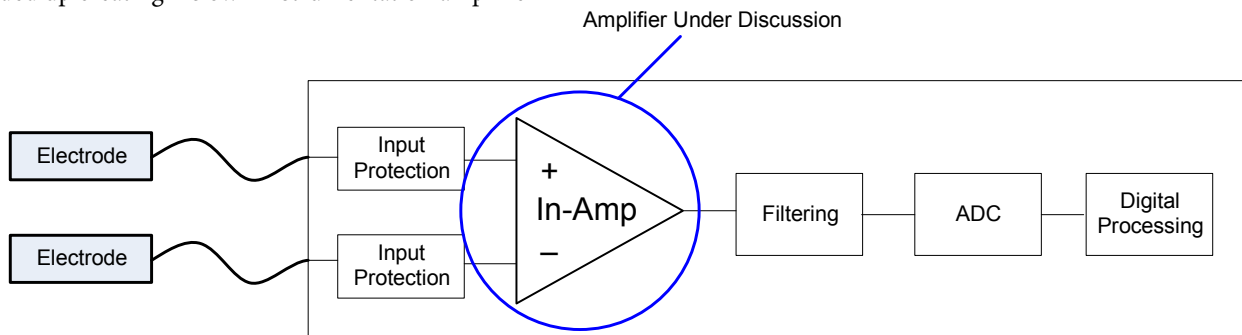


Figure 1. EEG Signal Chain

Unfortunately, in EEG and ECG applications, the gain is limited by the large offset from the electrodes. If you want to use a large gain to get good noise performance, the offset forces you to use large supplies to handle the large offsets.

Bill: This is indeed what we did on our previous design using an [AD8221](#) in-amp. The output noise is $75 \text{ nV}/\sqrt{\text{Hz}}$ and the input noise is $8 \text{ nV}/\sqrt{\text{Hz}}$. In order to reduce the contribution of the large output noise when referred to the inputs, we set the [AD8221](#) to a gain of 14.8 (see Equation 1 and Equation 2 for our noise calculation detail). The gain also increases our common-mode rejection by 23 dB, as the common-mode gain is unity (see Equation 3). But then in order to handle a 900 mV electrode offset with this gain, we have to use supply rails of $\pm 15.5 \text{ V}$ dc (see Equation 4). With 64 of these channels comprising our EEG amplifier, the power consumption becomes too high for battery powered applications.

I keep waiting for Analog Devices to come out with an in-amp with low output noise. When's that happening?

Matt: The output noise of an in amp is primarily driven by six resistors. (R1 through R6 in Figure 2) We could reduce these resistor values, but this has several drawbacks: 1) The in-amp amplifiers now have to drive more current into these resistors. To maintain good linearity in these higher drive conditions, we have to build beefier amplifiers, which consume more current. It's a double whammy for you: you have to supply the additional current through the small value resistors, as well more current for beefier amplifiers.

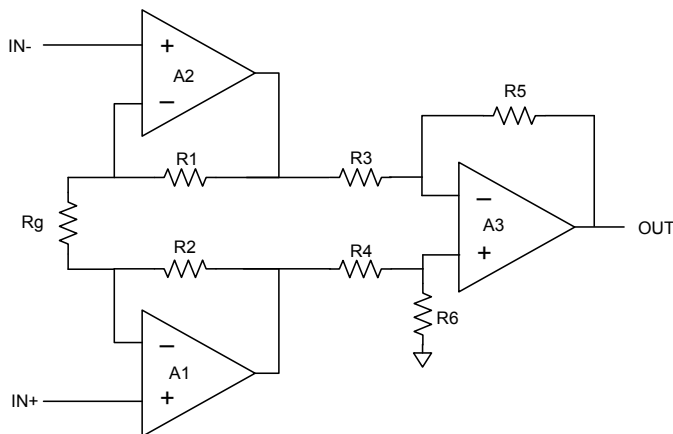


Figure 2. Textbook Instrumentation Amplifier Configuration

Bill: Doesn't sound like good news for my power consumption issues.

Matt: Your R_g gain setting resistor would get smaller. This is a good thing for noise, but not so good if you expect a large differential overvoltage condition. It makes the input of your

amplifier less robust to large differential voltages in high gain. We can add circuitry to combat this, but this circuitry adds to the input noise.

Bill: That one is probably not a problem for us because of the protection circuitry we already have on our electrode inputs.

Matt: As the resistors in your subtractor circuit get smaller, the input impedance of our reference pin also gets smaller. This means that if you want to drive this pin with a buffer—something that's pretty common in your type of application—the drive amplifier has to have very low output impedance over the frequency range of interest. Otherwise, you reduce the CMRR vs. frequency of your system. Lower output impedance vs. frequency requires a higher power driver amplifier.

Bill: Yes, in our new design we are driving that pin so this would be a concern. We spent some time finding a buffer that gave similar CMRR performance as just grounding the pin.

Going back to the original problem, we had the [AD8221](#) with a supply current of 0.9 mA running on $\pm 15.5 \text{ V}$. We wanted to lower the power consumption by reducing the current draw of the in-amp and reducing the supply rails. We started looking for lower power devices that could still meet our other performance requirements.

One in-amp that we looked at was the [AD8235/AD8236](#). It has very low power and small size, but was too noisy and with a 5 V max rail couldn't meet our dc offset spec.

Matt: These are CMOS based in-amps consuming $40 \mu\text{A}$. Very popular for ECG monitoring applications, where power trumps performance, but not good enough for diagnostic EEGs, which CareFusion does.

Bill: Another part we considered was the [AD627](#). It also consumes very little power and allows for wide supply rails. We had tested the noise in the past, so knew it had good performance for the power consumption. However, it comes in an SOIC package, which is big these days and didn't work well for reducing board size.

Matt: Yeah, maybe we ought to do something about that...

Bill: Then you've got a wide range of parts with $300 \mu\text{A}$ to $500 \mu\text{A}$ supply currents and wide supply ranges—for example, the [AD8226](#) and [AD8227](#). However all of these parts have at least 20 nA of input bias current, which was exceeding the specified requirement of less than 5 nA for this design.

Matt: On parts like the [AD8226](#) and [AD8227](#), we wanted the ability to measure all the way down to the negative supply. We used a simpler input stage to do this and had to sacrifice some input bias current to get there. On the [AD8221](#), we use both input bias current compensation and superbeta transistors to get bias current down to typically a few hundred pA. This made a lot of our customers happy, but the trade-off is that we give up some headroom on the input.

Bill, what drives your bias current spec? I thought EEG electrodes had around 10 k Ω of source impedance? For the [AD8226](#), with a max input bias current of 27 nA, this is 270 μ V, which is nothing compared to the big offsets from the electrodes. Can you tell us what drives your bias current specification?

Bill: The 5 nA spec does come from some of our amplifiers that must deal with much higher electrode impedances. However, this amplifier has an EEG display bandwidth requirement down to dc. We were concerned with minimizing baseline drifting effects due to changing electrode impedances.

After we found that none of the in-amps from ADI or your competitors met all our requirements, we decided to look at building our own. We knew that it was important to have matched resistors in the subtractor stage for >100 dB CMRR. We had experimented with matched resistor networks in the past but found these to be expensive. We also never quite seemed to get the expected CMRR performance, probably due to circuit board parasitic capacitances. We found the [AD8278](#) difference amplifier had the performance and power consumption we were looking for.

Harry: The four resistor difference amp is more complicated than it first appears. With a perfect op amp, the CMRR is limited by the matching of the resistors. (R3-R6 in Figure 2). An approximation (see Reference 1) for a difference amp is:

$$CMRR \cong \frac{A_d + 1}{4t}$$

Where A_d is the gain of the difference amplifier and t is the tolerance of the resistors. So for a gain of one and 1% resistors, CMRR = 50 V/V, or about 34 dB, and for 0.1% resistors, CMRR = 500 V/V, or about 54 dB.

Bill: I came across a similar explanation in one of your handbooks. (See Reference 2)

Harry: The above formula applies for low frequencies. CMRR may be degraded even further at higher frequencies. For example, if the difference in the input capacitance on the

two op amp inputs is 400 to 500 femtofarads, due to PC board layout or internal die layout, and the resistors are 10 k Ω , the ac CMRR at 10 kHz is degraded by 6 dB to 7 dB. If there is a 20 kHz (or higher) switching regulator in the system, this can be important.

Even with perfect resistors and balanced capacitances, the CMRR is ultimately limited by the op amp.

I see two major performance categories for difference amps. First, typical high side current sensing applications require 3% to 5% accuracy at the high end of the current range. A low cost op amp with reasonable offset and some 1% resistors can get you there. Keep in mind that some of the low cost op amps can have a CMRR of less than 50 dB. This is often overlooked. Second, the more precision applications, usually as the second stage of a discrete instrumentation amplifier, in the 0.1% to 1% range, with CMRR greater than 70 dB to 80 dB. This can be done with a good op amp, four matched resistors with low TC, preferably ratio matched TC, and a careful pc board layout. Considering the total cost and board space, the monolithic difference op amps look quite attractive. I can see why Bill chose the [AD8278](#); we did the hard work for him.

Bill: Analog Devices offered a family of difference amplifiers with gains of 1/2, 1, or 2. We compared the [AD8271](#) and [AD8278](#), choosing the [AD8278](#) for lower power consumption. We configured it for a gain of 1/2. This allowed us to increase the gain of the input buffers, lower the supply rails (we settled on ± 7.5 V dc), and meet our noise and dc offset tolerance specifications. We believed that moving as much gain as possible to the input buffers provided the lowest noise. (See Equation 5 through Equation 11 for noise, CMRR, and offset tolerance of the new design.)

Matt: The [AD8278](#) can either be configured as a gain of 1/2 or gain of 2. Typically, we think we need to put an amplifier in the highest gain possible to get the best noise performance. However, because the [AD8278](#) is the second stage in this design, the noise performance of the design is actually helped by putting it in a lower gain. This allowed Bill to apply more gain in the first stage. A cardinal rule of low noise design is to have as much gain in the first stage as possible—and it certainly was the case here.

Applying more gain up front also helps the in-amp's CMRR. As we can calculate from our previous discussion of resistor tolerance vs. CMRR, changing the difference amplifier gain from 1/2 to 2 should give us an extra 6 dB of CMRR. This

also matches the [AD8278](#) data sheet. However, if instead we use the extra $4\times$ gain up front, it will increase the differential gain by $4\times$ while keeping the common-mode gain the same. In other words, by gaining up front we get an extra 12 dB of CMRR vs. the 6 dB we could get by applying the gain in the difference amplifier. Note that this trick only worked if the op amps in the first stage have good CMRR—so it's important to use high quality op amps.

Using $G = 1/2$ for the difference amplifier stage is one way Bill optimized his discrete design vs. our integrated in-amps. Typically for our integrated In Amps, we must keep the difference amplifier at $G = 1$ or higher, since lower diff amp gains limit the in-amp's ability to handle wide common mode voltage swings.

Bill: After extensive searching, we chose the [AD8622](#) for our input buffer op amps. This op amp had all the specifications we were looking for: small package size, low power, low input bias current, low 0.1–10 Hz noise, and wide supply rails. One other characteristic that we felt was important was unity gain stability. Although our buffers were run at a gain of 10, in the in-amp configuration the common-mode signal sees a gain of 1, thus causing potential stability issues. (See Reference 3)

Harry: For the front end op amps, there are dozens of choices, perhaps hundreds, so getting the exact offset voltage, bias current, supply current, bias current, etc. allows one to optimize the design. When we design an instrumentation amplifier, we have to make some broad trade-offs, so for the last ten percent of performance, it's worth the hard work. The [AD8622](#) is a recent addition to our precision amplifier line and is a really nice combination of voltage noise, low $1/f$ corner, supply current, gain bandwidth, offset voltage, offset voltage drift, etc.

I want to compliment Bill on the way he partitioned the system. Sometimes we see three sections of a quad being used for instrumentation amplifiers. This is an easy trap to fall into. The requirements of the first stage are totally different than the difference amplifier stage in terms of V_{os} , TCV_{os} , gain, bandwidth, CMRR, etc. Again, for the last ten percent of performance, a dual for the first stage and a single for the second stage make a lot of sense. To get low voltage noise in an op amp, we burn a lot of current that you don't need in the second stage. If the second stage drives a heavy load, you need much more drive than the first stage op amps. Another drawback of a quad: you may get thermal

feedback from the output op amp to the first stage op amps. A more detailed discussion is in Reference 4 and Reference 5.

Bill: Our first choice would have been to use an integrated in-amp for board space reasons. However, having precision difference amplifiers available really allowed us to fine tune our instrumentation amplifier without the need for expensive and board-space-consuming resistor networks. We were able to significantly reduce our power consumption while still maintaining our important performance characteristics, such as noise, CMRR, and dc input tolerance.

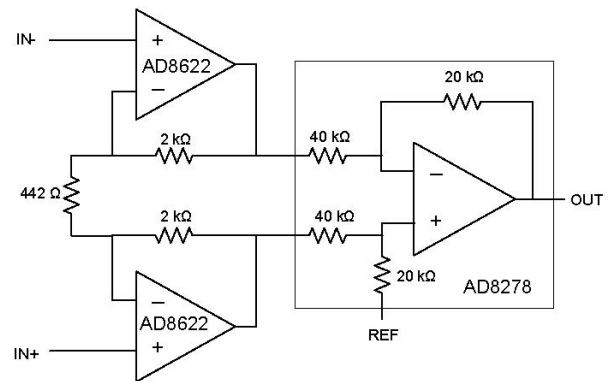


Figure 3. Simplified CareFusion In-Amp

Harry: Thanks, Bill. Matt and I have enjoyed working with you on a state-of-the-art design.

Biographies:

Bill Kolasa has been with the NeuroCare Division of CareFusion for the past seven years involved in the design of medical instrumentation. He received his BSEE from Michigan Technological University. He would like to recognize Bill Lutz and Dan Lombardi also at CareFusion for their contributions to this article.

Harry Holt is a staff applications engineer at Analog Devices (San Jose, CA) in the precision amplifier group where he has worked for four years, following 27 years in both field and factory applications at National Semiconductor for a variety of products, including data converters, op amps, references, audio codecs, and FPGAs. He has a BSEE degree from San Jose State University and is a life member of Tau Beta Pi and an elected Senior Member of the IEEE.

Matt Duff has worked as an applications engineer at Analog Devices covering instrumentation amplifiers and various other products for the past five years. Prior to joining Analog Devices, Matt worked for National Instruments in both design and project management positions on

instrumentation and automotive products. He received his BSEE from Texas A&M and MSEE from Georgia Tech.

APPENDIX: BILL'S EQUATIONS

Calculation of expected p-p noise of AD8221 in a 0.1 Hz to 100 Hz BW showing effect of gain (neglecting current noise because electrode impedance is low).

$$noise = \sqrt{\left(e_{n_in}\right)^2 + \left(\frac{e_{n_out}}{Gain}\right)^2} \times \sqrt{Bandwidth} \times CrestFactor = \tag{1}$$

$$\sqrt{8^2 + \left(\frac{75}{14.9}\right)^2} \times \sqrt{100} \times 4 = 0.379 \mu V \text{ p-p}$$

Adding in 1/f noise (using Gain = 10 from data sheet):

$$\sqrt{0.379^2 + 0.5^2} = 0.73 \mu V \text{ p-p} \tag{2}$$

Calculation of expected min CMRR of AD8221BR showing increase due to gain.

(Using gain = 1 number from data sheet):

$$CMRR = 90 \text{ dB} + 20 \times \log(gain) = \tag{3}$$

$$90 \text{ dB} + 20 \times \log(14.8) = 113 \text{ dB}$$

Calculation of electrode offset tolerance AD8221:

$$\left(\frac{Supply \text{ Rail} - Output \text{ Swing}}{gain}\right) = \left(\frac{15.5 \text{ V} - 1.6 \text{ V}}{14.8}\right) \tag{4}$$

$$= 940 \text{ mV}$$

For new in-amp design (neglecting current noise because of low impedances).

Noise of AD8622 buffers :

$$e_n \times \sqrt{Bandwidth} \times CrestFactor = \tag{5}$$

$$11 \text{ nV} \times \sqrt{100} \times 4 = 0.44 \mu V \text{ p-p}$$

Add in 1/f noise =

$$\sqrt{0.44^2 + 0.2^2} = 0.48 \mu V \text{ p-p} \tag{6}$$

Noise of 1/2 Rg in parallel with Rf:

$$\sqrt{4kT \times \frac{1}{2} Rg} \left| Rf \times \sqrt{Bandwidth} \times CrestFactor \right. = \tag{7}$$

$$\sqrt{4 \times 1.38^{-23} \times 300 \times 2k} \times \sqrt{100} \times 4 = 0.23 \mu V \text{ p-p}$$

Noise from AD8278:

$$\frac{Output \text{ Noise}}{Gain} \times \sqrt{Bandwidth} \times CrestFactor = \tag{8}$$

$$\frac{50 \text{ nV}}{5} \times \sqrt{100} \times 4 = 0.4 \mu V \text{ p-p}$$

Add in 1/f:

$$\sqrt{0.4^2 + \left(\frac{1.4}{5}\right)^2} = 0.49 \mu V \text{ p-p} \tag{9}$$

Summing all sources:

$$en = \sqrt{0.48^2 + 0.48^2 + 0.23^2 + 0.23^2 + 0.49^2} = \tag{10}$$

$$0.9 \mu V \text{ p-p}$$

Expected min CMRR of new in-amp design:

$$CMRR \text{ of AD8278B} + 20 \times \log(Buffer \text{ stage gain}) = \tag{11}$$

$$80 + 20 \times \log(10) = 100 \text{ dB}$$

Electrode offset tolerance of new design (dc source tied to one input, second input at ground).

$$\frac{Supply \text{ rail} - output \text{ swing}}{gain(gain \text{ in this case is } 1 + (Rf / Rg))} = \frac{7.5 \text{ V} - 0.25 \text{ V}}{5.5} \tag{12}$$

$$= 1.32 \text{ V}$$

REFERENCES

1. Pallás-Areny, Ramón and Webster, John G. "Common Mode Rejection Ratio in Differential Amplifiers" *IEEE Transactions On Instrumentation and Measurement*, Vol. 40, No 4, August 1991, pp 669-676.
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