

## Mitigation Strategies for ECG Design Challenges

by Bill Crone, Systems Engineer, Healthcare  
Analog Devices, Inc.  
william.crone@analog.com

### IDEA IN BRIEF

Engineers can use Analog Devices solutions to manage the major challenges of electrocardiogram subsystem design, including safety, common-/differential-mode interference, input dynamic range requirements, device reliability and protection, noise reduction, and EMC/RFI considerations.

An electrocardiogram (ECG) is a common medical recording that must be readable and accurate in many harsh environments. Whether in a hospital, ambulance, aircraft, marine vehicle, clinic or home, sources of interference are pervasive. A new wave of highly portable ECG technology has made it possible to measure the heart's electrical activity in a larger variety of settings. As ECG subsystems make their way into more out-of-hospital applications, manufacturers face continued pressure to reduce system cost and development time while maintaining or increasing performance levels. The resulting demands on ECG design engineers are considerable: provide a safe and effective ECG subsystem that can withstand the challenges of the intended use environment.

This paper identifies what are typically considered the major challenges of ECG subsystem design and recommends various methodologies with which to mitigate them. The challenges that are discussed are safety, common-/differential-mode interference, input dynamic range requirements, device reliability and protection, noise reduction, and EMC/RFI considerations.

### CHALLENGE #1: MEETING THE HIGHEST LEVEL OF SAFETY TO ENSURE THAT THE ECG SUBSYSTEM IS SAFE AND EFFECTIVE

Safety is always the number one design concern of the ECG designer. Both the patient and the operator must be protected from power surges or overvoltage coming from the ac mains and from any current path through the ECG electrodes that could exceed the recommended limit of 10  $\mu$ A rms. The ultimate goal is to ensure patient and operator safety from dangerous voltages or currents that can occur should there be a fault condition in the ECG subsystem itself or in some other medical device attached to the patient or operator.

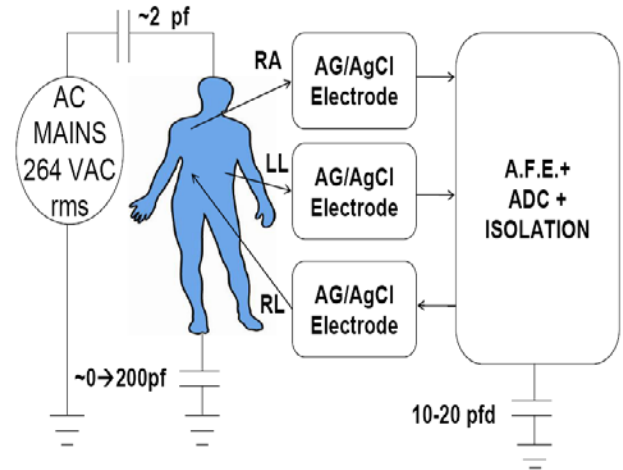


Figure 1. Overview of AC Mains Coupling

Prior to the start of the ECG design, engineers must determine the clinical applications, as well as where the device is to be used and stored. Engineers must evaluate all possible misuse of the device and potential external connections that could result in currents applied to the patient. Safety for the operator and patient can be maintained when the applied current (sink or source) is limited to less than 10  $\mu$ A rms, even during single-fault failures. The patient must be protected from accidental electric shock, and the ECG apparatus must be protected from extreme voltages generated by emergency use of a cardiac defibrillator.

ECG systems must meet federal regulations as well as international standards and individual country directives. In the U.S., the Food and Drug Administration (FDA) classifies medical products as Class I, Class II, or Class III. These classification categories impact product design and the approval process. For instance, a portable Holter monitor for diagnosing cardiac rhythms is considered a Class II device. In contrast, a cardiac monitor/defibrillator with an ECG subsystem is designated Class III.

What is the significance of a device classification? On its [Device Classification web page](#), the FDA states

The class to which your device is assigned determines, among other things, the type of premarketing submission/application required for FDA clearance to market. If your device is classified as Class I or II, and if it is not exempt, a 510k will be required for marketing. All devices classified as exempt are subject to the limitations on exemptions. Limitations of device exemptions are covered under 21 CF xxx.9, where xxx refers to

Parts 862-892. For Class III devices, a premarket approval application (PMA) will be required unless your device is a preamendments device (on the market prior to the passage of the medical device amendments in 1976, or substantially equivalent to such a device) and PMA's have not been called for. In that case, a 510k will be the route to market.

Device classification depends on the *intended use* of the device and also upon *indications for use*.

Each medical device has a classification/rating of Type B, Type BF, or Type CF. These classifications affect how the device is designed and used. Different leakage current limits and safety testing apply per IEC60601-1. The IEC standard also defines an applied part as the part of the medical device that comes into physical contact with the patient in order for the device to carry out its intended function.

Most medical devices are classified as Type BF or Type CF. Type BF devices have conductive contact with the patient but not the heart. Type CF is reserved for devices and parts directly contacting the heart. ECG designers are advised to approach every ECG application as a type CF Class III system. The designer has no control over how the ECG subsystem is applied to a patient and, if the patient has an access point to the heart, the device must be classified as Class III due to the potential direct connection of an applied part to the heart. All cardiac-monitor/defibrillators are classified as Class III devices.

The human heart is most sensitive to electric current in the 50 Hz to 60 Hz range. As little as 34  $\mu\text{A}$  rms at 50 Hz/60 Hz traveling through the heart has been shown to compromise the heart and cause a life threatening event. Given various procedures that can occur while an ECG system is attached to a patient, including indwelling catheters for pacemakers/AICDs (automatic implantable cardioverter-defibrillators), the present limit of current permitted at 50 Hz/60 Hz is set to 10  $\mu\text{A}$  rms. In ECG design, a limit of 10  $\mu\text{A}$  rms with no fault conditions is the design parameter. The American College of Cardiologists (ACC) also recommends that the limit of 10  $\mu\text{A}$  rms extend to single-fault failures as well.

The designer must examine all scenarios where current between electrodes, or from electrodes to the circuitry or to earth ground, could create single-fault scenarios where the current can exceed 10  $\mu\text{A}$  rms. This source/sink current is a function of frequency, but the 10  $\mu\text{A}$  rms limit ranges in frequency from dc to 1 kHz. From 1 kHz to 100 kHz, the current level linearly increases with frequency: from 10  $\mu\text{A}$  rms at 1 kHz to 1 mA rms at 100 kHz. Above 100 kHz, the current is limited to 1 mA rms.

Solutions come in the form of resistance placed in the signal path and/or current-limiting devices. Analog Devices manufactures components that can assist in addressing the needs for patient safety.

## CHALLENGE #2: COMMON-MODE AND DIFFERENTIAL-MODE ENVIRONMENTAL SIGNALS AND RADIO FREQUENCY INTERFERENCE (RFI)

An ECG measures the voltage generated by the heart's electrical system. At the same time, the ECG subsystem must reject environmental electrical signals, such as ac mains, security systems, and radio frequency interference (RFI) to amplify and display the ECG signal. Common-mode voltage does not provide any useful information about the heart and may actually impede measurement accuracy. The ECG system must be able to reject common-mode interference, while responding to the signal of interest—the differential-mode ECG voltage. The ability to reject large common-mode signals in the presence of a small differential signal relates to the common-mode rejection (CMR) of the system.

Common-mode rejection can be measured many ways. In this paper, two methods are discussed. The first is to tie all of the ECG electrodes together and drive the electrodes relative to the ECG analog front-end voltage reference. For single-supply operation, the reference may take the form of a virtual voltage driven from the RLD electrode that places the level at half the distance between the unipolar supply and isolated ground. The common-mode rejection in this case is the resultant output level relative to the input level ( $20 \times \log(V_{\text{OUT}}/V_{\text{IN}})$ ).  $V_{\text{IN}}$  is the common-mode voltage applied, and  $V_{\text{OUT}}$  is the voltage that appears at the particular lead of interest. To see the common-mode rejection of Lead II, the voltage is applied to all electrode inputs relative to the right leg drive terminal (if this represents the midpoint of the ADC or the RLD reference) and the device is programmed to display Lead II. The voltage appearing at Lead II is  $V_{\text{OUT}}$ , the applied voltage,  $V_{\text{IN}}$ .

Another method of measuring common-mode rejection is to tie all the electrodes together and drive them relative to earth ground. Again, the definition of the common-mode rejection is  $20 \times \log(V_{\text{OUT}}/V_{\text{IN}})$ , where  $V_{\text{IN}}$  is the common-mode drive signal and  $V_{\text{OUT}}$  is the signal seen on the particular lead of interest.

This part of the subsystem design and components selection requires modeling the human subject, the environmental coupling of the ac mains and incoming RFI into and through the patient, and the subsequent impact on the performance of the ECG amplifier as it attempts to reject the incoming common-mode signals. Incoming RFI is removed by

multiple methods, including differential- and common-mode filtering, environmental shielding, and algorithms.

Figure 2 shows a traditional high frequency, low pass filter network, which is prone to differences in C1A, C1B, and C2 values. Figure 3 shows an integrated X2Y capacitor implementation that offers higher performance due to the nature of the X2Y construction and design.

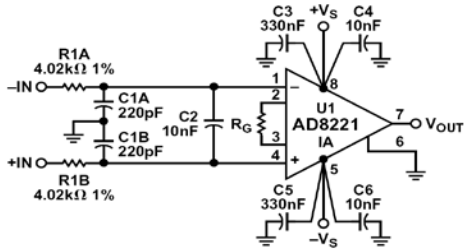


Figure 2. Traditional High Frequency, Low Pass Filter Network

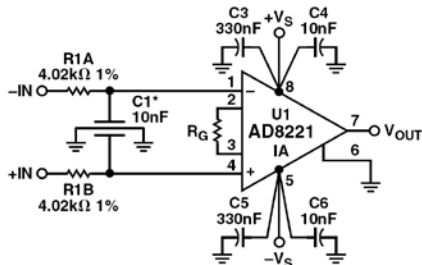


Figure 3. Integrated X2Y Capacitor Implementation

Dedicated ECG designers should model the potential environment to determine not only the ac power mains common-mode signal but also other common-mode and differential-mode signals that may arrive at the ECG electrodes when attached to the patient. Most ECG cables have protection resistors embedded in them for defibrillator protection. This impact, along with differences in cable capacitance and front-end EMI filtering, can cause the common-mode signal to become unbalanced, resulting in phase shifts and common-mode to differential-mode conversion.

A technique called right leg drive (RLD) can reduce the CMR requirements of multiple-lead configurations. The common-mode voltage seen by the amplifier relative to earth ground can be reduced even in a 2-lead system by using a form of RLD that drives current back into the electrodes 180 degrees out of phase with the incoming CM signal. Because the electrode impedances are not matched, the current injection must account for this, adjusting the relative current/phase to minimize the effective common-mode signal.

In short, the amplifier input must have large enough common-mode (CM) and differential-mode (DM) signal ranges to accommodate arriving CM/DM signals from ac

mains as well as other external inference sources, such as equipment powering on/off and radio-frequency transmission sources. The common-mode rejection must be as good with zero offset on the inputs of the differential amplifier as it is with a differential input voltage as high as  $\pm 1$  V.

Other solutions to power-line interference include DSP techniques such as subtraction algorithms. To assist the designer, Analog Devices offers components that reduce the impact of large incoming common-mode signals: CMR INA amplifiers, PLLs, converters, and synchronous modulators/demodulators for lock-in amplifier systems. The ADAS1000 ECG AFE addresses common-mode rejection by featuring high differential input impedance and RLD.

### CHALLENGE #3: ANALOG FRONT-END COMMON-MODE AND DIFFERENTIAL-MODE DYNAMIC RANGE

ECG devices must be able to react quickly when a patient is shocked with a defibrillator. A physician may need to see the patient's electrocardiogram within one second after defibrillation. If this pulse is applied through certain types of metal such as stainless steel, the post defibrillation polarization of the material may be as high as 0.7 volts after 1 second. This differential offset, along with potential electromagnetic (EMI) and/or radio frequency interference (RFI), can exceed the input range of the ECG front end. In short, the amplifier saturates and the ECG signal cannot be seen.

The ECG design must be able to maintain its common-mode and differential input performance even during this type of transient input. Because most ECG systems are now sold worldwide, designers must also address the worst-case ac mains input range. Case in point: in west Australia, the ac mains voltage can be as high as 264 VAC rms with 6 kV spikes. The common-mode rejection in this environment must be a factor of approximately two times higher than in the United States where the ac mains voltage is 120 VAC rms. This fact, along with the electrode offsets and polarization that can occur, require high differential and common-mode input dynamic range. Because the ECG voltage is between 100  $\mu$ V and 3 mV peak to peak, the dynamic range input capability of the analog front end prior to digitization of the signal of interest is significant. Modern day ECG front ends have dynamic input ranges that are approximately  $\pm 1$  V for Ag/Ag-Cl electrode applications to  $\pm 1.5$  V or higher for defibrillator pad applications.

Some systems operate off a single supply voltage with a generated virtual ground that applies a midpoint voltage to the patient (no current) halfway between the supply ground and the supply rail. This is typically part of the RLD

circuitry. The electrode amplifiers are relative to this mid-supply rail to insure no injection of ac or dc current. The required input dynamic range of  $\pm 1$  V relative to this virtual ground is what is required for rapid response post defibrillation and anticipated worst-case environmental conditions.

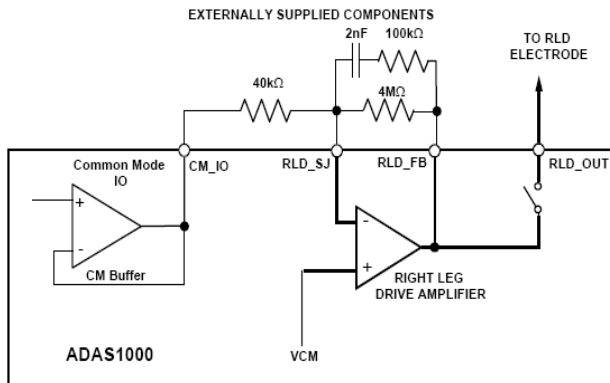


Figure 4. Right Leg Drive—Possible External Component Configuration

The noise performance, linearity, CMRR, and differential gain of the ECG front end must not be compromised by the particular input operating point of the amplifier. The input impedance for each electrode must be greater than 1 G $\Omega$  with capacitance of approximately 10 pF or lower, preferably matched between electrodes. The Analog Devices discrete [AD8220](#) and [AD8226](#) instrumentation amplifiers feature wide dynamic range to enable circuit architectures that meet CMR needs. The [ADAS1000](#) ECG AFE meets the requirements for low noise, high dynamic range, CMR, and linearity. Blackfin® processors also meet the back-end needs of ECG and automated external defibrillator (AED) devices.

#### CHALLENGE #4: ESD, ENVIRONMENTAL, AND DEFIBRILLATOR PROTECTION

Design engineers must protect the ECG front end from damage. ECG systems require built-in protection circuitry to handle electrostatic discharges, defibrillator discharges, or other overvoltage and overcurrent events. The human hand model, which mimics the electrostatic discharge of a human touching a device, uses a 1500  $\Omega$  resistor and a series 100 pF capacitor that limit the current that can be discharged through the human hand. The charged voltage dictates the amount of instantaneous voltage that can be applied and how the current is limited. Voltages in excess of 18 kV are possible. Some standards set the voltage to as low as 8 kV.

Most ECG systems have input protection for a defibrillator pulse and ESD using the human hand model. Defibrillator protection circuitry has multiple requirements: to maintain the CMR of the preamplifier at performance frequencies; to

shunt less than 5% of the delivery defibrillator energy away from the defibrillation electrodes/pads; and to fully protect the preamplifier circuitry in such a way that the ECG can quickly be seen on either a display or strip chart after a defibrillator pulse. In the emergency room (ER), a one-second delay (or shorter) is the desired response time.

The defibrillator protection circuitry can take two forms. In one case, where the ECG cable is part of a cardiac monitor defibrillator, a series of resistors (energy rated high voltage resistors) typically limits the current into an ECG front end. In addition, some protection circuits have argon or xenon bulbs on the ECG side of the protection resistors to limit the preamp side voltage to less than 100 V. Additionally, voltage and current limiting devices ensure that the ECG system is not damaged. The designer should consult with the manufacturer of the particular instrumentation amplifier (INA) or any active/passive circuitry that can potentially see this high voltage and current. Silicon-controlled rectifiers (SCRs) provide some of the overvoltage protection. Energy-rated series resistors provide current protection. Current limiters can also be considered.

Most active devices cannot tolerate the voltages associated with ESD testing without some form of protection. It is a requirement to check with the active device manufacturer to determine the degree of protection required and the suggested mitigation. The designer is encouraged to review the FDA guidance relating to energy-rated resistors for defibrillator protection. Some devices have been recalled due to improper measurement/rating of these resistors (the FDA recently announced it is reviewing regulations for AEDs amid reports of device malfunctions).

To aid the designer with discrete defibrillator protection circuitry, Analog Devices components have been tested to tolerate high levels of ESD and input current and voltage. The ADAS1000 ECG AFE includes large ESD protection structures on its package pins and has been evaluated for tolerance of maximum source/sink current.

#### CHALLENGE #5: ELECTRICAL NOISE

ECG signals may be corrupted by multiple sources including power-line interference, contact noise between the electrode and the skin, motion artifacts, muscle contraction, and electromagnetic interference from other electronic devices. Any number of sources can cause the ECG baseline to drift or appear electrically noisy. What's important to clinicians is that the ECG signal be clear and that all the electrical noise combined be as small as possible so as to not confound the ECG diagnosis. For diagnostic ECG applications, the noise floor should be designed to meet 10  $\mu$ V peak to peak.

ECG designers must take steps to filter out or discard all these noise sources. The requirements for the equivalent input noise floor varies by application. For monitor quality systems, such as a heart rate monitor (HRM), it is usually adequate to specify an equivalent noise value of approximately 25  $\mu\text{V}$  peak to peak over a 0.5 Hz to 40 Hz bandwidth. In some cases, to make the system extremely low power, a higher noise floor may be allowed. Even in monitor-quality applications, the noise floor is required to be lower than 25  $\mu\text{V}$  peak to peak, hence the need to fully understand the clinical environment and algorithm requirements.

When designing a fully diagnostic 12-lead ECG system (10 electrodes), the bandwidth can be as low as 0.05 Hz to 150 Hz or as broad as 0.05 Hz to 2000 Hz. Pacer detection requirements increase the bandwidth further to at least 100 kHz.

In Holter monitors, for example, evaluation of the ST segment of the ECG waveform is used to determine STEMI (ST segment elevation myocardial infarction); a bandwidth of 0.05 Hz to 40 Hz can be selected to help reduce the overall noise floor, even at the expense of evaluating higher frequency components beyond 40 Hz. In other monitors, the bandwidth can be 0.05 Hz to 150 Hz or even 250 Hz depending on the patient and the intent of the evaluation.

Other noise considerations include cable movement, which can create low-frequency noise unless properly constructed, and burst noise, also known as shot noise or telegraph noise. This type of noise prevents physicians from seeing important information at various portions of the cardiac cycle, including the ST segment.

To manage the problem of noise, Analog Devices uses various circuit techniques to remove the  $1/f$  characteristic of a typical input amplifier while still maintaining low Gaussian noise and excellent device linearity. The Analog Devices CMOS process lends itself to very low levels of telegraph noise.

### **CHALLENGES #6: ELECTROMAGNETIC COMPATIBILITY (ECM) AND RADIO FREQUENCY INTERFERENCE (RFI)**

ECG subsystems must be protected from a variety of external/environmental emissions. For example, nearby medical equipment, as well as high frequency industrial or consumer electronics in the environment can generate sufficient E and H fields with complex modulation/transmission protocols. Interfering signals can reach the ECG front end through conducted or radiated emissions.

Thus, early in the process, designers must consider regulatory standards for radiated emissions, radiated susceptibility, immunity, conducted emissions, and conducted susceptibility/immunity. Due to atmospheric contamination throughout the world, it is becoming increasingly hard to find an open area test site (OATS) that allows full spectrum testing of a unit. In some countries, usage of a full height 10 meter test chamber is now acceptable in lieu of an OATS.

System designers must work with the EMC testing agency to determine the levels of essential performance, as defined in the third edition of IEC60601 and derivatives. Margin in reading must also be defined as having a 0.1 dB margin at a particular frequency while officially passing may not be acceptable because there may be as much as  $\pm 4.0$  dB variability in readings between OATS and 10 meter chambers at multiple sites. Typically, an 8.4 dB margin is considered conservative.

The designer should examine the PCB footprint for the ECG, the digital and/or analog I/O to the remaining portion of the system, the incoming power forms, the grounding, and the Faraday shield, which assists in preventing radiated emissions from being detected by protection diodes and other circuitry embedded in the ECG design. The ECG cable itself may have resonances at specific frequencies relating to the cable length. In the event that one of those resonances is energized by an internal clock or emitter inside the ECG design, compliance to Level B of the standard may be difficult. This is why common-mode/differential chokes and inline ferrite may be needed on various cables.

Prior to formal testing, a designer can consider sniffing the design with a series of E and H field probes and a spectrum analyzer to define radiating frequencies and harmonics. A series of prescans can determine the location of hot frequencies and how close they come to the limit. Consulting a source list, a designer can then determine if a Faraday shield is required over this emitter or whether slowing of signal edges may be adequate. Some cables inside the system may need ferrite or other filters to quell a resonance or high-level emitter.

Another solution is to seek out highly integrated, small packaged devices that are equipped to meet radiated emissions and incoming radiated susceptibility. The [ADAS1000](#) ECG AFE meets these needs and is the first device on the market to incorporate leads-off detection, respiration monitoring, and pacemaker pulse detection on a single chip.

## SUMMARY

Designing an ECG subsystem presents a plethora of safety and signal processing challenges characterized by small signals, a wide bandwidth requirement, interference from power lines and the environment, and the desire to have a very low noise ECG amplifier while maintaining very low power consumption. A wealth of information exists to assist the designer in developing safe, reliable, and high performance ECG designs. As a leader in signal-processing technologies, Analog Devices offers a wide range of solutions to help design engineers overcome all of the major ECG challenges.

## RESOURCES

For additional information, visit [www.analog.com/healthcare](http://www.analog.com/healthcare).

### Products Mentioned in This Article

Product	Description
<a href="#">AD8220</a>	JFET Input Instrumentation Amplifier with Rail-to-Rail Output in MSOP Package
<a href="#">AD8221</a>	Precision Instrumentation Amplifier
<a href="#">AD8226</a>	Wide Supply Range, Rail-to-Rail Output Instrumentation Amplifier
<a href="#">ADAS1000</a>	Low Power, 5-Electrode Electrocardiogram (ECG) Analog Front End (AFE)