Designing With Single-Ended Passive Mixers
For CDMA-Based Systems

By Eric J. Newman
Analog Devices, Inc.

Introduction

Code division multiple access (CDMA) and wideband CDMA (W-CDMA) are becoming widely deployed as communication standards for cellular telephony. The base station transceivers in these systems require high dynamic range components to provide immunity to blocking signals that would otherwise interfere with overall system performance. The mixers used in these designs need to offer high input linearity and moderately low noise in order to avoid excessive signal distortion and sensitivity degradation due to mixer spurious products. Traditionally, high-intercept balanced passive mixers have been utilized, as they provide sufficient instantaneous dynamic range and exceptional dynamic performance. Unfortunately, they require fairly strong local oscillator drive levels and need external balun/transformer structures for proper operation. Recently, single-ended gallium arsenide (GaAs) pseudomorphic high electron mobility transistor (pHEMT)-based mixers have become more popular as an alternative high-intercept mixer solution for common cellular transceiver designs. This article outlines the general design procedures for successful implementation of the ADL5350 single-ended passive mixer for common CDMA and W-CDMA frequency allocations.

Background

Single-ended mixers have been used for several years at microwave frequencies for both up and down conversions. Most single-ended mixers are implemented using fast-switching diodes that tend to require exotic processing techniques. Such mixers can provide reasonable performance out to millimeter-wave frequencies but can be cumbersome to use at cellular frequencies, because they are two terminal devices that require cautious design of bias networks and diplexer networks to properly couple the RF, LO, and IF signals. Traditionally, doubly balanced mixer topologies have been adopted for cellular applications due to their high intercepts and availability. Doubly balanced mixers use transformers to couple the signals to the mixing core and require less consideration in comparison to a single-diode mixer. However, the transformer networks can consume considerable board space and add significant cost to the design. Recently, field effect transistor (FET)-based single-ended mixers have demonstrated similar performance using lower local oscillator drive levels as compared to doubly balanced solutions. The single-ended mixer can use small low-cost LC filter solutions to realize the necessary external matching and signal coupling. Figure 1 depicts an idealized FET-based single-ended mixer.
The single-ended mixer relies on external filter structures to isolate RF and IF ports. Typically the RF filter is a bandpass or highpass network, while the IF filter is a band-reject or lowpass network. The LO drive modulates the impedance presented to the RF port, causing the RF voltage to be modulated by the applied LO signal at the RFIF common junction. If the LO drive is strong enough, or passed through a sufficiently high gain amplifier, the impedance variation will take on a square wave shape and cause the modulated signal to take on the zero crossings of the applied LO, resulting in sum and difference products. The modulated RF signal is then passed through a lowpass or band-reject filter that rejects the RF carrier frequency and allows the difference frequency to pass. In a similar manner, the signal flow could be reversed allowing the single-ended mixer to operate as an up-converter.

Analog Devices’ ADL5350 is a high-linearity single-ended mixer. The device is designed on a pHEMT switch process and incorporates an on-chip LO buffer amplifier to ease LO drive requirements. The part relies on off-chip filter networks to provide optimum port isolation. This allows the same mixer to be applied at low IF frequencies up to high RF frequencies with only a few changes to the external LC filter networks.

**Implementation methodology**

In order to optimize dynamic performance, it is necessary to properly tune four networks around the mixer. The LO interface needs to be designed to provide strong control of the nonlinear junction that provides the desired mixing behavior. This interface consists of an input matching network and a load/bias network around the internal LO buffer amplifier.
The RF and IF port networks must be designed to provide adequate port isolation as described previously. Figure 2 indicates the relevant external connections and component designators. The following discussion provides an outline on how to achieve optimum performance.

![Figure 2: Typical Implementation Schematic.](image)

**Step 1. Tune the LO buffer supply inductor for minimum supply current.**

In order to start this procedure it is necessary to make some initial assumptions about the optimum target choke inductor. It’s important to reactively load the drain at the desired LO frequency to ensure ample LO swing into the gate of the mixing FET, yet too large of an inductor selection may cause resonance issues that will roll off the LO buffer amplifier gain prematurely. *Table 1* can be used as a starting point. It is not necessary to terminate or populate the RF and IF port networks to complete this first step; the RF and IF ports can be left open while tuning the LO buffer networks.
Table 1: Recommended LO Bias Inductor.

<table>
<thead>
<tr>
<th>Desired LO frequency</th>
<th>Recommended LO bias inductor (L4)</th>
</tr>
</thead>
<tbody>
<tr>
<td>750 MHz</td>
<td>24 nH</td>
</tr>
<tr>
<td>1000 MHz</td>
<td>18 nH</td>
</tr>
<tr>
<td>1750 MHz</td>
<td>3.8 nH</td>
</tr>
<tr>
<td>2000 MHz</td>
<td>2.7 nH</td>
</tr>
</tbody>
</table>

In order to test the supply current consumption, simply power up the device and apply the desired LO signal through an adequately sized AC-coupling capacitor. Attempt to increase and decrease the LO frequency. If the current consumption increases as the LO frequency is decreased, try increasing the value of L4. If the current consumption decreases as the LO frequency is decreased, try decreasing the value of L4. After determining the optimum inductor value the current consumption should be minimized at the desired LO frequency.

**Step 2. Tune the LO port input network for optimum return loss.**

Typically a bandpass network is used to pass the LO signal to the gate input of the LO buffer. It is desirable to block high frequency harmonics of the LO from the mixer core. LO harmonics will cause higher RF frequency images to be down-converted to the desired IF frequency, and result in a degradation of sensitivity. If the intended LO source has poor harmonic distortion and questionable spectral purity, it may be desirable to employ a higher order bandpass filter network to clean up the LO signal. *Figure 2* illustrates a simple L-C bandpass filter used to pass the fundamental frequency of the LO source. Capacitor C3 is a simple DC block, while the series-inductor (L3) and gate-to-source capacitance of the buffer amplifier form a lowpass network. The native gate input of the LO buffer FET presents a rather high input impedance alone. The gate bias is generated internally using feedback, which can result in a positive return loss at the intended LO frequency. It may be desirable to add a shunt resistor to ground before the coupling capacitor C3 to present a lower loading impedance to the LO source if a better than –10 dB return loss is desired.

**Steps 3 and 4. Design the RF and IF filter networks.**

*Figure 2* depicts simple LC tank filter networks for the IF and RF port interfaces. The RF port LC network is designed to pass the RF input signal. The series LC tank has a resonant frequency at \(1/(2\pi\sqrt{LC})\). At resonance the series reactances cancel, presenting a series short to the RF signal. A parallel LC tank is used on the IF port to reject the RF and LO signals. At resonance, the parallel LC tank presents an open circuit.

It is necessary to accommodate for the board parasitics and finite Q and self-resonant frequencies of the LC components when designing the RF, IF, and LO filter networks. *Table 2* provides suggested values for initial prototyping.
Table 2: Suggested RF, IF, and LO filter networks for low-side LO injection.

<table>
<thead>
<tr>
<th>RF Frequency</th>
<th>L1</th>
<th>C1</th>
<th>L2</th>
<th>C2</th>
<th>L3</th>
<th>C3</th>
</tr>
</thead>
<tbody>
<tr>
<td>850 MHz</td>
<td>6.8 nH</td>
<td>4.7 pF</td>
<td>4.7 nH</td>
<td>5.6 pF</td>
<td>8.2 nH</td>
<td>100 pF</td>
</tr>
<tr>
<td>1950 MHz</td>
<td>1.7 nH</td>
<td>1.5 pF</td>
<td>1.7 nH</td>
<td>1.2 pF</td>
<td>3.5 nH</td>
<td>100 pF</td>
</tr>
</tbody>
</table>

Figure 3: RF and IF port interface transfer characteristics.

Figure 3 illustrates the RF and IF port transfer characteristics. The simulated data uses real S2P files to describe the inductor and capacitor parasitics, as well as the printed circuit board parasitics. The RF port S21 data is the response measured at the RFIF pins for a stimulus applied to the evaluation board RF port connection. Similarly, the IF port S21 data is the response measured at the evaluation board IF port connection for a stimulus applied to the RFIF pins. It is worth noting that the networks are symmetrical, and that the same response characteristics would apply in an up-converting application.

Performance Summary

Figure 4 depicts the dynamic performance as measured on the customer evaluation board for 800 MHz CDMA and 1950 MHz W-CDMA frequency allocations. In general, the
input third order intercept point (IIP3) remains better than or equal to 25 dBm with less than 7 dB NF over the entire base station receive bands.

Figure 4: Input linearity, loss, and single-sideband noise figure as measured for (a) 800MHz CDMA and (b) 1950 MHz W-CDMA base station receiver designs.
In terms of spurious free dynamic range (SFDR), this level of performance corresponds
to more than 80 dBC of instantaneous dynamic range over a 5-MHz-wide analysis
bandwidth. The high SFDR is needed to cope with the in-band blocking signals that may
otherwise generate intermodulation products and potentially desensitize the receiver,
resulting in unacceptable bit-error-rates. The high input 1-dB compression point (IP1dB)
helps to ensure that the mixer will not degrade the receiver's sensitivity in the presence of
a single-tone in-band interfering signal. The CDMA 2000 specifications call out inter-
mod and single-tone desense specifications, which the ADL5350 exceeds with ample
margin. The standard requires that the reference sensitivity be degraded by no more than
3 dB in the presence of intermodulation products resulting from two-tone interferers at
72 dBC above the desired signal level (–117 dBm). The ADL5350 could tolerate >30 dB
of pre-gain in a 800 MHz receiver design before intermodulation products generated in
the mixer would become problematic. The ADL5350 enables multi-carrier CDMA and
W-CDMA base station designs using a very small footprint at a low implementation cost.
The integrated LO amplifier allows for low LO input drive, typical only 4 dBm, which
permits the use of lower cost local oscillator synthesizer designs. The combination of
high input linearity, low loss, and lower LO drive in a compact package makes the
ADL5350 an excellent mixer solution for high performance transceiver designs.

About the author

Eric Newman is an applications systems engineer in the RF and Wireless
Products Group at Analog Devices Inc. In 1993, he received his Masters
of Science in Electrical Engineering, focusing on wireless
communications, from the University of Massachusetts at Lowell.