

The World Leader in High Performance Signal Processing Solutions



HDMI-enabled Designs Using the ADV7511

Analog Devices, Video Transmitters Product Line
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Presentation Overview

- ◆ **Introduction to the ADV7511**
 - Block Diagram and Features
 - **Support Documents**
- ◆ **Basic Setup and Configuration**
 - Example schematic and Quick-Start Setup Guide
 - Processor Interface and general control
 - ◆ I2C, Interrupts, Hot-plug Detect, DDC, EDID
 - Video Input
 - Audio Input
 - HDMI Output
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 - **Audio Return Channel (ARC)**
- ◆ **Advanced Usage**
 - Video Formatting
 - ◆ CSC, 422<->444 conversion, DE and Sync Generation
 - ◆ Pixel Repetition
 - HDCP

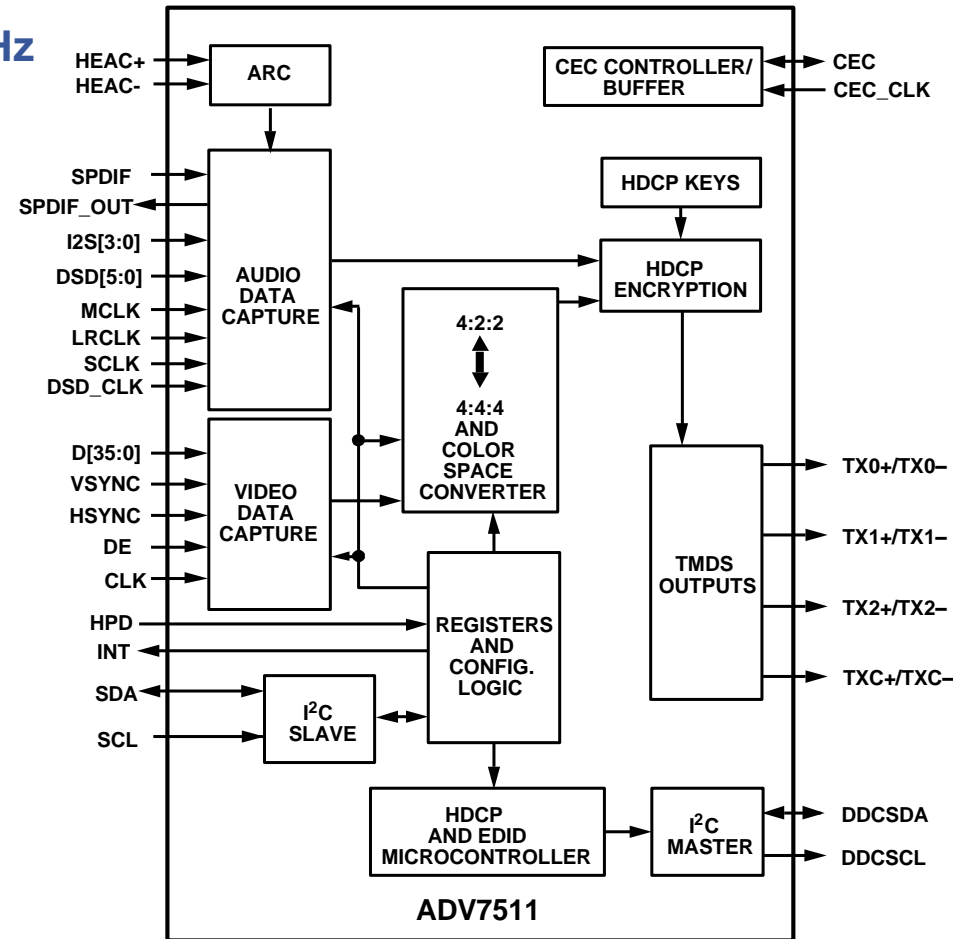


Introduction to the ADV7511

ADV7511 Features Overview



- Supports display resolutions at 25~225 MHz (up to 1080p deep color)
- Incorporates HDMI v1.3/1.4 features
 - ◆ Deep Color support (12-bit 4:4:4)
 - ◆ Supports extended colorimetry (e.g. x.v.Color™)
 - ◆ HBR audio formats
 - ◆ DST/DSD audio formats
 - ◆ Audio Return Channel
 - ◆ 3D Ready (720p50/60 & 1080p24/25/30)
- Integrated CEC support
 - ◆ Buffer CEC signals
 - ◆ Off-loads real-time monitoring from host μ P
- Low standby power
- Software driver → Easy implementation
- Optional on-chip HDCP support
- Programmable color space converter
- Flexible video inputs:
 - ◆ RGB 4:4:4, YCbCr 4:4:4, YCbCr 4:2:2
 - ◆ 36-bit input interface
- Integrated I2C Master for DDC bus
- +5V tolerant I/Os for HPD and I2C
- 1.8V & 3.3V supplies



Part	HDCP	Package	Temp
ADV7511KSTZ	Internal	16 mm ■ 0.5 mm ϕ LQFP 100-pin Pb-free	0 ~ 70 °C
ADV7511KSTZ-P	N/A		



ADV7511 Advantage Summary

- ◆ **Integrated CEC (Consumer Electronics Control) buffer/controller**
 - 3 command buffer
- ◆ **Low dynamic power and stand-by power**
- ◆ **Customer support services**
 - Field tested software driver for easy implementation
 - HDMI compliance test labs in Tokyo, Greensboro, Beijing and Taipei to perform pre-test for ADI customers
 - Multi-level support via Engineering Zone, market segment FAE's and product line Applications Engineers
 - Comprehensive, easy-to-use product user guides



ADV7511 Reference Documents

◆ ADI Documents

● Data Sheet

- ◆ Feature list
- ◆ Electrical specifications
- ◆ Pin diagrams and descriptions
- ◆ Package drawings

● Hardware User's Guide

- ◆ Detailed descriptions of hardware blocks
- ◆ External connection recommendations
- ◆ PCB layout guidelines

● Programming Guide

- ◆ Detailed register maps and descriptions
- ◆ Programming guidelines organized by system level function

● Software Driver User's Guide (DVP Transmitter Library Specification 1.9)

- ◆ Detailed description of C code functions that can be integrated into system SW
- ◆ Describes how functions are used to meet HDMI requirements

● User Guides, schematics, etc. available on ez.analog.com



ADV7511 Reference Documents

◆ Other Documents

- **HDMI Specification 1.4**

- ◆ Beyond the obvious, detailed information on CEC and HDMI compliance are included

- **EIA/CEA-861**

- ◆ Includes timing specifications for various video formats

- **HDCP 1.3**

- **IEC 60958**

- ◆ Audio standard

- **IEC 61937**

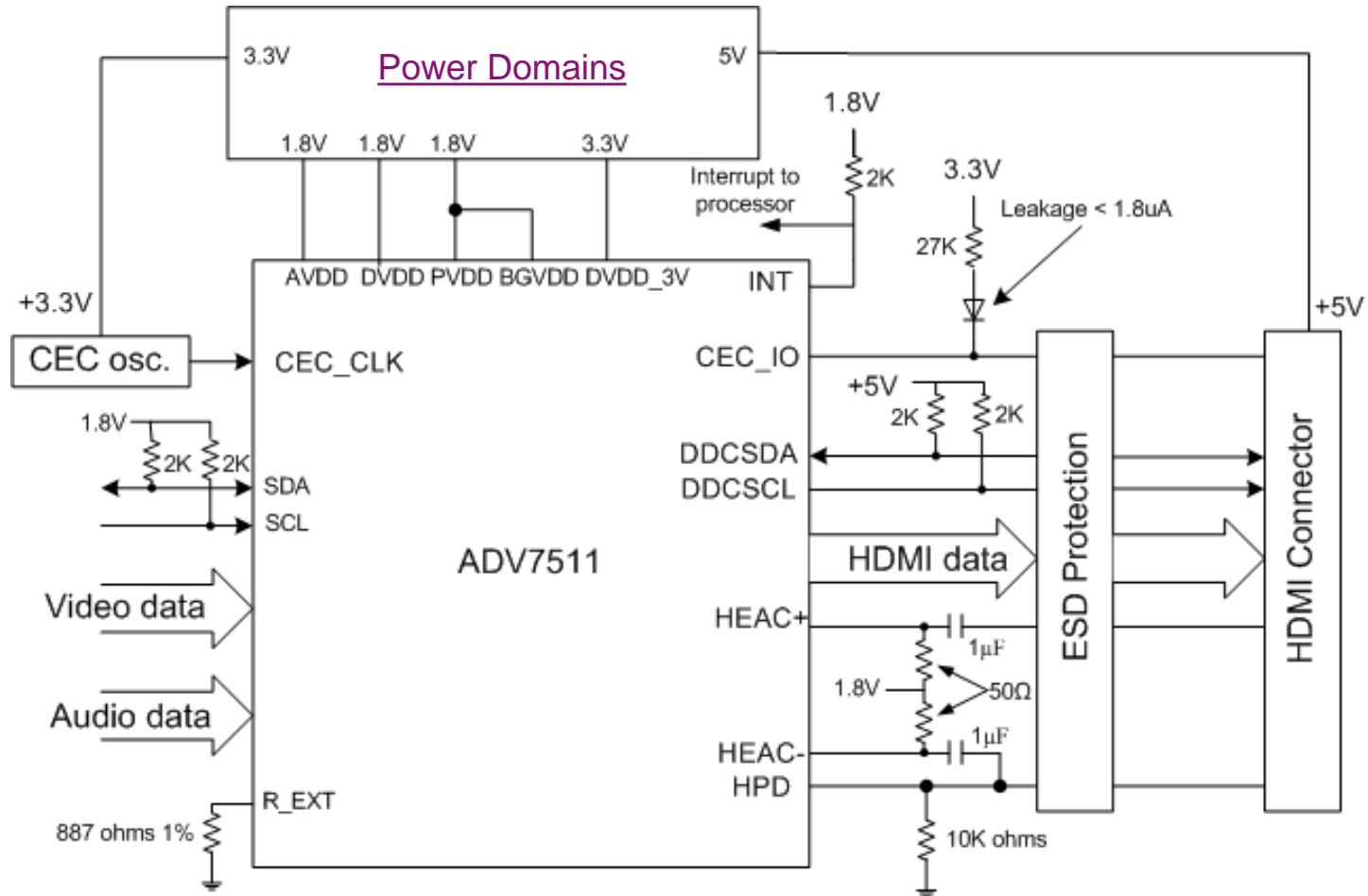
- ◆ Advanced audio standard

- **I2C-Bus Specification**



Basic Setup and Configuration

Example Schematic



[Go Back](#)

- See power domain slides for power details



Programming Quick-Start Guide

- ◆ **Power-up the Tx (HPD must be high)**
 - 0x41[6] - Power-down (Power-up = 0)
- ◆ **Fixed registers that must be set on power up**
 - 0x98 = 0x03
 - 0x9A[7:5] = 3'b111
 - 0x9C = 0x30
 - 0x9D[1:0] = 2'b01
 - 0xA2 = 0xA4
 - 0xA3 = 0xA4
 - 0xE0 = 0xD0
 - 0xF9 = 0x00
- ◆ **Set up the video input mode**
 - 0x15[3:0] –Input ID (default = 4:4:4)
 - 0x16[5:4] – 4:2:2 Width (default = 12 bit) – Used when using 4:2:2 Input ID
 - 0x16[3:2] – Video Input Style (default = 2) – Sets pin mapping along with Input ID and 4:2:2 width
 - 0x17[1] – Aspect ratio of video in (4x3 = 0, 16x9 = 1) – Used for video detection
 - 0x56[5:4] – Picture Aspect Ratio – aspect ratio of video being sent to Rx
 - ◆ part of AVI InfoFrame and required for HDMI compliance
 - ◆ should match the aspect ratio of the video input



Programming Quick-Start Guide

◆ Set up the video output mode

- 0x16[7] - Output Format (4:4:4 = 0)
- 0x18[7] - CSC Enable (YCbCr to RGB = 1)
- 0x18[6:5] - CSC Mode (YCbCr to RGB = 0b00)
- 0xAF[1] - Manual HDMI or DVI mode select (HDMI = 1)

◆ Audio setup

- 0x01 – 0x03 = N Value (0x001800 for 48kHz)
- 0x0A[6:4] – Audio Select (I2S = 3'b00, SPDIF = 3'b01, 3'b011 = HBR)
- 0x0B[7] - 0b1 – SPDIF Enable (Enable = 1)
- 0x0C[5:2] - I2S Enable (Enable = 4'b1111)
- 0x15[7:4] – I2S Sampling Frequency (48kHz = 0b0010)
- 0x0A[3:2] = Audio Mode
- 0x46 = 0xFF – Enables 8-channel DSD (leave at default if not implementing DSD audio)

◆ HDCP

- 0xAF[7] = 1 for enable HDCP
- 0x97[6] – BKSV Interrupt Flag (Wait for value to be 1 then write 1)

Processor Interface and General Control

◆ I2C slave Interface

- Standard I2C protocol up to 400KHz

- Hardware considerations

➡ [See schematic](#)

- ◆ SDA and SCL pins should be connected to an I2C Master
- ◆ 2K Ω (+/-5%) pull-up resistors to 1.8V or 3.3V recommended for each signal

- Software considerations

- ◆ Contains four memory maps

- “Main” register device address is 0x72 (where the R/W~ bit is the LSB)
 - Contains all non-CEC status and control registers
- “Packet Memory” device address is set by register 0x45 of the Main map.
 - Default setting is 0x70
- “EDID Memory” device address is set by 0x43 of the Main map
 - Default setting is 0x7E
 - Used to store EDID that is automatically retrieved from HDMI sink device
- “CEC Memory” device address is set by 0xE1 of the Main map
 - Default setting is 0x78
 - Used for CEC related control and command storage

Processor Interface and General Control

◆ Interrupts

● INT pin enables interrupt driven system design

- ◆ Connect to the input of the system controller

➔ [See schematic](#)

- ◆ Should be pulled up to the power rail that supplies power to the system controller (either 1.8V or 3.3V) through a resistor (2KΩ to 5KΩ)

● List of Interrupts (green text indicates most commonly used basic interrupts)

◆ Hot Plug Detect (HPD)

- Edge sensitive

◆ Rx Sense

- Edge sensitive

◆ EDID Ready

- EDID successfully uploaded and ready to parse

◆ Active Vsync Edge

- Can be used when dynamically changing video-related parameters such as color space

◆ Audio FIFO Full

◆ Embedded Sync Parity Error

◆ HDCP Authenticated

◆ HDCP Error

◆ BKSX Flag

◆ Wake Up Op Codes

◆ CEC Tx Ready Flag

◆ CEC Tx Arbitration Lost Flag

◆ CEC Tx Retry Timeout Flag

◆ CEC Rx Ready Flags

● Interrupt-related registers (Main map)

- ◆ Interrupts and their enable bits are found in registers 0x92 – 0x97

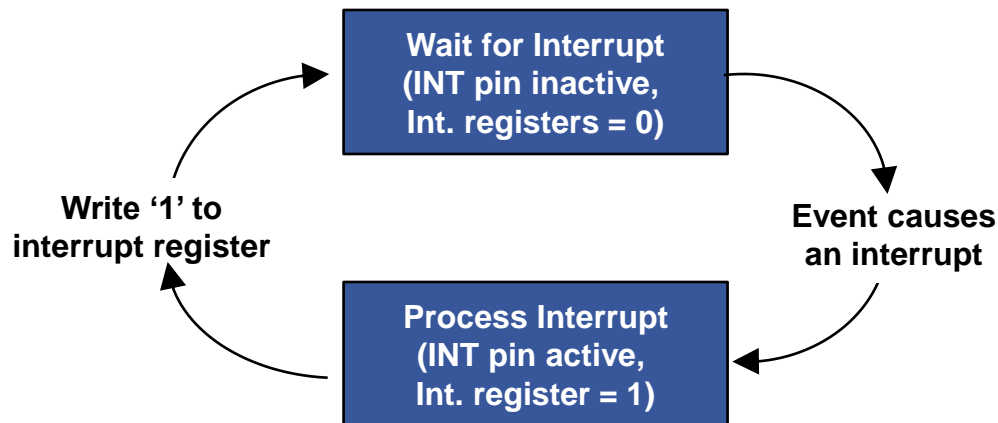
- ◆ “Status” bits are also available for system level monitoring (HPD and Rx_sense for ex.)

Processor Interface and General Control

◆ Interrupts (continued)

● Interrupt handling

- ◆ The figure below shows the process of detecting and clearing an interrupt
- ◆ The interrupt pin and interrupt register become active simultaneously when an event triggers an interrupt
- ◆ System software processes the interrupt, and then writes a '1' to the interrupt register to clear the register and set the interrupt pin back to inactive
- ◆ The pin will remain active until each active interrupt register is cleared
- ◆ Interrupt handling example in Programming Guide



Processor Interface and General Control

◆ Hot-plug Detect (HPD)

● Detects if a DVI or HDMI sink is connected

- ◆ Voltage on HPD > 1.2V = sink is connected

● Hardware considerations

- ◆ HPD connects directly to HDMI connector
 - 10KΩ pull down resistor to ground recommended
 - ESD device may also be connected

➔ [See schematic](#)

● Software considerations

- ◆ Use HPD interrupt or status (R0x42[6]) to initiate ADV7511 configuration
 - Start with powering up the device via R0x41[6]
 - “Quick-Start Guide” section provided in the Programming Guide
- ◆ When HPD is low, some registers will be reset to their default values and cannot be written to:

Address (Main Map)	HPD Pin	Power Down (0x41[6])	Full Reset (0xF8[7])
0x00 – 0x7C	Reset	Not Reset	Reset
0x92 – 0xAE	Not Reset	Not Reset	Reset
0xAF-0xCC	Reset	Reset	Reset
0xCE -0xFF	Not Reset	Not Reset	Reset

Processor Interface and General Control

◆ Display Data Channel (DDC) Controller

- I2C master connected to DDCSDA and DDCSCL pins of HDMI connector
 - ◆ 1.5K – 2.0K Ω pull up resistor to the HDMI +5V supply required on each
 - ◆ ESD device may also be connected

● Usage

- ◆ EDID download and buffering from sink device ➡ [See schematic](#)
 - Done automatically when R0xC9[4] set from '0' to '1'
 - EDID information is stored in EDID Memory Map
 - Information is used by system software to configure HDMI output appropriately for sink device
- ◆ HDCP handling
 - Refer to Programming Guide

◆ Current Reference

- The ADV7511 uses an external resistor connected to the R_EXT pin to accurately set the internal reference currents
 - ◆ Connect 887 Ω ($\pm 1\%$) resistor from R_EXT to ground
 - ◆ Avoid routing high-speed AC or noisy signals next to the R_EXT trace or resistor



Video Input

◆ Supported Formats

Color Space	Bits per Color	Format	Sync Type	Clocks
YCbCr or RGB	8, 10, or 12	4:2:2 or 4:4:4	Separate or Embedded	1x, 2x or DDR

◆ Hardware Considerations

● Video data input

- ◆ Can use bus widths (number of pins) of 8, 10, 12, 16, 20, 24, 30, or 36 bits
- ◆ Pin mapping and bus width set according to “Input ID” and “Input Style”
- ◆ Use 50Ω trace impedance on PCB

● Sync input

- ◆ Accepts Hsync, Vsync, and DE signals on separate pins or as embedded data on the video data pins

● Clock Input

- ◆ Low-jitter, low-noise clock = best performance (max jitter is 2nS)
- ◆ Use 50Ω trace impedance on PCB (minimize trace length)



Video Input

◆ Software Considerations

- “Input ID” register (0x15[3:1]) should be set to reflect the video data format, color space, bus width, # bits per color, and sync type that is input to the ADV7511 from the system SoC

Input ID	Bits per Color	Bus Width	Format Name	Sync Type
0	8, 10, 12	24,30,36	RGB 4:4:4 or YCbCr 4:4:4	Separate syncs
1	8, 10, 12	16,20,24	YCbCr 4:2:2	Separate syncs
2	8, 10, 12	16,20,24	YCbCr 4:2:2	Embedded syncs
3	8, 10, 12	8,10,12	YCbCr 4:2:2 2X clock	Separate syncs
4	8, 10, 12	8,10,12	YCbCr 4:2:2 2X clock	Embedded syncs
5	8, 10, 12	12,15,18	RGB 4:4:4, YCbCr 4:4:4 DDR	Separate syncs
6	8, 10, 12	8,10,12	YCbCr 4:2:2 DDR	Separate syncs
7	8,10,12	8,10,12	YCbCr 4:2:2 DDR	Separate syncs
8	8,10,12	8,10,12	YCbCr 4:2:2 DDR	Embedded syncs

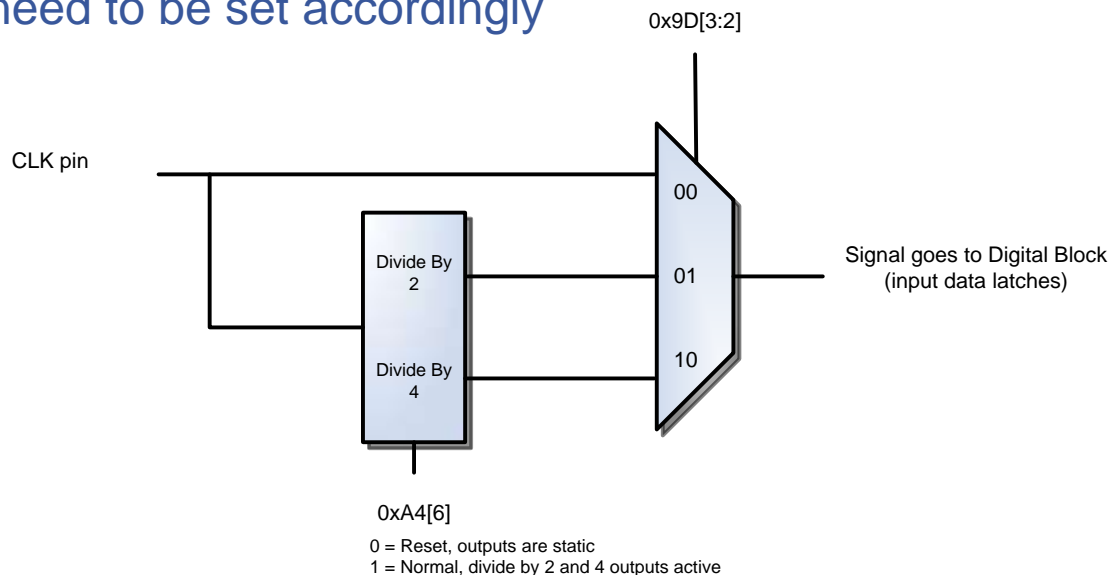
- “Color Depth” register (0x16[5:4]) sets the bits-per-color at the input
 - ◆ 10 = 12 bit, 01 = 10 bit, 11 = 8 bit
- “Input Style” register (0x16[3:2]) sets the pin mapping for video input data
 - ◆ 01 = style 2, 10 = style 1, 11 = style 3
 - ◆ See Programming Guide or Hardware User’s Guide for pin mapping details

Video Input

◆ Software Considerations (continued)

● Input data clock

- ◆ For formats with clock at 2 or 4 times the frequency of the data (480i at 27MHz, for example) “CLK Divide” (0x9D[3:2]) and “CLK Divide Enable” (0xA4[6]) need to be set accordingly



- ◆ “Clock Delay” (0xBA[7:5]) setting can be used to better align the clock with data to ensure robust data capture



Video Input

◆ Software Considerations (continued)

● Synchronization

◆ Separate Syncs using Hsync, Vsync, and DE pins

- All 3 signals are transmitted as part of the HDMI interface
- DE can be generated internally (registers 0x17[0], 0x35-0x3A) if Vsync and Hsync only are provided

◆ Embedded Syncs

- F, H, and V codes from the embedded syncs define the DE
- H and V syncs must be generated using the Hsync and Vsync Generator
 - Automatically enabled when using Video ID's 2 and 4
 - Registers 0x30 – 0x34 and 0x17[6:5]

◆ Adjustments

- The DE and sync generation circuits can also be used to adjust timing parameters to conform to the CEA861 specification as required by the HDMI specification
 - See Programming Guide for details



Audio Input

- ◆ **Supports I2S, and SPDIF audio from 32KHz up to 192KHz**
 - **I2S formats**
 - ◆ Standard
 - ◆ left-justified
 - ◆ right-justified
 - ◆ direct AES3 stream
 - **SPDIF formats**
 - ◆ 2-channel LPCM
 - ◆ IEC61937 encoded multi-channel audio
- ◆ **Supports advanced audio formats**
 - **Direct Stream Digital audio (DSD)**
 - ◆ Up to 8 data lanes
 - **HBR**
 - ◆ I2S Style
 - ◆ BPM Style
 - ◆ Refer to IEC61937
 - **Direct Stream Transfer (DST)**
 - ◆ Refer to IEC14496



Audio Input

◆ Hardware Considerations

- I2S requires SCLK and LRCLK input (MCLK is optional)
- SPDIF does not require a separate sampling clock (MCLK optional)
- Match trace length of audio signals to optimize audio data capture
- Add series termination resistors close to the audio source to minimize the effect of impedance mismatch
- **DSD**
 - ◆ DSD clock and data are 64 times the corresponding PCM sampling frequencies
 - ◆ DSD[7:6] input use the I2S[3:2] pins
- **HBR**
 - ◆ Both four stream and one stream HBR modes are supported
 - Can use the I2S[3:0] input pins or SPDIF input pin for either mode
 - ◆ Four stream mode using SPDIF is recommended
 - Channel Status bits are embedded in this mode so they do not need to be set manually
 - ◆ MCLK is required for the BPM encoding modes
- **DST**
 - ◆ DST is compressed DSD and uses the DSD[5:4] and DSD_CLK input pins
 - DSD[5] is the frame flag, DSD[4] is used for audio data



Audio Input

◆ Software Considerations

- **“Audio Select” (R0x0A[6:4]) is used to select audio type**
 - ◆ I2S ('000'), SPDIF ('001'), DSD, ('010'), HBR ('011'), or DST ('100')
- **“Audio Mode” (R0x0A[3:2]) is used to select the audio transmission method when using one of the advanced audio formats (DSD, HBR, DST)**
- **I2S**
 - ◆ R0x0C[1:0] selects I2S format (standard, right, left, AES3 direct)
 - ◆ Use “MCLK I2S” bit (R0x0A[2]) to enable MCLK using the Hsync input
 - Must set “MCLK Mux” bit (0xD6[6]) and “HSYNC/MCLK Schmitt Enable” bit (0xE5[3])
- **SPDIF**
 - ◆ “SPDIF Enable” (0x0B[7]) enables the SPDIF receiver
 - ◆ The “SPDIF Sampling Frequency” register (0x0A[7:4]) indicates the detected audio sampling frequency



Audio Input

◆ Software Considerations (continued)

● HBR

- ◆ The sampling frequency in the General Control Packet must be set to 768 kHz. This can be set by $(0x15[7:4] = 9)$
- ◆ Re-mapping of the inputs may need to be adjusted if using non-ADI HDMI Rx devices as the input. This is set in registers 0x0E through 0x11
- ◆ Audio Mode register (0x0A[3]) selects four-stream or one-stream encoding
- ◆ Audio Mode register (0x0A[2]) enables BPM encoding if desired

● DSD

- ◆ If using DVD audio look into the necessity for setting the ACP packet

● DST

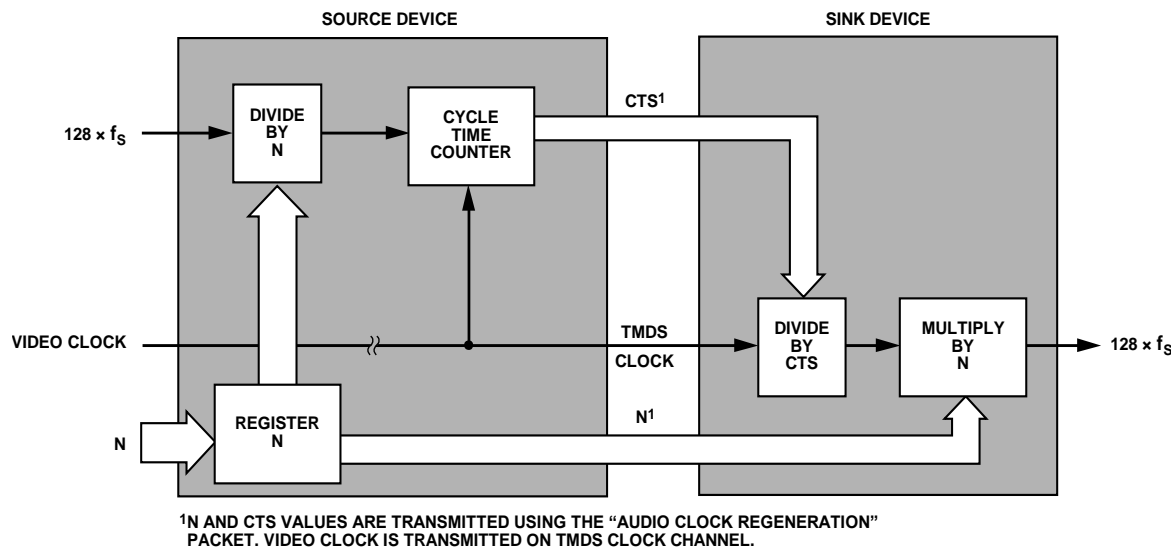
- ◆ If using DVD audio look into the necessity for setting the ACP packet

● See section 4.4 of the **ADV7511 PG** for details

Audio Input

◆ Audio Clock Regeneration

- Audio sampling rate clocks are derived from video clock



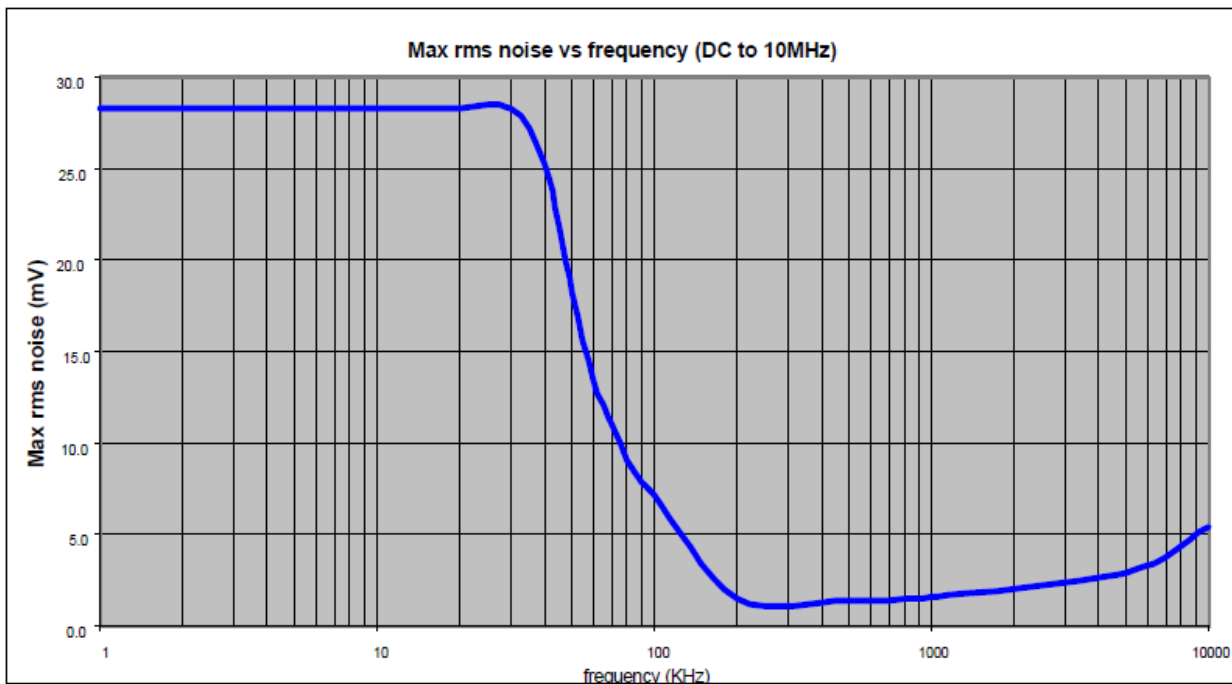
- N and CTS must be set appropriately for HDMI sink to recreate the audio clocks
 - ◆ N should be set according to tables 58-60 in Programming Guide
 - ◆ CTS is automatically generated based on detected audio and video rates when "CTS Source Select" (0x0A[7]) is set to auto mode

HDMI Output

- ◆ **“Output Format” register bit (0x16[7]) selects 4:2:2 or 4:4:4**
 - **Output color space is determined by the state of the Color Space Converter (CSC)**
 - ◆ The Y1Y0 bits of the AVI Infoframe (0x55[6:5]) should be set to match the HDMI output format
 - ◆ More information on the CSC on slide 30
- ◆ **HDMI uses 4 TMDS pairs**
 - **3 data pairs at up to 2.25GB**
 - **Clock pair up to 225MHz**
 - **Each pair should be routed differentially with 100Ω impedance (50Ω each to ground)**
 - **Low capacitance (<0.6pF) ESD suppressors recommended**
 - ◆ Placed as close as possible to the HDMI connector.
 - ◆ Differential TMDS lines should be routed through the pad of the ESD suppressor to minimize the disruption in the differential impedance

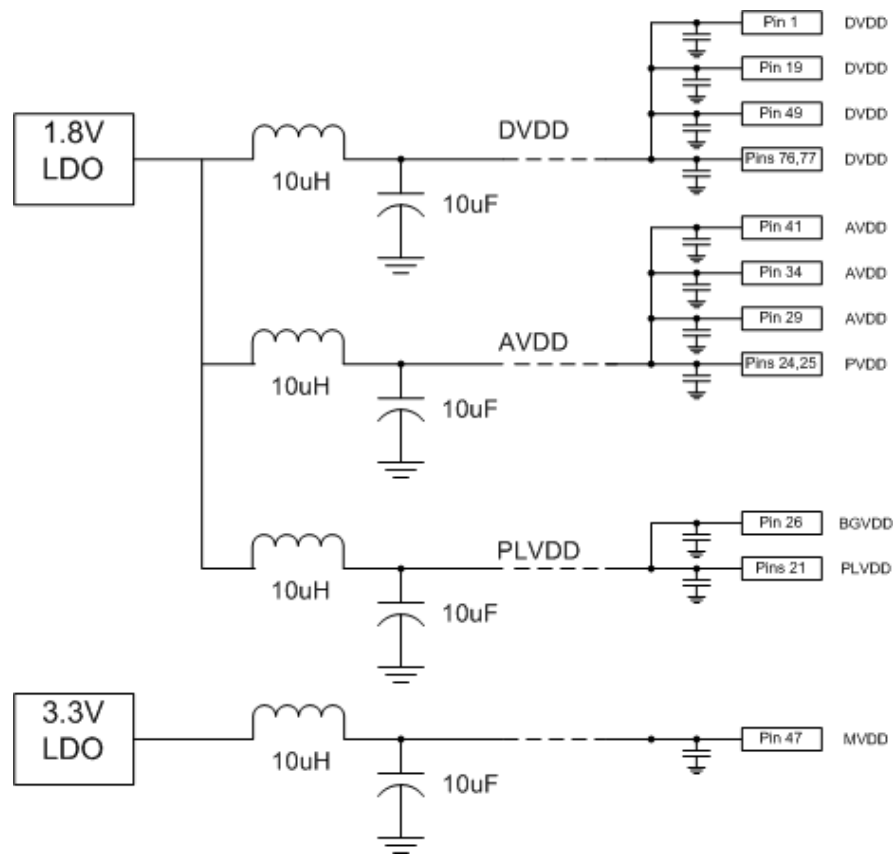
Power Supply Filtering

- ◆ All 1.8V supply domains need to be as noise-free as possible
- ◆ The graph below shows AVDD and PVDD Max Noise vs. Frequency



Power Domains

- ◆ **Four separate pcb power domains are recommended**
 - Each with low-pass filtering that has a cutoff frequency between 10 and 20KHz
 - Each power pin should have a 0.1uF bypass capacitor placed as close as possible to the pin



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Consumer Electronics Control (CEC)



What is CEC?

◆ CEC – Consumer Electronics Control.

- A subsection of the HDMI specification
- Not a required feature to be HDMI compliant.
- Basic function is to connect all HDMI equipped devices into a network, and be able to control any device on the network from any other device, e.g. TV remote control could control HS, DVC, DSC
 - ◆ Some typical commands are “one touch play”, “stand-by”, “Record”
 - ◆ Allows additional commands, which are defined by a device maker.

◆ Basic PHY spec

- Serial bit transmission mechanism.
- It is a very low speed bus (400Hz)
- Uses full CMOS signal swings (0V – 3.3V)

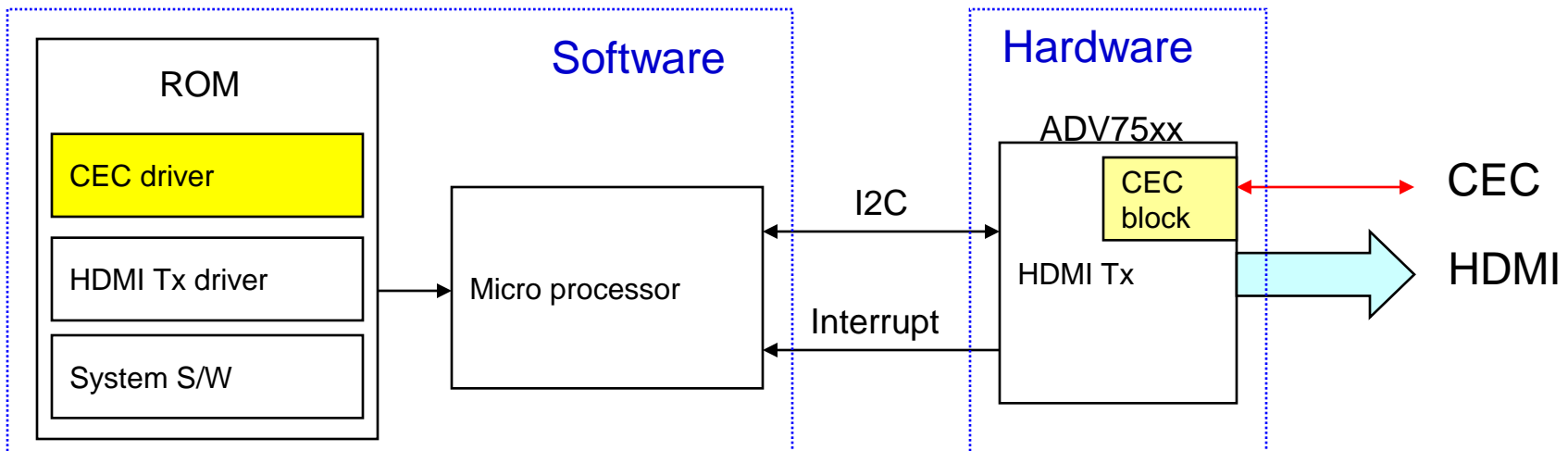


How is it being implemented in Tx?

- ◆ **The CEC bus specification is partitioned in its implementation.**
 - Electrical PHY, bit signaling, and transmission
 - High level MAC layer, command translation, logical address generation, transmission error handling
- ◆ **Controller implementation on Tx is an “enhanced PHY”**
 - All basic electrical operations, bit timings, etc.
 - Handles transmission errors and schedules re-transmission of faulty frames
- ◆ **Host processor will implement remainder of MAC layer functions.**
 - “Command to action” translation
 - Logical address generation
 - These are functions that would be implemented in Software

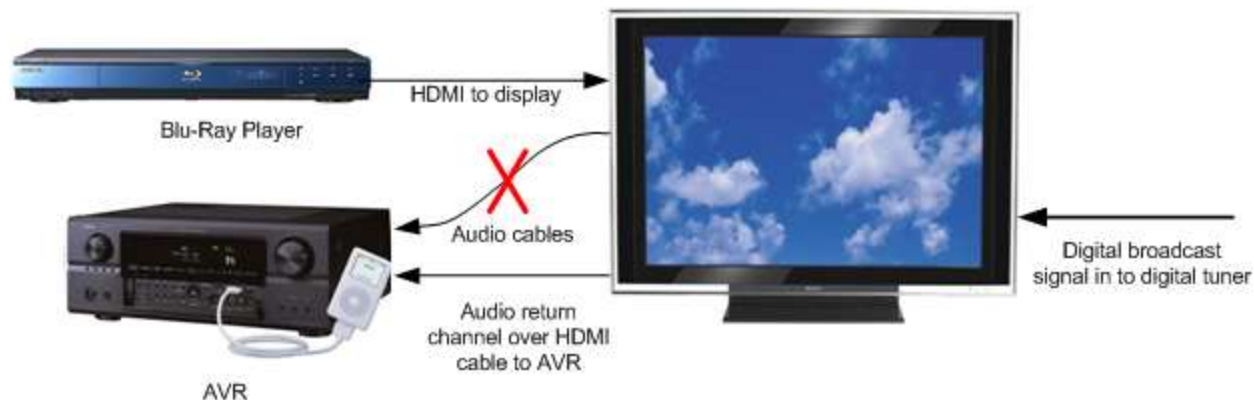
Block Diagram: ADI Solution

- ◆ **Combination of H/W and S/W.**
- ◆ **H/W is responsible for physical layer.**
 - Signal level and bit timing.
 - 0.1 – 5ms order.
- ◆ **S/W is responsible for (low level) application layer.**
 - Logical address, physical address
 - Respond to the received message automatically.
 - Data link between System S/W.
 - 5 - 50ms order.



Audio Return Channel

- ◆ **HDMI 1.4 provides for an audio return channel (ARC)**
 - Audio channel added to reduce the number of cables required to deliver audio “upstream” from a TV to an AVR for processing and playback.
 - In cases where a TV includes an internal content source (built-in tuner or DVD player), the ARC allows the TV to send audio data upstream to the AVR via the HDMI cable, eliminating the need for an extra cable.
 - ◆ Alternately, this feature could allow a television (or other sink device) to receive HDMI signals directly from an HDMI source but still provide a means to send the audio data to an AVR for processing
 - **Application example illustrated below**





ARC Receiver Features

- ◆ **Programmable input configuration**
 - Single-ended input on HEAC+ pin
 - Differential input on HEAC+, HEAC- pins
- ◆ **Power down circuit by itself or with chip power down**
- ◆ **Compliant the HDMI1.4a specification**
- ◆ **LPCM (IEC 60958-1) Audio Support via SPDIF_OUT pin**
 - 32KHz, 44.1KHz or 48KHz sampling rates

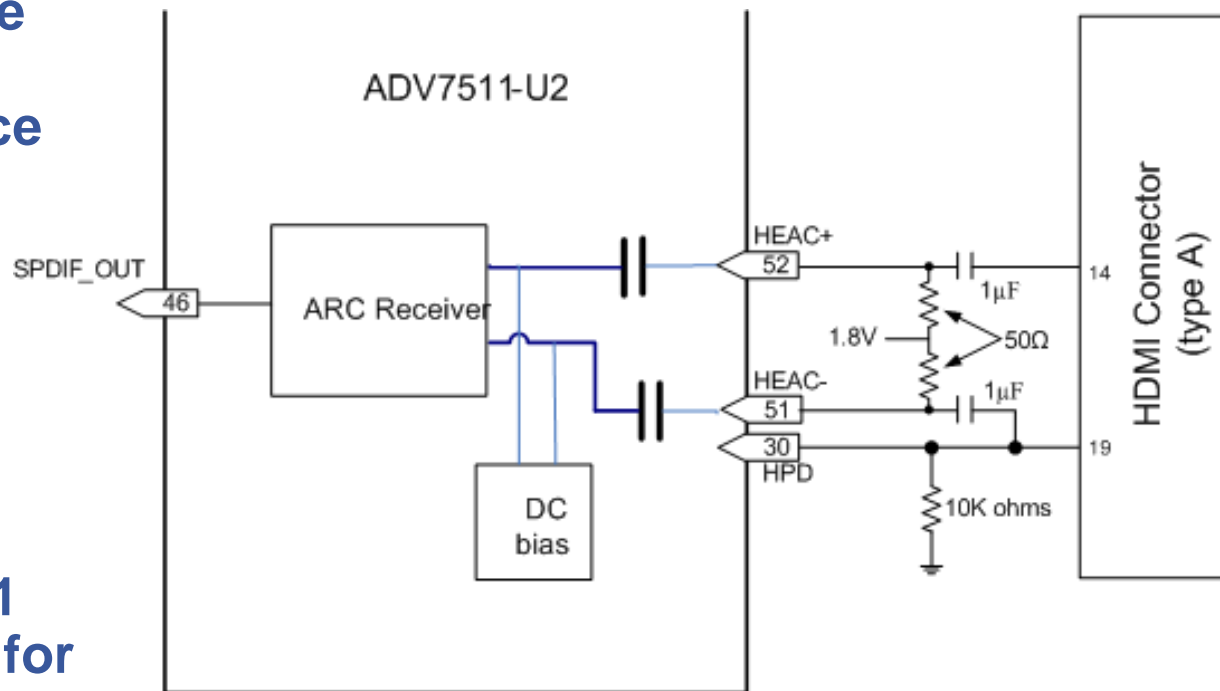
ARC Design Considerations

◆ Hardware configuration

- Route common-mode signals with 100Ω differential impedance
- Add external components as illustrated here

◆ Software

- Refer to the ADV7511 Programming Guide for setup instructions





Advanced Usage



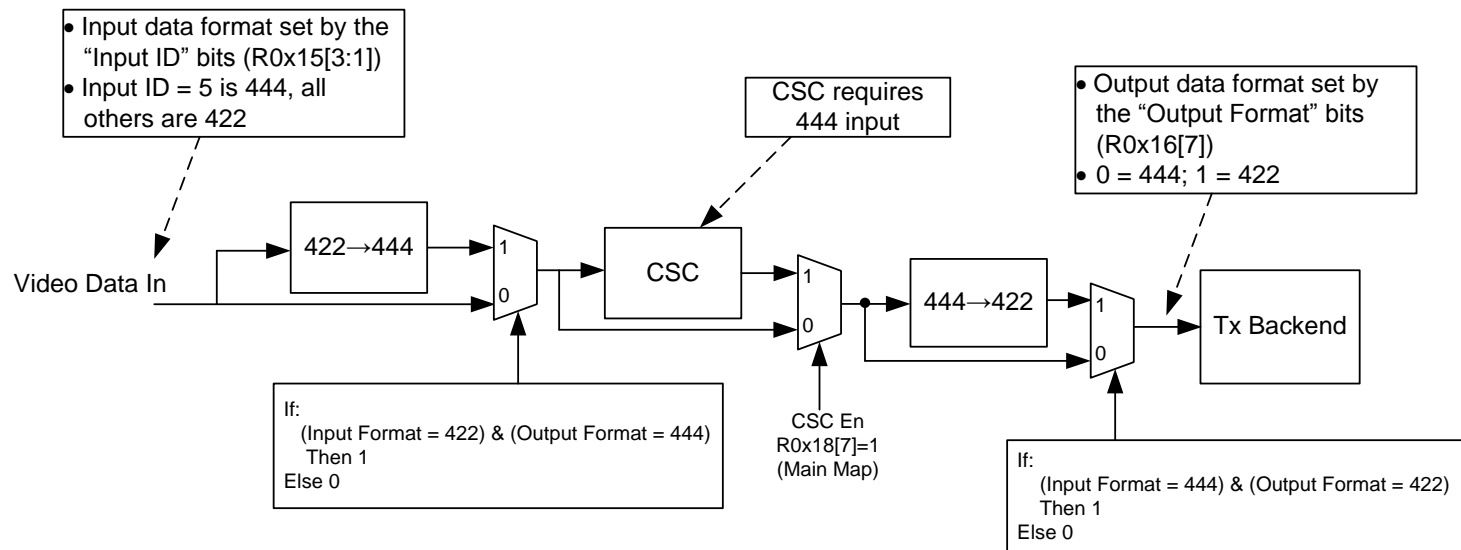
Video Formatting

◆ CSC (color space converter)

- **Used when color space is different between input and output**
 - ◆ RGB input to YCbCr output
 - ◆ YCbCr input to RGB output
- **Fully programmable**
 - ◆ CSC control registers at 0x18 - 0x2F
- **Settings for common color space conversions contained in Programming Guide**
 - ◆ HDTV YCbCr (16to 235) to RGB (16to 235)
 - ◆ HDTV YCbCr (16to 235) to RGB (0 to 255)
 - ◆ SDTV YCbCr (16to 235) to RGB (16 to 235)
 - ◆ SDTV YCbCr (16to 235) to RGB (0 to 255) - (Default Value)
 - ◆ RGB (16 to 235) to HDTV YCbCr (16to 235)
 - ◆ RGB (0 to 255) to HDTV YCbCr (16to 235)
 - ◆ RGB (16 to 235) to SDTV YCbCr (16to 235)
 - ◆ RGB (0 to 255) to SDTV YCbCr (16to 235)
 - ◆ Identity Matrix (Output = Input)

Video Formatting

- ◆ **4:2:2 to 4:4:4 and 4:4:4 to 4:2:2 conversion**
 - Used when input and output format doesn't match
 - No need to enable/disable the function. If the format doesn't match, it will be automatically enabled.
 - There are 2 options for 4:2:2 to 4:4:4 model
 - ◆ Zero-order (repetition)
 - ◆ First-order (linear interpolation)





Video Formatting

◆ Pixel Repetition

● Why is pixel repetition needed?

- ◆ To increase the amount of blanking period available to send packets
- ◆ To increase the pixel clock frequency to meet the minimum specified clock frequency (25MHz)

● Three modes of operation using 0x3B[6:5]

◆ Auto mode

- Uses the audio sampling rate and detected VIC information to determine if pixel repeat is needed to obtain sufficient blanking periods to send the audio

◆ Manual mode

- VIC sent in the AVI info should also be set in register 0x3C
- The multiplication factor of the input clock must be programmed in 0x3B[4:3]
- Pixel repeat value sent to the Rx must be programmed in 0x3B[2:1].

◆ Max mode

- Same as auto mode, except it selects the highest pixel repeat multiple possible
- Video timing is independent of the audio sampling rate
- Not typically used.

TMDS Power Down

- ◆ **Used to ensure no corrupted video is sent during register setup**
- ◆ **Procedure:**
 - **Power Down the TMDS Clock and Data right after setting 0x41[6] to 0 to power up the device**
 - **Power Up the TMDS lines when video input is stable and register settings are complete**
 - **Soft TMDS Clock Turn On is recommended if TMDS Power Down is used**
 - ◆ Helps avoid Rx Sense glitches caused by active Rx 3.3V termination
 - ◆ Enable by setting 0xD5[4] = 1 and 0xD6[3] = 1
- ◆ **Registers**
 - **Channel 0 to Channel 2 Power Down – 0xA1[5:3]**
 - ◆ ‘111’ = power down; ‘000’ = power up
 - **TMDS Clock Power Down - 0xA1[4]**
 - ◆ ‘1’ = power down; ‘0’ = power up

AV Mute

- ◆ **Used while HDCP is active to mute the audio and video without losing HDCP authentication**
- ◆ **Audio and Video are still sent, but a message is sent via the General Control Packet telling the sink to mute**
- ◆ **AV Mute is not suitable for blocking protected audio and video from the sink**
- ◆ **Procedure:**
 - **Enable the General Control Packet First**
 - ◆ $0x40[7] = 1$
 - **Next set the AV Mute Bits**
 - ◆ Set AV Mute by setting $0x4B[7:6] = '01'$
 - ◆ Clear AV Mute by setting $0x4B[7:6] = '10'$



Black Video Data

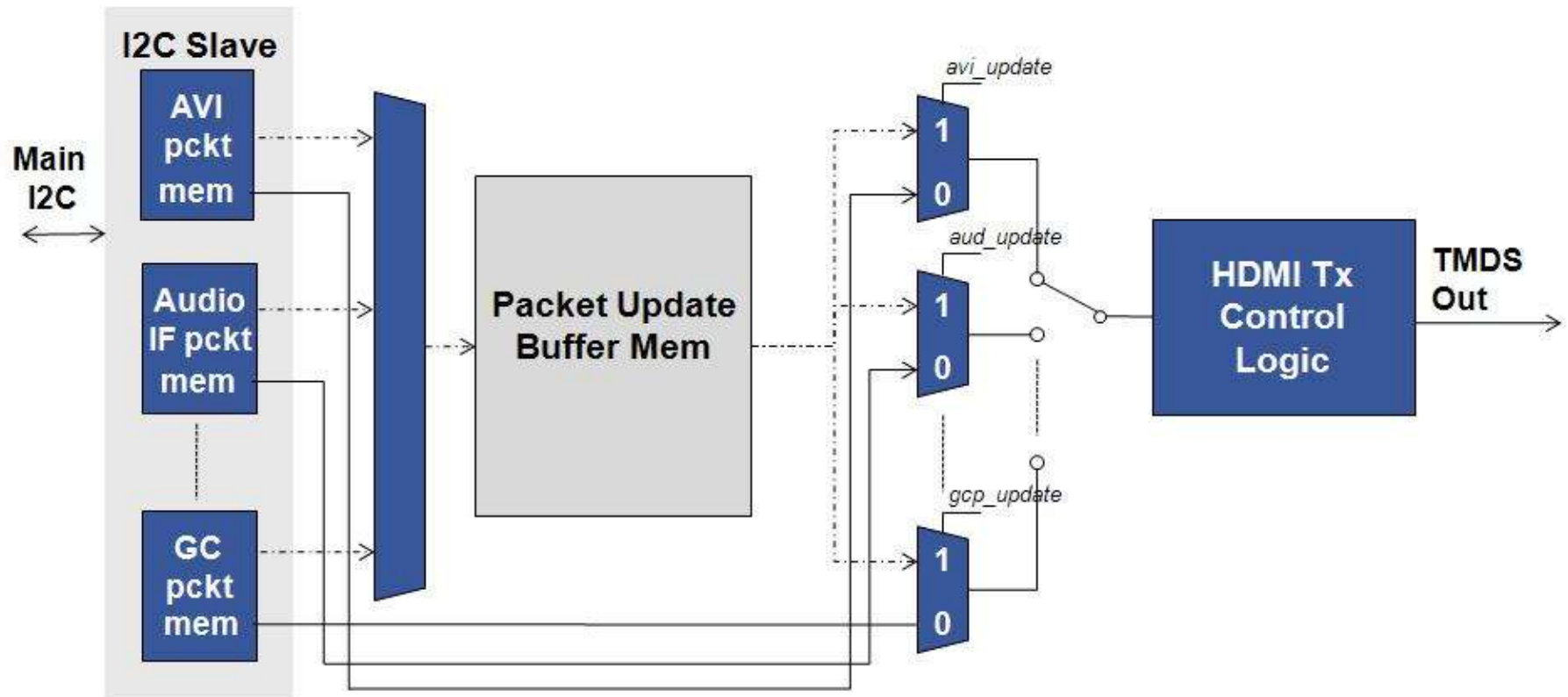
- ◆ **Black video data can sent from the Tx when unstable video data is at the input**
- ◆ **To send black video the color space converter can be used**
 - **CSC coefficients can be set to 0**
 - **Offsets can be set to the appropriate values for RGB or YCbCr in either full range or limited range**
- ◆ **Black video bit**
 - **A shortcut to blank the output video using CSC**
 - **The previous CSC settings will be preserved when black video is disabled**
 - **This is for 0-255 (full range) values only.**
 - **Register bit 0x16[0] selects between RGB and YCbCr mode**
 - **Register bit 0xD5[0] enables or disables black video data**



Packet Update Feature (1)

- ◆ A packet update feature is available to ensure that partially updated packets are not sent
- ◆ A bit is available for each packet to continue sending the current contents until update is complete
- ◆ The feature is available for the following packets:
 - AVI InfoFrame
 - MPEG InfoFrame
 - GMP Packet
 - Audio InfoFrame
 - GC Packet
 - SPD Packet
 - ACP Packet
 - ISRC1 Packet
 - ISRC2 Packet
 - Spare Packet1
 - Spare Packet2

Packet Update Feature (2) Block Diagram





HDCP

- ◆ **HDCP is always initiated with the following sequence**
 - Enable HDCP by setting $0xAF[7]$ to 1
 - Wait for BKS_V Ready Interrupt ($0x97[6]$) to be 1
 - Collect BKS_V from register map and check with revocation list
 - Clear BKS_V Ready Interrupt by writing $0x97[6] = 1$
- ◆ **If the Tx is connected to a single device, then HDCP authentication is complete**
- ◆ **Check that $0xAF[7]$ is still set to 1 at least once every 2 seconds until HDCP is disabled to avoid external register tampering**
- ◆ **If the Tx is connected to a repeater device, then the additional steps on the following page should be followed**

HDCP Repeater Case

- ◆ **After clearing the BKSV flag, if the interrupt occurs again...**
 - Additional BKSVs will be stored at I2C address 0x7E
 - These are available 13 BKSVs at a time
- ◆ **After reading the BKSVs clear flag again by writing 0x97[6] = 1**
 - If the interrupt occurs again...
 - Collect additional BKSVs from 0x7E
 - Continue this process until all BKSVs are read
 - ◆ One way to confirm that all BKSVs have been read is to check if the “HDCP Authenticated” interrupt 0x96[1] has occurred
 - ◆ Another way is to confirm this is to check that the BKSV ready interrupt 0x97[6] remains 0 after clearing it
 - The ADV7511 supports up to 128 BKSVs, which is the maximum number allowed by HDCP 1.3