EVALUATION BOARD OVERVIEW

This document explains the design and setup of the AD1940 SigmaDSP evaluation board.

The EVAL-AD1940AZ provides a full range of analog and digital inputs and outputs to and from the AD1940. The SigmaDSP can connect to analog I/O signals through the AD1939 codec and AD1974 ADC. Digital I/O connections are available in both S/PDIF and 3-wire serial data formats. The DSP is controlled by Analog Devices’ SigmaStudio™ software, which interfaces to the evaluation boards with a USB cable via the EVAL-ADUSB2EBZ add-on board, also known as the USBi. Power is distributed by a single DC supply, which is regulated to the necessary voltages on the board. The PCB is an 7” x 5” 4-layer design with split analog and digital power and ground planes on the two inner layers.

The AD1940 evaluation board should be used for AD1941 evaluation. There is no AD1941 evaluation board.

PACKAGE CONTENTS

The EVAL-AD1940AZ package contains these items:
- AD1940 evaluation board
- EVAL-ADUSB2EBZ (USBi) communications adapter
- 6V DC power supply with standard US plug
- USB cable with mini-B plug
- Evaluation board/software quick-start guide
- SigmaStudio software

OTHER SUPPORTING DOCUMENTATION

AD1940/AD1941 datasheet
AD1939 datasheet
AD1974 datasheet
SigmaStudio Help (included in the software installation)
AN-1006: Using the EVAL-ADUSB2EBZ

FUNCTIONAL BLOCK DIAGRAM

Figure 1. Functional Block Diagram
Figure 2. Board Layout Block Diagram
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SETTING UP THE EVALUATION BOARD

SIGMASTUDIO SOFTWARE INSTALLATION

1. Open the provided .zip file and extract the files to your PC. Alternately, insert the SigmaStudio CD into the computer's optical drive and browse the CD to the SigmaStudio folder.

2. Install Microsoft .NET Framework ver2.0, if you do not already have it installed. (Do this by double-clicking dotnetfx.exe)

3. Install SigmaStudio by double-clicking setup.exe, and following the prompts. A computer restart is not required.

POWERING THE BOARD

The board is powered by the included 6V DC power supply, which should be connected to power jack J14. The power indicator LEDs D3 and D2 should be lit.

HARDWARE SETUP - USBI

4. Plug the USBi into the PC’s USB port using the included mini USB cable. Plug in the USBi into the control port J2 on the eval board (marked yellow on Figure 1).

5. Connect the USB cable to your computer, and to the USBi.

6. When prompted for drivers:
   • Choose “Install from a list or a specific location.”
   • Choose “Search for the best driver in these locations.”
   • Check the box for “Include this location in the search.”
   • The USBi driver is located in C:\Program Files\Analog Devices Inc\Sigma Studio\USB drivers, click Next.
   • If prompted to choose driver, select CyUSB.sys
   • In XP click Continue Anyway if you are prompted saying the software hasn’t passed Windows Logo testing.

CONNECTING THE AUDIO CABLES

For this example, we will set up the board to have stereo analog inputs and stereo analog outputs.

7. Connect the audio source to the ANALOG INPUT CHANNEL 0-1 jack J15 (marked blue in Figure 1) on the top of the board, using a 1/8” cable.

8. Connect the ANALOG OUTPUT CHANNEL 0-1 jack J18 (marked green in Figure 1) to your active speakers or headphones.

SWITCH AND JUMPER SETTINGS

In order to configure the board for stereo analog in and out, make sure the switches and jumpers are set as indicated in Figure 3.

A black rectangle indicates a connected jumper or switch position.
YOUR FIRST SIGMASTUDIO PROJECT – EQ AND VOLUME CONTROL

1. Create a new project. The Hardware Configuration Tab will be open.

2. Drag an AD1940 and a USBi cell into the blank white space.

3. Connect the USBi cell to the AD1940 cell by clicking and dragging from the top blue output pin to the green input pin.

Your screen should now look something like Figure 4.

4. Click on the Schematic tab at the top of the screen.

5. In the cell Toolbox expand the IO → Input. Click&Drag an Input cell to the work area.

6. Similarly, expand Filters → Second Order → Double Precision → 2 Ch and click&drag Medium Size Eq

7. Right click the General (2nd Order) cell labeled Gen Filter1, click Grow Algorithm → 1.2 Channel – Double

Figure 3. Evaluation Board Default Setup and Configuration

Figure 4. Hardware Configuration Tab
Precision → 4. This creates a five band EQ. Each band’s general filter settings can be modified by clicking the blue boxes on the cell.

8. Expand Volume Controls → Adjustable Gain → Shared Slider → Clickless SW Slew and click&drag Single slew

9. Expand the IO → Output. Click&Drag two Output cells

10. Connect all the cells as depicted in Figure 3.

11. Make sure your board is powered and connected to the PC. Click the Link-Compile-Download button in SigmaStudio.

12. If the project compiled without error you will be in Ready-Download mode.

Your screen should now look something like Figure 5.

13. Start your audio source playing, and you should hear audio. You can now move the volume control and filter sliders and hear the effect on the output audio in real time.

The online documentation contains more tutorials and detailed information about every cell available.
USING THE EVALUATION BOARD

**AD1940 SIGMADSP**

The AD1940 is a complete 28-bit, single-chip, multi-channel audio SigmaDSP™ for equalization, multiband dynamic processing, delay compensation, speaker compensation, and image enhancement. These algorithms can be used to compensate for the real world limitations of speakers, amplifiers, and listening environments, resulting in a dramatic improvement of perceived audio quality.

The signal processing used in the AD1940 is comparable to that found in high end studio equipment. Most of the processing is done in full, 56-bit double-precision mode, resulting in very good, low level signal performance and the absence of limit cycles or idle tones. The dynamics processor uses a sophisticated, multiple-breakpoint algorithm often found in high end broadcast compressors.

The AD1940 is a fully programmable DSP. Easy to use software allows the user to graphically configure a custom signal processing flow using blocks such as biquad filters, dynamics processors, and surround sound processors. An extensive control port allows click-free parameter updates, along with readback capability from any point in the algorithm flow.

The AD1940’s digital input and output ports allow a glueless connection to ADCs and DACs by multiple, 2-channel serial data streams or TDM data streams. When in TDM mode, the AD1940/AD1941 can input 8 or 16 channels of serial data, and can output 8 or 16 channels of serial data. The input and output port configurations can be individually set. The AD1940 is controlled by a 4-wire SPI® port.

The EVAL-AD1940AZ should be used to evaluate both the AD1940 and the AD1941, which is equivalent to the AD1940 except for its I²C control interface.

**POWER**

The evaluation board uses two ADP3339 low-dropout voltage regulators to generate the 3.3 V analog and digital supplies. The current consumption of the board is approximately 500 mA at a maximum.

The regulators’ inputs should be supplied with +5 to +6 V DC power on connector J14. The power supply should have a female cord plug with a 2.1 mm inner diameter, 5.5 mm outer diameter, and 9.5 mm length. The polarization should be positive-center.

A lab supply can also be used to power the board, and should be connected across test points TP48 (VIN+) and TP70 (GND).

**CLOCKING THE EVALUATION BOARD**

The EVAL-AD1940AZ requires a master clock (MCLK) to operate. The master clock can be supplied from a variety of sources, and is used to clock the AD1940 DSP, AD1974 ADCs, AD1939 ADCs/DACs, External Digital Audio Interfaces, and the S/PDIF Transmitter.

In most common board configurations, MCLK will be generated by the on-board AD1939. The AD1939 has an internal oscillator that drives a 12.288 MHz crystal to produce a 12.288 MHz master clock suitable for 48 kHz, 96 kHz, and 192 kHz processing applications.

For configurations utilizing the S/PDIF receiver, MCLK must be supplied to the system by the recovered MCLK of the S/PDIF stream. This recovered MCLK has a frequency 256 times the sample rate of the S/PDIF data.

A master clock can also be supplied from an external (off-board) source on the digital audio interface headers J22, J23, and J24. The corresponding MCLK direction switch should be set to IN or OUT as required.

A description of the jumpers used to route MCLK is given in Table 1. Examples of common MCLK configurations are given in the Example Configurations section of this document and in Figure 6.

### Table 1. Master Clock Routing

<table>
<thead>
<tr>
<th>Component</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>Select MCLK Source/Destination</td>
</tr>
<tr>
<td>J3</td>
<td>Enable AD1939 Crystal Oscillator Circuit</td>
</tr>
<tr>
<td>SW3</td>
<td>Set direction of MCLK on H1 (J22)</td>
</tr>
<tr>
<td>SW4</td>
<td>Set direction of MCLK on H2 (J23)</td>
</tr>
<tr>
<td>SW5</td>
<td>Set direction of MCLK on H3 (J24)</td>
</tr>
</tbody>
</table>

![Figure 6. Example Master Clock Routing Settings](image)

The AD1940 must be set up to properly receive MCLK as an input to its PLL. The board will most often be used with a 12.288 MHz master clock, which is equivalent to 256×Fₛ, with...
F_\text{c} = 48 \text{ kHz}. In order to set up the AD1940 PLL in 256xF_c mode, switch SW1 must be set up as shown in Figure 7.

![Figure 7. PLL Mode Selection for 12.288 MHz Master Clock](image)

A description of all possible PLL settings is shown in Table 2, with 0 corresponding to setting the switch to the right, a 1 corresponding to setting the switch to the left, and “don’t care” represented as an “X.”

<table>
<thead>
<tr>
<th>PLL Mode</th>
<th>PLL-CTRL0 SW1-1</th>
<th>PLL-CTRL1 SW1-2</th>
<th>PLL-CTRL2 SW1-3</th>
</tr>
</thead>
<tbody>
<tr>
<td>64xF_c</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>256xF_c</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>384xF_c</td>
<td>X</td>
<td>X</td>
<td>0</td>
</tr>
<tr>
<td>512xF_c</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Bypass</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

The ADR-SEL switch (SW1-4) determines the SPI address of the AD1940. The default is 0 (switch to the right).

**INPUT ROUTING**

Audio data is routed to the AD1940 via four jumpers: J4, J5, J6, and J7. A description of these jumpers is in Table 3.

<table>
<thead>
<tr>
<th>Component</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>J4</td>
<td>Select data to input to AD1940 – SDATA_IN0</td>
</tr>
<tr>
<td>J5</td>
<td>Select data to input to AD1940 – SDATA_IN1</td>
</tr>
<tr>
<td>J6</td>
<td>Select data to input to AD1940 – SDATA_IN2</td>
</tr>
<tr>
<td>J7</td>
<td>Select data to input to AD1940 – SDATA_IN3</td>
</tr>
</tbody>
</table>

Input clocks are configured via two jumpers: J8 and J9. A description of these jumpers is in Table 4.

<table>
<thead>
<tr>
<th>Component</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>J8</td>
<td>Select frame clock source for AD1940 serial input ports</td>
</tr>
<tr>
<td>J9</td>
<td>Select bit clock source for AD1940 serial input ports</td>
</tr>
</tbody>
</table>

The AD1940 serial input ports are always configured as slaves, so clocks must always be supplied from another source in order for them to function.

**ANALOG AUDIO INPUTS**

The EVAL-AD1940AZ has three stereo 1/8” input jacks, allowing for a total of 6 channels of analog audio input. Input channels 0-3 are routed to the AD1939 ADCs and input channels 4-5 are routed to the AD1974 ADCs. In order to input the converted audio data to the AD1940 DSP, it must be routed appropriately using the audio data routing jumpers.

Proper configuration for inputting all analog audio to the DSP is shown in Figure 8. Note that it is not necessary to use all analog audio inputs simultaneously, and the jumpers can be set in any desired configuration to allow for flexibility in routing a combination of analog, digital, and S/PDIF inputs.

![Figure 8. Input Routing Jumpers - Analog Configuration](image)

In an analog input configuration the AD1939 will most commonly be used as the source for LRCLK and BCLK signals. To route this signals to the AD1940’s LRCLK_IN and BCLK_IN pins, configure the jumpers J8 and J9 as shown in Figure 9.

![Figure 9. LRCLK_IN/BCLK_IN Routing Jumpers - Analog Configuration](image)

With the jumpers configured as shown in Figure 8 and Figure 9, the analog input signals will appear in SigmaStudio as input channels 0-5, as shown in Figure 10.
EXTERNAL DIGITAL AUDIO (I²S/TDM) INPUTS

The EVAL-AD1940AZ has a digital interface input header (J22) with connections for MCLK, LRCLK, BCLK, and four serial data lines, allowing for a total of 8 channels of serial audio input (I²S, right-justified, or left-justified) or up to 16 channels when TDM modes are used. In order to input the audio data to the AD1940 DSP, it must be routed appropriately using the audio data routing jumpers.

Proper configuration for inputting all I²S/TDM audio to the DSP is shown in Figure 11.

When data is supplied on the digital interface input header, there are two options for LRCLK and BCLK routing. First, the AD1939 can be the clock master. This configuration is shown in Figure 12.

Alternatively, the LRCLK and BCLK signals can be taken from an external source over the LRCLK_IN and BCLK_IN pins of the digital interface input header J22. This configuration is shown in Figure 13.

With the jumpers configured as shown in Figure 12 and Figure 13, the external I²S input signals will appear in SigmaStudio as input channels 0-7, as shown in Figure 14.

S/PDIF RECEIVER

The EVAL-AD1940AZ has an S/PDIF receiver with both optical and coaxial connections, allowing for a total of 2 channels of S/PDIF audio to be input to the AD1940. In order to input the audio data to the AD1940 DSP, it must be routed appropriately using the audio data routing jumpers.

Proper configuration for inputting all S/PDIF audio to the DSP is shown in Figure 16.
Because the S/PDIF receiver is always a clock master to the AD1940, the LRCLK_IN and BCLK_IN lines must be connected to the S/PDIF receiver as shown in Figure 17.

The master clock must also be provided from the S/PDIF receiver. For proper operation, J1 should have a jumper on “DIR” and J3 should be set to “EXT.”

The S/PDIF receiver can only input data from one connector at a time. To select the optical connector, set switch SW6 in the up position. To select the coaxial electrical connector, set switch SW6 in the down position.

With the jumpers configured as shown in Figure 16 and Figure 17, the S/PDIF inputs will appear in SigmaStudio as shown in Figure 18.

**OUTPUT ROUTING**

The AD1940 serial output ports are always connected to the DACs, digital audio output headers, and S/PDIF transmitter. These data signals do not require any jumpers or switches to be output properly. The AD1940 serial output ports can be configured as either masters or slaves. If the AD1940’s serial output ports are configured as masters, then jumpers J10, J11, J12 and J13 can be left disconnected. If the AD1940’s serial output ports are configured as slaves, then jumpers J10, J11, J12 and J13 must be connected in order to output data. The functionality of these jumpers is described in Table 5.

**Table 5. Output Clock Routing**

<table>
<thead>
<tr>
<th>Component</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>J10</td>
<td>Connect LRCLK_OUT0 to LRCLK_IN. Must be connected if serial output channels 0-7 are configured as slaves and not externally clocked.</td>
</tr>
<tr>
<td>J11</td>
<td>Connect BCLK_OUT0 to BCLK_IN. Must be connected if serial output channels 0-7 are configured as slaves and not externally clocked.</td>
</tr>
<tr>
<td>J12</td>
<td>Connect LRCLK_OUT1 to LRCLK_IN. Must be connected if serial output channels 8-15 are configured as slaves and not externally clocked.</td>
</tr>
<tr>
<td>J13</td>
<td>Connect BCLK_OUT1 to LRCLK_IN. Must be connected if serial output channels 8-15 are configured as slaves and not externally clocked.</td>
</tr>
</tbody>
</table>

**ANALOG AUDIO OUTPUTS**

The EVAL-AD1940AZ has four stereo 1/8’ input jacks, allowing for a total of 8 channels of analog audio output. Output channels 0-7 are routed to the AD1939 DACs. The analog outputs are hardwired to the AD1940’s serial output ports and are always active.

The analog outputs 0-7 correspond to outputs 0-7 in SigmaStudio.

**EXTERNAL DIGITAL AUDIO (I²S/TDM) OUTPUTS**

The EVAL-AD1940AZ has two external digital interface output headers, J23 and J24, with connections to all eight SDATA_OUT data lines, and two pairs of output LRCLK/BCLK lines. These output headers are hardwired to the AD1940’s serial output ports and are always active.

The I²S/TDM outputs 0-15 correspond to outputs 0-15 in SigmaStudio.

**S/PDIF TRANSMITTER**

The EVAL-AD1940AZ has an S/PDIF transmitter with both optical and coaxial electrical outputs. These outputs are hardwired to the AD1940 and are always active.

The S/PDIF outputs 0-1 correspond to outputs 8-9 in SigmaStudio.
EXAMPLE CONFIGURATIONS

ANALOG IN/OUT MODE

ACTIVE CHANNELS:

0 2 4 6 8 10 12 14
1 3 5 7 9 11 13 15

ANALOG IN
ANALOG OUT
I2S/TDM IN
I2S/TDM OUT
S/PDIF IN
S/PDIF OUT

= NOT ACTIVE
= ACTIVE INPUT
= ACTIVE OUTPUT

J1
MCLK
1939

SW3
H1=MCLK
OUT
1939_BCLK

J8
LRCLK_IN
1939_LRCLK

J9
BCLK_IN
1939_BCLK

J4
SDATA_IN0
1939_DATA1

J5
SDATA_IN1
1939_DATA2

J6
SDATA_IN2
1974_DATA1

J7
SDATA_IN3
INTF_IN3

J10/12
LR/BCLK0

J11/13
LR/BCLK1

J3
MCLK

XTAL

AD1940 SERIAL OUT MAX MASTER:
CONNECT ALL JUMPER RS100-113

AD1940 SERIAL OUT SLAVE:
DISCONNECT ALL JUMPER RS100-113
S/PDIF IN/OUT MODE

ACTIVE CHANNELS:

ANALOG IN
0 2 4 6 8 10 12 14
1 3 5 7 9 11 13 15

ANALOG OUT

DIGITAL IN

DIGITAL OUT

S/PDIF IN

S/PDIF OUT

= NOT ACTIVE

= ACTIVE INPUT

= ACTIVE OUTPUT

J1  SW3  J8  J9  J4  J5  J6  J7  J10/12  J11/13  J3
MCLK  H1=MCLK  LRCLK_IN  BCLK_IN  SDATA_IN0  SDATA_IN1  SDATA_IN2  SDATA_IN3  LR/BCLK0  LR/BCLK1  MCLK
OUT  OUT  SPDIF_LRCLK  SPDIF_BCLK  1939_DATA1  1939_DATA2  1974_DATA1  SPDIF_RX_DATA

AD1940 SERIAL OUT MA: STER:
CONNECT ALL JUMPER RS J10-113

AD1940 SERIAL OUT SL: AVE
DISCONNECT ALL JUMPER RS J10-113
I2S/TDM IN/OUT MODE
(AD1939 X TAL GENERATES MCLK)

ACTIVE CHANNELS:

- NOT ACTIVE
- ACTIVE INPUT
- ACTIVE OUTPUT

Analog in
Analog out
Digital in
Digital out
S/PDIF in
S/PDIF out

J1  MCLK  SW3  J8  J9  J4  J5  J6  J7  J10/12  J11/13  J3  MCLK
H1=MCLK  LRCLK_IN  BCLK_IN  SDATA_IN0  SDATA_IN1  SDATA_IN2  SDATA_IN3  LR/BCLK0  LR/BCLK1  EXT

AD1940 SERIAL OUT MASTER: CONNECT ALL JUMPER RS J10-J13
AD1940 SERIAL OUT SLAVE: DISCONNECT ALL JUMPER RS J10-J13
I2S/TDM IN/OUT MODE
(EXTERNAL MCLK INPUT ON H1)

ACTIVE CHANNELS:

- NOT ACTIVE
- ACTIVE INPUT
- ACTIVE OUTPUT

<table>
<thead>
<tr>
<th>ANALOG IN</th>
<th>ANALOG OUT</th>
<th>DIGITAL IN</th>
<th>DIGITAL OUT</th>
<th>S/PDIF IN</th>
<th>S/PDIF OUT</th>
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J1: MCLK
H1=MCLK OUT
1939, H1 (OUT)

J8: LRCCLK_IN
BCLK_IN
1939_LRCCLK
1939_BCLK

J9: SDATA_IN0
SDATA_IN1
SDATA_IN2
SDATA_IN3

J4: INTF_IN0
INTF_IN1
INTF_IN2
INTF_IN3

J5: LR/BCLK0
LR/BCLK1

J6: INTF_OUT

J7: XTAL1939_LRCLK

J10/12: AD1940 SERIAL OUT MASTER
CONNECT ALL JUMPER RS J10-13

J11/13: AD1940 SERIAL OUT SL SLAVE
DISCONNECT ALL JUMPER RS J10-13

J3: MCLK XTAL

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EVAL-AD1940AZ Preliminary Technical Data
POWER SUPPLIES AND RESET

5 to 6 Volts, >700mA

3.3V Digital Supply

Linear Regulators

3.3V Analog Supply

Reset Generator

Master Reset Switch

Reset Threshold = 3.08V

R13 604r

R14 604r

1 A 2K

D2 RED

D3 GREEN

KA

D4 TP48

VIN+

L5 2 1

J14 3

Coax Power Jack

IN

OUT

GND

4 OUT

U5 ADP3339-3.3V

C47 1.0uF

C48 1.0uF

TP49 TP50

3 IN

2 OUT

1 GND

4 OUT

U6 ADP3339-3.3V

C49 1.0uF

C50 1.0uF

TP51 TP52

Reset Generator

SW2

R15 4 VCC 3MR

1 GND 2 RESET

U17 ADM811TARTZ

C179 100uF 16V

A3V3 D3V3

Figure 20. Power Supplies and Reset Schematics
AD1939 CODEC

AD1939 DAC Serial Port:
- AD1939 DACs are always Slaves
- Set AD1940 Serial Output 0 to Master
- AD1940 Output Channels 0-7 in I2S Mode

AD1939 ADC Serial Port:
- AD1939 ADCs are always Master
- AD1940 Input is always Slave
- AD1940 Input Channels 0-3 in I2S Mode

To use DACs and Digital output header 2 simultaneously,
set AD1940 outputs to slave and external device as LRCLK/BCLK master

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Figure 21: AD1939 Codec Schematics
AD1974 ADC

Figure 22. AD1974 ADC Schematics
Figure 23. Analog Audio Input Filters Schematics
Figure 24. Analog Audio Output Filters (1) Schematics
Figure 25. Analog Audio Output Filters (2) Schematics
DIGITAL AUDIO I/O

AD1940 Input is Slave by Default
Set external source to LRCLK/BCLK Master
AD1940 Input Channels 0-7 in I2S Mode
Dual Wire 8-Channel TDM: Ch 0-7 on SDATA_IN3, Ch 8-15 on SDATA_IN2
Single Wire 16-Channel TDM: Ch 0-15 on SDATA_IN3

AD1940 Output 0 can be Master or Slave
AD1940 Output Channels 0-7 in I2S Mode
Dual Wire 8-Channel TDM: Ch 0-7 on SDATA_OUT0
Single Wire 16-Channel TDM: Ch 0-15 on SDATA_OUT0

Figure 26. Digital Audio I/O Schematics
S/PDIF INTERFACE

S/PDIF Rx Serial Port:
CS8416 is Master by Default
AD1940 Input is Slave by Default
AD1940 Input Channels 6-7 in I2S Mode

S/PDIF Input Selection

S/PDIF Transmitter
CS8406 is Slave by Default
Set AD1940 Serial Output 1 to Master
AD1940 Output Channels 8-9 in I2S Mode

Figure 27. S/PDIF Interface Schematics
Figure 28. Audio Data and Clock Routing Schematics
BOARD SILKSCREEN AND PARTS PLACEMENT

Figure 29. Board Top Layer Layout
# BILL OF MATERIALS

<table>
<thead>
<tr>
<th>Reference</th>
<th>Qty</th>
<th>Value</th>
<th>Manufacturer</th>
<th>Part Number</th>
<th>Description</th>
<th>Vendor</th>
<th>Vendor Order #</th>
</tr>
</thead>
<tbody>
<tr>
<td>C105 C112 C119 C126 C133 C140 C147 C154</td>
<td>8</td>
<td>220pF</td>
<td>Murata ENA</td>
<td>GRM15555C1H221J A01D</td>
<td>Multilayer Ceramic 50V NPO (0402)</td>
<td>Digi-Key</td>
<td>490-1293-1-ND</td>
</tr>
<tr>
<td>C107 C114 C121 C128 C135 C142 C149 C156</td>
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<td>2.2nF</td>
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<td>2-pin Header Unshrouded Jumper 0.10*; use Shunt Tyco 881545-2</td>
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<td>3-pos SIP Header</td>
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**ORDERING GUIDE**

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<th>Model</th>
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**ESD CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

![ESD Sensitive Device Warning](image-url)