AD9643/AD6649 ENG (SOCKET)

DUT

EXTRA CIRCUITRY FOR AD9258 COMPATIBILITY
NOT NEEDED FOR AD9643/AD6649

SYNC

PDWN

OEN

LAYOUT: DECOUPLING QUANTITY MAY VARY LAYOUT DEPENDING

AD9643/AD6649 ENG (SOCKET)
ANALOG INPUT

THIS SECTION WILL CHANGE BASED ON 9644 EXPERIMENTS

PASSIVE PATH A

LAYOUT: SMA'S SHOULD BE 540 MILS CENTER TO CENTER

NOTE: CUTS REQ'D FOR 2ND TRANSF USE

PASSIVE PATH B

LAYOUT: SMA'S SHOULD BE 540 MILS CENTER TO CENTER
ACTIVE CLOCK PATH

PASSIVE CLOCK

KP ICELL

LAYOUT: SMD'S SHOULD BE 540 MILS CENTER TO CENTER
LAYOUT: SHARE PADS WITH ACTIVE CLOCK PATH S'S

SHEET 5 OF 4
LAYOUT: PLACE C705 NEAR DUT

NOTE: THIS SYMBOL IS DRAWN GIVEN INPUT 1 LOGIC

SPI & FPGA CONN.

LAYOUT: ROUTE ALL TRACES TO THE TYCO CONN ON TOP OF BOARD

USING FIFO5