HMC797

GaAs PHEMT MMIC
1 WATT POWER AMPLIFIER, DC - 22 GHz

Typical Applications
The HMC797 is ideal for:
• Test Instrumentation
• Microwave Radio & VSAT
• Military & Space
• Telecom Infrastructure
• Fiber Optics

Features
High P1dB Output Power: +28 dBm
High Psat Output Power: +31 dBm
High Gain: 14.5 dB
High Output IP3: +40 dBm
Supply Voltage: +10 V @ 400 mA
50 Ohm Matched Input/Output
Die Size: 2.89 x 1.55 x 0.1 mm

General Description
The HMC797 is a GaAs MMIC PHEMT Distributed Power Amplifier die which operates between DC and 22 GHz. The amplifier provides 14.5 dB of gain, 40 dBm output IP3 and +28 dBm of output power at 1 dB gain compression while requiring 400mA from a +10V supply. This versatile PA exhibits a positive gain slope from 3 to 21 GHz making it ideal for EW, ECM, Radar and test equipment applications. The HMC797 amplifier I/Os are internally matched to 50 Ohms facilitating integration into Multi-Chip-Modules (MCMs). All data is taken with the chip connected via two 0.025mm (1 mil) wire bonds of minimal length 0.31 mm (12 mils).

Electrical Specifications, \( T_A = +25^\circ C, Vdd = +10V, Vgg2 = +3.5V, Idd = 400 \, mA * \)

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</thead>
<tbody>
<tr>
<td>Frequency Range</td>
<td>DC - 10</td>
<td>10 - 18</td>
<td>18 - 22</td>
<td>GHz</td>
<td></td>
<td></td>
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<tr>
<td>Gain</td>
<td>13.5</td>
<td>14.5</td>
<td>15.5</td>
<td>dB</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Gain Flatness</td>
<td>±0.5</td>
<td>±0.7</td>
<td>±0.4</td>
<td>dB</td>
<td></td>
<td></td>
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<tr>
<td>Gain Variation Over Temperature</td>
<td>0.009</td>
<td>0.01</td>
<td>0.012</td>
<td>dB/ °C</td>
<td></td>
<td></td>
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<tr>
<td>Input Return Loss</td>
<td>16</td>
<td>17</td>
<td>18</td>
<td>dB</td>
<td></td>
<td></td>
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<td>Output Return Loss</td>
<td>16</td>
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<td>18</td>
<td>dB</td>
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<tr>
<td>Output Power for 1 dB Compression (P1dB)</td>
<td>27</td>
<td>28.5</td>
<td>27</td>
<td>28.5</td>
<td>26.5</td>
<td>28</td>
<td>dBm</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Saturated Output Power (Psat)</td>
<td>31</td>
<td>31</td>
<td>31</td>
<td>dBm</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Output Third Order Intercept (IP3)</td>
<td>41</td>
<td>40</td>
<td>39</td>
<td>dBm</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Noise Figure</td>
<td>3.5</td>
<td>3</td>
<td>3.5</td>
<td>dB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply Current (Idd) (Vdd= 10V, Vgg1= -0.8V Typ.)</td>
<td>400</td>
<td>400</td>
<td>400</td>
<td>mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tbody>
</table>

* Adjust Vgg1 between -2 to 0V to achieve Idd = 400 mA typical.
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Gain & Return Loss

Gain vs. Temperature

Input Return Loss vs. Temperature

Output Return Loss vs. Temperature

Reverse Isolation vs. Temperature

Noise Figure vs. Frequency

For price, delivery, and to place orders: Hittite Microwave Corporation, 2 Elizabeth Drive, Chelmsford, MA 01824
Phone: 978-250-3343     Fax: 978-250-3373     Order On-line at www.hittite.com
Application Support: Phone: 978-250-3343  or  apps@hittite.com

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P1dB vs. Temperature

Psat vs. Temperature

P1dB vs. Vdd

Psat vs. Vdd

Output IP3 vs.
Temperature @ Pout = 18 dBm Tone

Output IP3 vs. Output Power @ 10 GHz
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**Power Compression @ 2 GHz**

**Power Compression @ 10 GHz**

**Power Compression @ 22 GHz**

**Power Dissipation**

**Second Harmonics vs. Temperature @ Pout = 18 dBm**

**Second Harmonics vs. Vdd @ Pout = 18 dBm**
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Second Harmonics vs. $I_{dd} @ P_{out} = 18$ dBm

Absolute Maximum Ratings

- **Drain Bias Voltage (Vdd)**: +12 Vdc
- **Gate Bias Voltage (Vgg1)**: -3 to 0 Vdc
- **Gate Bias Voltage (Vgg2)**: $V_{gg2} = (V_{dd} - 6.5V)$ to 4.5V. For $V_{dd} < 8.5V$, $V_{gg2}$ must remain >2V
- **RF Input Power (RFIN)**: +27 dBm
- **Channel Temperature**: 150 °C
- **Continuous $P_{diss}$ (T= 85 °C)**: 4.5 W
- **Thermal Resistance (channel to die bottom)**: 14.5 °C/W
- **Output Power into VSWR >7:1**: 29 dBm
- **Storage Temperature**: -65 to 150°C
- **Operating Temperature**: -55 to 85 °C

Second Harmonics vs. $P_{out}$

Typical Supply Current vs. $V_{dd}$

<table>
<thead>
<tr>
<th>$V_{dd}$ (V)</th>
<th>$I_{dd}$ (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>+9</td>
<td>400</td>
</tr>
<tr>
<td>+10</td>
<td>400</td>
</tr>
<tr>
<td>+11</td>
<td>400</td>
</tr>
</tbody>
</table>

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

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Outline Drawing

This die utilizes fragile air bridges. Any pick-up tools used must not contact the die in the cross hatched area.

Die Packaging Information [1]

<table>
<thead>
<tr>
<th>Standard</th>
<th>Alternate</th>
</tr>
</thead>
<tbody>
<tr>
<td>WP-19 (Waffle Pack)</td>
<td>[2]</td>
</tr>
</tbody>
</table>

[1] Refer to the “Packaging Information” section on our website for die packaging dimensions.


NOTES:
1. ALL DIMENSIONS ARE IN INCHES [MM]
2. DIE THICKNESS IS .004”
3. TYPICAL BOND PAD IS .004” SQUARE
4. BOND PAD METALIZATION: GOLD
5. BACKSIDE METALIZATION: GOLD
6. BACKSIDE METAL IS GROUND
7. NO CONNECTION REQUIRED FOR UNLABELED BOND PADS
8. OVERALL DIE SIZE ±.002”
# Pad Descriptions

<table>
<thead>
<tr>
<th>Pad Number</th>
<th>Function</th>
<th>Description</th>
<th>Interface Schematic</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>RFIN</td>
<td>This pad is DC coupled and matched to 50 Ohms. Blocking capacitor is required.</td>
<td><img src="image1" alt="RFIN Interface Schematic" /></td>
</tr>
<tr>
<td>2</td>
<td>VGG2</td>
<td>Gate control 2 for amplifier. Attach bypass capacitors per application circuit herein. For nominal operation +3.5V should be applied to Vgg2.</td>
<td><img src="image2" alt="VGG2 Interface Schematic" /></td>
</tr>
<tr>
<td>4, 7</td>
<td>ACG2, ACG4</td>
<td>Low frequency termination. Attach bypass capacitors per application circuit herein.</td>
<td><img src="image3" alt="ACG2 Interface Schematic" /></td>
</tr>
<tr>
<td>3</td>
<td>ACG1</td>
<td>Low frequency termination. Attach bypass capacitors per application circuit herein.</td>
<td><img src="image4" alt="ACG1 Interface Schematic" /></td>
</tr>
<tr>
<td>5</td>
<td>RFOUT &amp; VDD</td>
<td>RF output for amplifier. Connect DC bias (Vdd) network to provide drain current (Idd). See application circuit herein.</td>
<td><img src="image5" alt="RFOUT &amp; VDD Interface Schematic" /></td>
</tr>
<tr>
<td>6</td>
<td>ACG3</td>
<td>Low frequency termination. Attach bypass capacitor per application circuit herein.</td>
<td><img src="image6" alt="ACG3 Interface Schematic" /></td>
</tr>
<tr>
<td>8</td>
<td>VGG1</td>
<td>Gate control 1 for amplifier. Attach bypass capacitor per application circuit herein. Please follow “MMIC Amplifier Biasing Procedure” application note.</td>
<td><img src="image7" alt="VGG1 Interface Schematic" /></td>
</tr>
<tr>
<td>Die Bottom</td>
<td>GND</td>
<td>Die bottom must be connected to RF/DC ground.</td>
<td><img src="image8" alt="GND Interface Schematic" /></td>
</tr>
</tbody>
</table>
Assembly Diagram

NOTE 1: Drain Bias (Vdd) must be applied through a broadband bias tee with low series resistance and capable of providing 500mA.
Mounting & Bonding Techniques for Millimeterwave GaAs MMICs

The die should be attached directly to the ground plane eutectically or with conductive epoxy (see HMC general Handling, Mounting, Bonding Note). 50 Ohm Microstrip transmission lines on 0.127mm (5 mil) thick alumina thin film substrates are recommended for bringing RF to and from the chip (Figure 1). If 0.254mm (10 mil) thick alumina thin film substrates must be used, the die should be raised 0.150mm (6 mils) so that the surface of the die is coplanar with the surface of the substrate. One way to accomplish this is to attach the 0.102mm (4 mil) thick die to a 0.150mm (6 mil) thick molybdenum heat spreader (moly-tab) which is then attached to the ground plane (Figure 2).

Microstrip substrates should be placed as close to the die as possible in order to minimize bond wire length. Typical die-to-substrate spacing is 0.076mm to 0.152 mm (3 to 6 mils).

Handling Precautions

Follow these precautions to avoid permanent damage.

Storage: All bare die are placed in either Waffle or Gel based ESD protective containers, and then sealed in an ESD protective bag for shipment. Once the sealed ESD protective bag has been opened, all die should be stored in a dry nitrogen environment.

Cleanliness: Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.

Static Sensitivity: Follow ESD precautions to protect against ESD strikes.

Transients: Suppress instrument and bias supply transients while bias is applied. Use shielded signal and bias cables to minimize inductive pick-up.

General Handling: Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers. The surface of the chip may have fragile air bridges and should not be touched with vacuum collet, tweezers, or fingers.

Mounting

The die should be attached directly to the ground plane coplanarly. The mounting surface should be clean and flat.

Eutectic Die Attach: A 80/20 gold tin preform is recommended with a work surface temperature of 255 °C and a tool temperature of 265 °C. When hot 90/10 nitrogen/hydrogen gas is applied, tool tip temperature should be 290 °C. DO NOT expose the chip to a temperature greater than 320 °C for more than 20 seconds. No more than 3 seconds of scrubbing should be required for attachment.

Epoxide Die Attach: Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip once it is placed into position. Cure epoxy per the manufacturer’s schedule.

Wire Bonding

RF bonds made with two 1 mil wires are recommended. These bonds should be thermosonically bonded with a force of 40-60 grams. DC bonds of 0.001" (0.025 mm) diameter, thermosonically bonded, are recommended. Ball bonds should be made with a force of 40-50 grams and wedge bonds at 18-22 grams. All bonds should be made with a nominal stage temperature of 150 °C. A minimum amount of ultrasonic energy should be applied to achieve reliable bonds. All bonds should be as short as possible, less than 12 mils (0.31 mm).
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Notes: