FEATURES
High Slew Rate: 10 V/μs Min
Fast Settling Time: 0.9 μs to 0.1% Type
Low Input Offset Voltage Drift: 10 μV/°C Max
Wide Bandwidth: 3.5 MHz Min
Temperature-Compensated Input Bias Currents
Guaranteed Input Bias Current: 18 nA Max (125°C)
Bias Current Specified Warmed Up over Temperature
Low Input Noise Current: 0.01 pA/√Hz Type
High Common-Mode Rejection Ratio 86 dB Min
Pin Compatible with Standard Dual Pinouts
Models with MIL-STD-883 Class B Processing Available

GENERAL DESCRIPTION
The OP215 offers the proven JFET-input performance advantages of high speed and low input bias current with the tracking and convenience advantages of a dual op amp configuration.

Low input offset voltages, low input currents, and low drift are featured in these high-speed amplifiers.

On-chip zener-zap trimming is used to achieve low V_{OS}, while a bias-current compensation scheme gives a low input bias current at elevated temperature. Thus, the OP215 features an input bias current of 1.4 nA at 70°C ambient (not junction) temperature which greatly extends the application usefulness of this device.

Applications include high-speed amplifiers for current output DACs, active filters, sample-and-hold buffers, and photocell amplifiers. For additional precision JFET op amps, see the OP249 and AD712 data sheets.

Figure 1. Simplified Schematic (1/2 OP215)
COMPARABLE PARTS
View a parametric search of comparable parts.

DOCUMENTATION
Application Notes
• AN-113: Precision Ramp Generator
Data Sheet
• OP215: Dual Precision JFET-Input Operational Amplifier Data Sheet
• OP215: Military Data Sheet

TOOLS AND SIMULATIONS
• OP215 SPICE Macro Models

DESIGN RESOURCES
• OP215 Material Declaration
• PCN-PDN Information
• Quality And Reliability
• Symbols and Footprints

DISCUSSIONS
View all OP215 EngineerZone Discussions.

SAMPLE AND BUY
Visit the product page to see pricing options.

TECHNICAL SUPPORT
Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK
Submit feedback for this data sheet.
## OP215—SPECIFICATIONS

### ELECTRICAL CHARACTERISTICS  
(at $V_S = \pm 15$ V, $T_A = 25^\circ$C, unless otherwise noted.)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>OP215E Min</th>
<th>Type</th>
<th>Max</th>
<th>OP215G Min</th>
<th>Type</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Offset Voltage</td>
<td>$V_{OS}$</td>
<td>$R_S = 50$ $\Omega$, 'G' Grade</td>
<td>0.2</td>
<td>1.0</td>
<td></td>
<td>2.0</td>
<td>4.0</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Input Offset Current(^1)</td>
<td>$I_{OS}$</td>
<td>$T_j = 25^\circ$C, Device Operating</td>
<td>3</td>
<td>50</td>
<td></td>
<td>3</td>
<td>100</td>
<td></td>
<td>pA</td>
</tr>
<tr>
<td>Input Bias Current(^1)</td>
<td>$I_B$</td>
<td>$T_j = 25^\circ$C, Device Operating</td>
<td>$\pm 15$</td>
<td>$\pm 100$</td>
<td></td>
<td>$\pm 15$</td>
<td>$\pm 300$</td>
<td></td>
<td>pA</td>
</tr>
<tr>
<td>Input Resistance</td>
<td>$R_{IN}$</td>
<td></td>
<td>$10^{1,2}$</td>
<td></td>
<td></td>
<td>$10^{1,2}$</td>
<td></td>
<td></td>
<td>$\Omega$</td>
</tr>
<tr>
<td>Large-Signal Voltage Gain</td>
<td>$A_{VO}$</td>
<td>$R_L \geq 2$ $k\Omega$, $V_{O} = \pm 10$ $V$</td>
<td>150</td>
<td>500</td>
<td></td>
<td>50</td>
<td>200</td>
<td></td>
<td>V/mV</td>
</tr>
<tr>
<td>Output Voltage Swing</td>
<td>$V_O$</td>
<td>$R_L = 10$ $k\Omega$, $R_L = 2$ $k\Omega$</td>
<td>$\pm 12$</td>
<td>$\pm 13$</td>
<td></td>
<td>$\pm 12$</td>
<td>$\pm 13$</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Supply Current</td>
<td>$I_{SY}$</td>
<td>'G' Grade</td>
<td>6.0</td>
<td>8.5</td>
<td></td>
<td>7.0</td>
<td>10.0</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Slew Rate</td>
<td>$SR$</td>
<td>$A_{VCL} = 1$</td>
<td>10</td>
<td>18</td>
<td></td>
<td>5</td>
<td>15</td>
<td></td>
<td>V/$\mu$s</td>
</tr>
<tr>
<td>Gain Bandwidth Product(^3)</td>
<td>GBW</td>
<td></td>
<td>3.5</td>
<td>5.7</td>
<td></td>
<td>3.0</td>
<td>5.4</td>
<td></td>
<td>$MHz$</td>
</tr>
<tr>
<td>Closed-Loop Bandwidth</td>
<td>CLBW</td>
<td>$A_{VCL} = 1$</td>
<td>13</td>
<td>12</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$MHz$</td>
</tr>
<tr>
<td>Setting Time</td>
<td>$t_S$</td>
<td>To 0.01%</td>
<td>2.3</td>
<td>1.1</td>
<td>0.9</td>
<td>2.4</td>
<td>1.2</td>
<td>1.0</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>Input Voltage Range</td>
<td>IVR</td>
<td></td>
<td>10.2</td>
<td>14.8</td>
<td>$-10.2$</td>
<td>$-11.5$</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Common-Mode Rejection Ratio</td>
<td>CMRR</td>
<td>$V_{CM} = \pm IVR$</td>
<td>82</td>
<td>100</td>
<td></td>
<td>80</td>
<td>96</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Power Supply Rejection Ratio</td>
<td>PSRR</td>
<td>$V_S = \pm 10$ $V$ to $\pm 16$ $V$, $V_S = \pm 10$ $V$ to $\pm 15$ $V$</td>
<td>10</td>
<td>51</td>
<td></td>
<td>16</td>
<td>100</td>
<td></td>
<td>$\mu V/V$</td>
</tr>
<tr>
<td>Input Noise Voltage Density</td>
<td>$\theta_n$</td>
<td>$f_0 = 100$ $Hz$, $f_0 = 1,000$ $Hz$</td>
<td>20</td>
<td>15</td>
<td></td>
<td>20</td>
<td>15</td>
<td></td>
<td>nV/$\sqrt{Hz}$</td>
</tr>
<tr>
<td>Input Noise Current Density</td>
<td>$I_n$</td>
<td>$f_0 = 100$ $Hz$, $f_0 = 1,000$ $Hz$</td>
<td>0.01</td>
<td>0.01</td>
<td></td>
<td>0.01</td>
<td>0.01</td>
<td></td>
<td>pA/$\sqrt{Hz}$</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>$C_{IN}$</td>
<td></td>
<td>3</td>
<td>3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>pF</td>
</tr>
</tbody>
</table>

### NOTES

\(^1\)Input bias current is specified for two different conditions. The $T_j = 25^\circ$C specification is with the junction at ambient temperature; the device operating specification is with the device operating in a warmed up condition at 25$^\circ$C ambient. The warmed up bias-current value is correlated to the junction temperature value via the curves of $I_S$ versus $T_j$ and $I_S$ versus $T_A$. PMI has a bias-current compensation circuit that gives improved bias current and bias current over temperature versus standard JFET input op amps. $I_S$ and $I_{OS}$ are measured at $V_{CM} = 0$.

\(^2\)Setting time is defined here for a unity gain inverter connection using 2 $k\Omega$ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within a specified percent of its final value from the time a 10 $V$ step input is applied to the inverter. See setting time test circuit.

\(^3\)Sample tested.

Specifications are subject to change without notice.
## SPECIFICATIONS

### ELECTRICAL CHARACTERISTICS

(at \( V_S = \pm 15 \text{ V}, 0^\circ \text{C} \leq T_A \leq 70^\circ \text{C} \) for E Grade, \(-40^\circ \text{C} \leq T_A \leq +85^\circ \text{C} \) for G Grade, unless otherwise noted.)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>OP215E</th>
<th>OP215G</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min</td>
<td>Type</td>
</tr>
<tr>
<td>Input Offset Voltage</td>
<td>( V_{OS} )</td>
<td>( R_S = 50 \Omega )</td>
<td>0.4</td>
<td>1.65</td>
</tr>
<tr>
<td>Average Input Offset Voltage Drift Without External Trim</td>
<td>( TCVOS )</td>
<td>( R_P = 100 , \text{k\Omega} )</td>
<td>3</td>
<td>15</td>
</tr>
<tr>
<td>Average Input Offset Voltage Drift With External Trim</td>
<td>( TCVOSn )</td>
<td>( R_P = 100 , \text{k\Omega} )</td>
<td>0.06</td>
<td>0.45</td>
</tr>
<tr>
<td>Input Offset Current(^2)</td>
<td>( I_{OS} )</td>
<td>( T_j = 70^\circ \text{C} )</td>
<td>±0.12</td>
<td>±0.70</td>
</tr>
<tr>
<td>Input Bias Current(^2)</td>
<td>( I_S )</td>
<td>( T_j = 25^\circ \text{C} )</td>
<td>±0.12</td>
<td>±0.70</td>
</tr>
<tr>
<td>Input Voltage Range</td>
<td>IVR</td>
<td>( V_{CM} = \pm \text{IVR} )</td>
<td>10.2</td>
<td>14.7</td>
</tr>
<tr>
<td>Common-Mode Rejection Ratio</td>
<td>CMRR</td>
<td>( V_{CM} = \pm \text{IVR} )</td>
<td>80</td>
<td>98</td>
</tr>
<tr>
<td>Power Supply Rejection Ratio</td>
<td>PSRR</td>
<td>( V_S = \pm 10 \text{ V} ) to ( \pm 16 \text{ V} )</td>
<td>13</td>
<td>100</td>
</tr>
<tr>
<td>Large-Signal Voltage Gain</td>
<td>( A_{VO} )</td>
<td>( R_L \geq 2 , \text{k\Omega} )</td>
<td>50</td>
<td>180</td>
</tr>
<tr>
<td>Output Voltage Swing</td>
<td>( V_O )</td>
<td>( R_L \geq 10 , \text{k\Omega} )</td>
<td>±12</td>
<td>±13</td>
</tr>
</tbody>
</table>

**NOTES**

\(^1\)Sample tested.

\(^2\)Input bias current is specified for two different conditions. The \( T_j = 25^\circ \text{C} \) specification is with the junction at ambient temperature; the Device Operating specification is with the device operating in a warmed up condition at 25°C ambient. The warmed up bias-current value is correlated to the junction temperature value via the curves of \( I_S \) versus \( T_j \) and \( I_S \) versus \( T_A \). PMI has a bias-current compensation circuit that gives improved bias current and bias current over temperature versus standard JFET input op amps. \( I_S \) and \( I_{OS} \) are measured at \( V_{CM} = 0 \).

Specifications are subject to change without notice.
OP215

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- OP215E, OP215G: ±18 V

Operating Temperature Range
- OP215E: 0°C to +70°C
- OP215G: -40°C to +85°C

Maximum Junction Temperature (Tj): 150°C

Differential Input Voltage
- OP215E: ±40 V
- OP215G: ±30 V

Input Voltage
- OP215E: ±20 V
- OP215G: ±16 V

Output Short-Circuit Duration: Indefinite

Storage Temperature Range: -65°C to +150°C

Lead Temperature (Soldering, 60 sec): 300°C

Junction Temperature (Tj): -65°C to +150°C

NOTES
1. Absolute maximum ratings apply to packaged parts, unless otherwise noted.
2. Unless otherwise specified, the absolute maximum negative input voltage is equal to one volt more positive than the negative power supply voltage.

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Model</th>
<th>Package Type</th>
<th>Temperature Range</th>
<th>VOS Max (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OP215EZ2</td>
<td>8-Lead CerDIP</td>
<td>COM</td>
<td>1.0</td>
</tr>
<tr>
<td>OP215GP2</td>
<td>8-Lead Plastic DIP</td>
<td>XIND</td>
<td>6.0</td>
</tr>
</tbody>
</table>

For military processed devices, please refer to the standard microcircuit drawing (SMD) available at www.dscc.dla.mil/programs/milspec/default.asp

SMD Part Number | ADI Equivalent
---|---
5962-8853801GA2 | OP215AJMDA
5962-8853801PA | OP215AZMDA
5962-8838032A2 | OP215BRCMDA

NOTES
1. Burn-in is available on commercial and industrial temperature range parts in CerDIP and plastic DIP packages.

CAUTION
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP215 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

WARNING! ESD SENSITIVE DEVICE
Typical Performance Characteristics—OP215

TPC 1. Large-Signal Transient Response

TPC 2. Small-Signal Transient Response

TPC 3. Settling Time

TPC 4. Closed-Loop Bandwidth and Phase Shift vs. Frequency

TPC 5. Bandwidth vs. Temperature

TPC 6. Open-Loop Frequency Response

TPC 7. Maximum Output Swing vs. Frequency

TPC 8. Slew Rate vs. Temperature

TPC 9. Common-Mode Rejection Ratio vs. Frequency
BASIC CONNECTIONS

**Figure 2.** Settling Time Test Circuit

**Figure 3.** Slew Rate Test Circuit

**Figure 4.** Input Offset Voltage Nulling

**NOTE**

$V_{OS}$ CAN BE TRIMMED WITH POTENTIOMETERS RANGING FROM 10 kΩ TO 1 MΩ. FOR MOST UNITS $TCV_{OS}$ WILL BE MINIMUM WHEN $V_{OS}$ IS ADJUSTED WITH A 100 kΩ POTENTIOMETER.
APPLICATIONS INFORMATION
Dynamic Operating Considerations
As with most amplifiers, care should be taken with lead dress, component placement, and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground sets the frequency of the pole. In many instances, the frequency of this pole is much greater than the expected 3 dB frequency of the closed-loop gain and, consequently, there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than, or equal to, the original feedback pole time constant.

OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).

8-Lead CERDIP (Z-Suffix)

0.005 (0.13) MIN 0.055 (1.4) MAX
PIN 1 0.310 (7.87) 0.220 (5.59)
0.100 (2.54) BSC
0.320 (8.13) 0.290 (7.37)
0.200 (5.08) MAX 0.070 (1.78) MIN
0.014 (0.36) 0.030 (0.76)

8-Lead Plastic DIP (P-Suffix)

0.430 (10.92) 0.348 (8.84)
PIN 1 0.405 (10.29) MAX 0.022 (0.56) 0.070 (1.77)
0.210 (5.33) MAX 0.160 (4.06) MIN
0.014 (0.36) 0.030 (0.76) 0.008 (0.20)
## Revision History

<table>
<thead>
<tr>
<th>Location</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Sheet changed from REV. 0 to REV. A.</td>
<td>1</td>
</tr>
<tr>
<td>Edits to GENERAL DESCRIPTION</td>
<td>2, 3</td>
</tr>
<tr>
<td>Edits to ELECTRICAL CHARACTERISTICS</td>
<td>4</td>
</tr>
<tr>
<td>Edits to ORDERING INFORMATION</td>
<td>4</td>
</tr>
<tr>
<td>Edits to PIN CONNECTIONS</td>
<td>4</td>
</tr>
<tr>
<td>Edits to ABSOLUTE MAXIMUM RATINGS</td>
<td>4</td>
</tr>
<tr>
<td>Edits to PACKAGE TYPE</td>
<td>4</td>
</tr>
<tr>
<td>Deleted WAFER TEST LIMITS</td>
<td>4</td>
</tr>
<tr>
<td>Deleted DICE CHARACTERISTICS</td>
<td>4</td>
</tr>
<tr>
<td>Deleted TYPICAL ELECTRICAL CHARACTERISTICS</td>
<td>4</td>
</tr>
<tr>
<td>Edits to BURN-IN CIRCUIT figure</td>
<td>7</td>
</tr>
</tbody>
</table>