FEATURES

Dual symmetric 600 MHz high performance Blackfin cores
328K bytes of on-chip memory
(see Memory Architecture)
Each Blackfin core includes
  Two 16-bit MACs, two 40-bit ALUs, four 8-bit video ALUs,
  40-bit shifter
  RISC-like register and instruction model for ease of pro-
  grammation and compiler-friendly support
  Advanced debug, trace, and performance monitoring
Wide range of operating voltages, (see Operating
Conditions)
256-ball CSP_BGA (2 sizes) and 297-ball PBGA
package options

PERIPHERALS

Dual 12-channel DMA controllers
(supporting 24 peripheral DMAs)
2 memory-to-memory DMAs
2 internal memory-to-memory DMAs and 1 internal memory
DMA controller
12 general-purpose 32-bit timers/counters with PWM
capability
SPI-compatible port
UART with support for IrDA
Dual watchdog timers
Dual 32-bit core timers
48 programmable flags (GPIO)
On-chip phase-locked loop capable of 0.5× to 64× frequency
multiplication
2 parallel input/output peripheral interface units supporting
ITU-R 656 video and glueless interface to analog front end
ADCs
2 dual channel, full duplex synchronous serial ports support-
ing eight stereo I²S channels

Figure 1. Functional Block Diagram

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Rev. F

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# TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Features</td>
<td>1</td>
</tr>
<tr>
<td>Peripherals</td>
<td>1</td>
</tr>
<tr>
<td>Table of Contents</td>
<td>2</td>
</tr>
<tr>
<td>Revision History</td>
<td>2</td>
</tr>
<tr>
<td>General Description</td>
<td>3</td>
</tr>
<tr>
<td>Portable Low Power Architecture</td>
<td>3</td>
</tr>
<tr>
<td>Blackfin Processor Core</td>
<td>3</td>
</tr>
<tr>
<td>Memory Architecture</td>
<td>4</td>
</tr>
<tr>
<td>DMA Controllers</td>
<td>8</td>
</tr>
<tr>
<td>Watchdog Timer</td>
<td>8</td>
</tr>
<tr>
<td>Timers</td>
<td>9</td>
</tr>
<tr>
<td>Serial Ports (SPORTs)</td>
<td>9</td>
</tr>
<tr>
<td>Serial Peripheral Interface (SPI) Port</td>
<td>9</td>
</tr>
<tr>
<td>UART Port</td>
<td>10</td>
</tr>
<tr>
<td>Programmable Flags (PFx)</td>
<td>10</td>
</tr>
<tr>
<td>Parallel Peripheral Interface</td>
<td>10</td>
</tr>
<tr>
<td>Dynamic Power Management</td>
<td>11</td>
</tr>
<tr>
<td>Voltage Regulation</td>
<td>12</td>
</tr>
<tr>
<td>Clock Signals</td>
<td>13</td>
</tr>
<tr>
<td>Booting Modes</td>
<td>14</td>
</tr>
<tr>
<td>Instruction Set Description</td>
<td>14</td>
</tr>
<tr>
<td>Development Tools</td>
<td>15</td>
</tr>
<tr>
<td>Additional Information</td>
<td>16</td>
</tr>
<tr>
<td>Related Signal Chains</td>
<td>16</td>
</tr>
<tr>
<td>Pin Descriptions</td>
<td>17</td>
</tr>
<tr>
<td>Specifications</td>
<td>20</td>
</tr>
<tr>
<td>Operating Conditions</td>
<td>20</td>
</tr>
<tr>
<td>Electrical Characteristics</td>
<td>21</td>
</tr>
<tr>
<td>Absolute Maximum Ratings</td>
<td>22</td>
</tr>
<tr>
<td>ESD Sensitivity</td>
<td>22</td>
</tr>
<tr>
<td>Timing Specifications</td>
<td>23</td>
</tr>
<tr>
<td>Output Drive Currents</td>
<td>41</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>42</td>
</tr>
<tr>
<td>Test Conditions</td>
<td>42</td>
</tr>
<tr>
<td>Environmental Conditions</td>
<td>44</td>
</tr>
<tr>
<td>256-Ball CSP_BGA (17 mm) Ball Assignment</td>
<td>46</td>
</tr>
<tr>
<td>256-Ball CSP_BGA (12 mm) Ball Assignment</td>
<td>51</td>
</tr>
<tr>
<td>297-Ball PBGA Ball Assignment</td>
<td>56</td>
</tr>
<tr>
<td>Outline Dimensions</td>
<td>61</td>
</tr>
<tr>
<td>Surface-Mount Design</td>
<td>63</td>
</tr>
<tr>
<td>Ordering Guide</td>
<td>63</td>
</tr>
</tbody>
</table>

## REVISION HISTORY

7/23—Rev. E to Rev. F

Updated Development Tools.................................................. 15
Added Related Signal Chains.................................................. 16
Corrected footnote 2 of Table 9 in Operating Conditions.................... 20
Removed Package Information section.
Revised Serial Ports—Enable and Three-State .................. 33
Revised Figure 24 to match parameter names in Table 27 in Serial Peripheral Interface (SPI) Port—Slave Timing ...... 36
Added Timer Clock Timing.................................................. 39
Revised Timer Cycle Timing .................................................. 39
Added figure JTAG Port Reset Timing................................. 40
Removed obsoleted models from Ordering Guide............. 63
GENERAL DESCRIPTION

The ADSP-BF561 processor is a high performance member of the Blackfin® family of products targeting a variety of multimedia, industrial, and telecommunications applications. At the heart of this device are two independent Analog Devices Blackfin processors. These Blackfin processors combine a dual-MAC state-of-the-art signal processing engine, the advantage of clean, orthogonal RISC-like microprocessor instruction set, and single instruction, multiple data (SIMD) multimedia capabilities in a single instruction set architecture.

The ADSP-BF561 processor has 328K bytes of on-chip memory. Each Blackfin core includes:

- 16K bytes of instruction SRAM/cache
- 16K bytes of instruction SRAM
- 32K bytes of data SRAM/cache
- 32K bytes of data SRAM
- 4K bytes of scratchpad SRAM

Additional on-chip memory peripherals include:

- 128K bytes of low latency on-chip L2 SRAM
- Four-channel internal memory DMA controller
- External memory controller with glueless support for SDRAM, mobile SDRAM, SRAM, and flash.

PORTABLE LOW POWER ARCHITECTURE

Blackfin processors provide world-class power management and performance. Blackfin processors are designed in a low power and low voltage design methodology and feature dynamic power management, the ability to vary both the voltage and frequency of operation to significantly lower overall power consumption. Varying the voltage and frequency can result in a substantial reduction in power consumption, compared with just varying the frequency of operation. This translates into longer battery life for portable appliances.

BLACKFIN PROCESSOR CORE

As shown in Figure 2, each Blackfin core contains two multiplier/accumulators (MACs), two 40-bit ALUs, four video ALUs, and a single shifter. The computational units process 8-bit, 16-bit, or 32-bit data from the register file.

Each MAC performs a 16-bit by 16-bit multiply in every cycle, with accumulation to a 40-bit result, providing eight bits of extended precision. The ALUs perform a standard set of arithmetic and logical operations. With two ALUs capable of operating on 16-bit or 32-bit data, the flexibility of the computational units covers the signal processing requirements of a varied set of application needs.

Each of the two 32-bit input registers can be regarded as two 16-bit halves, so each ALU can accomplish very flexible single 16-bit arithmetic operations. By viewing the registers as pairs of 16-bit operands, dual 16-bit or single 32-bit operations can be accomplished in a single cycle. By further taking advantage of the second ALU, quad 16-bit operations can be accomplished simply, accelerating the per cycle throughput.

The powerful 40-bit shifter has extensive capabilities for performing shifting, rotating, normalization, extraction, and depositing of data. The data for the computational units is found in a multiported register file of sixteen 16-bit entries or eight 32-bit entries.

A powerful program sequencer controls the flow of instruction execution, including instruction alignment and decoding. The sequencer supports conditional jumps and subroutine calls, as well as zero overhead looping. A loop buffer stores instructions locally, eliminating instruction memory accesses for tight looped code.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches from memory. The DAGs share a register file containing four sets of 32-bit Index, Modify, Length, and Base registers. Eight additional 32-bit registers provide pointers for general indexing of variables and stack locations.

Blackfin processors support a modified Harvard architecture in combination with a hierarchical memory structure. Level 1 (L1) memories are those that typically operate at the full processor speed with little or no latency. Level 2 (L2) memories are other memories, on-chip or off-chip, that may take multiple processor cycles to access. At the L1 level, the instruction memory holds instructions only. The two data memories hold data, and a dedicated scratchpad data memory stores stack and local variable information. At the L2 level, there is a single unified memory space, holding both instructions and data.

In addition, half of L1 instruction memory and half of L1 data memory may be configured as either Static RAMs (SRAMs) or caches. The Memory Management Unit (MMU) provides memory protection for individual tasks that may be operating on the core and may protect system registers from unintended access.

The architecture provides three modes of operation: user mode, supervisor mode, and emulation mode. User mode has restricted access to certain system resources, thus providing a protected software environment, while supervisor mode has unrestricted access to the system and core resources.

The Blackfin instruction set has been optimized so that 16-bit op-codes represent the most frequently used instructions, resulting in excellent compiled code density. Complex DSP instructions are encoded into 32-bit op-codes, representing fully featured multifunction instructions. Blackfin processors support a limited multi-issue capability, where a 32-bit instruction can be issued in parallel with two 16-bit instructions, allowing the programmer to use many of the core resources in a single instruction cycle.

The Blackfin assembly language uses an algebraic syntax for ease of coding and readability. The architecture has been optimized for use in conjunction with the VisualDSP C/C++ compiler, resulting in fast and efficient software implementations.
MEMORY ARCHITECTURE

The ADSP-BF561 views memory as a single unified 4G byte address space, using 32-bit addresses. All resources including internal memory, external memory, and I/O control registers occupy separate sections of this common address space. The memory portions of this address space are arranged in a hierarchical structure to provide a good cost/performance balance of some very fast, low latency memory as cache or SRAM very close to the processor, and larger, lower cost and performance memory systems farther away from the processor. The ADSP-BF561 memory map is shown in Figure 3.

The L1 memory system in each core is the highest performance memory available to each Blackfin core. The L2 memory provides additional capacity with lower performance. Lastly, the off-chip memory system, accessed through the External Bus Interface Unit (EBIU), provides expansion with SDRAM, flash memory, and SRAM, optionally accessing more than 768M bytes of physical memory. The memory DMA controllers provide high bandwidth data movement capability. They can perform block transfers of code or data between the internal L1/L2 memories and the external memory spaces.

Internal (On-Chip) Memory

The ADSP-BF561 has four blocks of on-chip memory providing high bandwidth access to the core.

The first is the L1 instruction memory of each Blackfin core consisting of 16K bytes of four-way set-associative cache memory and 16K bytes of SRAM. The cache memory may also be configured as an SRAM. This memory is accessed at full processor speed. When configured as SRAM, each of the two 16K banks of memory is broken into 4K sub-banks which can be independently accessed by the processor and DMA.

The second on-chip memory block is the L1 data memory of each Blackfin core which consists of four banks of 16K bytes each. Two of the L1 data memory banks can be configured as one way of a two-way set-associative cache or as an SRAM. The other two banks are configured as SRAM. All banks are accessed at full processor speed. When configured as SRAM, each of the four 16K banks of memory is broken into 4K sub-banks which can be independently accessed by the processor and DMA.

The third memory block associated with each core is a 4K byte scratchpad SRAM which runs at the same speed as the L1 memories, but is only accessible as data SRAM (it cannot be configured as cache memory and is not accessible via DMA).
The fourth on-chip memory system is the L2 SRAM memory array which provides 128K bytes of high speed SRAM operating at one half the frequency of the core, and slightly longer latency than the L1 memory banks. The L2 memory is a unified instruction and data memory and can hold any mixture of code and data required by the system design. The Blackfin cores share a dedicated low latency 64-bit wide data path port into the L2 SRAM memory.

Each Blackfin core processor has its own set of core Memory Mapped Registers (MMRs) but share the same system MMR registers and 128K bytes L2 SRAM memory.

**External (Off-Chip) Memory**

The ADSP-BF561 external memory is accessed via the External Bus Interface Unit (EBIU). This interface provides a glueless connection to up to four banks of synchronous DRAM (SDRAM) as well as up to four banks of asynchronous memory devices, including flash, EPROM, ROM, SRAM, and memory mapped I/O devices.

The PC133-compliant SDRAM controller can be programmed to interface to up to four banks of SDRAM, with each bank containing between 16M bytes and 128M bytes providing access to up to 512M bytes of SDRAM. Each bank is independently programmable and is contiguous with adjacent banks regardless of the sizes of the different banks or their placement. This allows...
ADSP-BF561

flexible configuration and upgradability of system memory while allowing the core to view all SDRAM as a single, contiguous, physical address space.

The asynchronous memory controller can also be programmed to control up to four banks of devices with very flexible timing parameters for a wide variety of devices. Each bank occupies a 64M byte segment regardless of the size of the devices used so that these banks will only be contiguous if fully populated with 64M bytes of memory.

**I/O Memory Space**

Blackfin processors do not define a separate I/O space. All resources are mapped through the flat 32-bit address space. On-chip I/O devices have their control registers mapped into memory mapped registers (MMRs) at addresses near the top of the 4G byte address space. These are separated into two smaller blocks, one which contains the control MMRs for all core functions, and the other which contains the registers needed for setup and control of the on-chip peripherals outside of the core. The core MMRs are accessible only by the core and only in supervisor mode and appear as reserved space by on-chip peripherals. The system MMRs are accessible by the core in supervisor mode and can be mapped as either visible or reserved to other devices, depending on the system protection model desired.

**Booting**

The ADSP-BF561 contains a small boot kernel, which configures the appropriate peripheral for booting. If the ADSP-BF561 is configured to boot from boot ROM memory space, the processor starts executing from the on-chip boot ROM.

**Event Handling**

The event controller on the ADSP-BF561 handles all asynchronous and synchronous events to the processor. The ADSP-BF561 provides event handling that supports both nesting and prioritization. Nesting allows multiple event service routines to be active simultaneously. Prioritization ensures that servicing of a higher priority event takes precedence over servicing of a lower priority event. The controller provides support for five different types of events:

- **Emulation** – An emulation event causes the processor to enter emulation mode, allowing command and control of the processor via the JTAG interface.
- **Reset** – This event resets the processor.
- **Nonmaskable Interrupt (NMI)** – The NMI event can be generated by the software watchdog timer or by the NMI input signal to the processor. The NMI event is frequently used as a power-down indicator to initiate an orderly shutdown of the system.
- **Exceptions** – Events that occur synchronously to program flow, i.e., the exception will be taken before the instruction is allowed to complete. Conditions such as data alignment violations or undefined instructions cause exceptions.
- **Interrupts** – Events that occur asynchronously to program flow. They are caused by timers, peripherals, input pins, and an explicit software instruction.

Each event has an associated register to hold the return address and an associated "return from event" instruction. When an event is triggered, the state of the processor is saved on the supervisor stack.

The ADSP-BF561 event controller consists of two stages: the Core Event Controller (CEC) and the System Interrupt Controller (SIC). The Core Event Controller works with the System Interrupt Controller to prioritize and control all system events. Conceptually, interrupts from the peripherals enter into the SIC, and are then routed directly into the general-purpose interrupts of the CEC.

**Core Event Controller (CEC)**

The CEC supports nine general-purpose interrupts (IVG15–7), in addition to the dedicated interrupt and exception events. Of these general-purpose interrupts, the two lowest priority interrupts (IVG15–14) are recommended to be reserved for software interrupt handlers, leaving seven prioritized interrupt inputs to support the peripherals of the ADSP-BF561. Table 1 describes the inputs to the CEC, identifies their names in the Event Vector Table (EVT), and lists their priorities.

**Table 1. Core Event Controller (CEC)**

<table>
<thead>
<tr>
<th>Priority (0 is Highest)</th>
<th>Event Class</th>
<th>EVT Entry</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Emulation/Test Control</td>
<td>EMU</td>
</tr>
<tr>
<td>0</td>
<td>Reset</td>
<td>RST</td>
</tr>
<tr>
<td>1</td>
<td>Nonmaskable Interrupt</td>
<td>NMI</td>
</tr>
<tr>
<td>2</td>
<td>Exceptions</td>
<td>EVX</td>
</tr>
<tr>
<td>3</td>
<td>Global Enable</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Hardware Error</td>
<td>IVHW</td>
</tr>
<tr>
<td>5</td>
<td>Core Timer</td>
<td>IVTMR</td>
</tr>
<tr>
<td>6</td>
<td>General Interrupt 7</td>
<td>IVG7</td>
</tr>
<tr>
<td>7</td>
<td>General Interrupt 8</td>
<td>IVG8</td>
</tr>
<tr>
<td>8</td>
<td>General Interrupt 9</td>
<td>IVG9</td>
</tr>
<tr>
<td>9</td>
<td>General Interrupt 10</td>
<td>IVG10</td>
</tr>
<tr>
<td>10</td>
<td>General Interrupt 11</td>
<td>IVG11</td>
</tr>
<tr>
<td>11</td>
<td>General Interrupt 12</td>
<td>IVG12</td>
</tr>
<tr>
<td>12</td>
<td>General Interrupt 13</td>
<td>IVG13</td>
</tr>
<tr>
<td>13</td>
<td>General Interrupt 14</td>
<td>IVG14</td>
</tr>
<tr>
<td>14</td>
<td>General Interrupt 15</td>
<td>IVG15</td>
</tr>
</tbody>
</table>

**System Interrupt Controller (SIC)**

The System Interrupt Controller provides the mapping and routing of events from the many peripheral interrupt sources to the prioritized general-purpose interrupt inputs of the CEC. Although the ADSP-BF561 provides a default mapping, the user can alter the mappings and priorities of interrupt events by
writing the appropriate values into the Interrupt Assignment Registers (SIC_IAR7–0). Table 2 describes the inputs into the SIC and the default mappings into the CEC.

Table 2. System Interrupt Controller (SIC)

<table>
<thead>
<tr>
<th>Peripheral Interrupt Event</th>
<th>Default Mapping</th>
</tr>
</thead>
<tbody>
<tr>
<td>PLL Wakeup</td>
<td>IVG7</td>
</tr>
<tr>
<td>DMA1 Error (Generic)</td>
<td>IVG7</td>
</tr>
<tr>
<td>DMA2 Error (Generic)</td>
<td>IVG7</td>
</tr>
<tr>
<td>IMDMA Error</td>
<td>IVG7</td>
</tr>
<tr>
<td>PPI0 Error</td>
<td>IVG7</td>
</tr>
<tr>
<td>PPI1 Error</td>
<td>IVG7</td>
</tr>
<tr>
<td>SPORT0 Error</td>
<td>IVG7</td>
</tr>
<tr>
<td>SPORT1 Error</td>
<td>IVG7</td>
</tr>
<tr>
<td>SPI Error</td>
<td>IVG7</td>
</tr>
<tr>
<td>UART Error</td>
<td>IVG7</td>
</tr>
<tr>
<td>Reserved</td>
<td>IVG7</td>
</tr>
<tr>
<td>DMA1 Channel 0 Interrupt (PPI0)</td>
<td>IVG8</td>
</tr>
<tr>
<td>DMA1 Channel 1 Interrupt (PPI1)</td>
<td>IVG8</td>
</tr>
<tr>
<td>DMA1 Channel 2 Interrupt</td>
<td>IVG8</td>
</tr>
<tr>
<td>DMA1 Channel 4 Interrupt</td>
<td>IVG8</td>
</tr>
<tr>
<td>DMA1 Channel 5 Interrupt</td>
<td>IVG8</td>
</tr>
<tr>
<td>DMA1 Channel 6 Interrupt</td>
<td>IVG8</td>
</tr>
<tr>
<td>DMA1 Channel 7 Interrupt</td>
<td>IVG8</td>
</tr>
<tr>
<td>DMA1 Channel 8 Interrupt</td>
<td>IVG8</td>
</tr>
<tr>
<td>DMA1 Channel 9 Interrupt</td>
<td>IVG8</td>
</tr>
<tr>
<td>DMA1 Channel 10 Interrupt</td>
<td>IVG8</td>
</tr>
<tr>
<td>DMA1 Channel 11 Interrupt</td>
<td>IVG8</td>
</tr>
<tr>
<td>DMA2 Channel 0 Interrupt (SPORT0 Rx)</td>
<td>IVG9</td>
</tr>
<tr>
<td>DMA2 Channel 1 Interrupt (SPORT0 Tx)</td>
<td>IVG9</td>
</tr>
<tr>
<td>DMA2 Channel 2 Interrupt (SPORT1 Rx)</td>
<td>IVG9</td>
</tr>
<tr>
<td>DMA2 Channel 3 Interrupt (SPORT1 Tx)</td>
<td>IVG9</td>
</tr>
<tr>
<td>DMA2 Channel 4 Interrupt (SPI)</td>
<td>IVG9</td>
</tr>
<tr>
<td>DMA2 Channel 5 Interrupt (UART Rx)</td>
<td>IVG9</td>
</tr>
<tr>
<td>DMA2 Channel 6 Interrupt (UART Tx)</td>
<td>IVG9</td>
</tr>
<tr>
<td>DMA2 Channel 7 Interrupt</td>
<td>IVG9</td>
</tr>
<tr>
<td>DMA2 Channel 8 Interrupt</td>
<td>IVG9</td>
</tr>
<tr>
<td>DMA2 Channel 9 Interrupt</td>
<td>IVG9</td>
</tr>
<tr>
<td>DMA2 Channel 10 Interrupt</td>
<td>IVG9</td>
</tr>
<tr>
<td>DMA2 Channel 11 Interrupt</td>
<td>IVG9</td>
</tr>
<tr>
<td>Timer0 Interrupt</td>
<td>IVG10</td>
</tr>
<tr>
<td>Timer1 Interrupt</td>
<td>IVG10</td>
</tr>
<tr>
<td>Timer2 Interrupt</td>
<td>IVG10</td>
</tr>
<tr>
<td>Timer3 Interrupt</td>
<td>IVG10</td>
</tr>
<tr>
<td>Timer4 Interrupt</td>
<td>IVG10</td>
</tr>
<tr>
<td>Timer5 Interrupt</td>
<td>IVG10</td>
</tr>
<tr>
<td>Timer6 Interrupt</td>
<td>IVG10</td>
</tr>
</tbody>
</table>

Table 2. System Interrupt Controller (SIC) (Continued)

<table>
<thead>
<tr>
<th>Peripheral Interrupt Event</th>
<th>Default Mapping</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer7 Interrupt</td>
<td>IVG10</td>
</tr>
<tr>
<td>Timer8 Interrupt</td>
<td>IVG10</td>
</tr>
<tr>
<td>Timer9 Interrupt</td>
<td>IVG10</td>
</tr>
<tr>
<td>Timer10 Interrupt</td>
<td>IVG10</td>
</tr>
<tr>
<td>Timer11 Interrupt</td>
<td>IVG10</td>
</tr>
<tr>
<td>Programmable Flags 15–0 Interrupt A</td>
<td>IVG11</td>
</tr>
<tr>
<td>Programmable Flags 15–0 Interrupt B</td>
<td>IVG11</td>
</tr>
<tr>
<td>Programmable Flags 31–16 Interrupt A</td>
<td>IVG11</td>
</tr>
<tr>
<td>Programmable Flags 31–16 Interrupt B</td>
<td>IVG11</td>
</tr>
<tr>
<td>Programmable Flags 47–32 Interrupt A</td>
<td>IVG11</td>
</tr>
<tr>
<td>Programmable Flags 47–32 Interrupt B</td>
<td>IVG11</td>
</tr>
<tr>
<td>DMA1 Channel 12/13 Interrupt (Memory DMA/Stream 0)</td>
<td>IVG8</td>
</tr>
<tr>
<td>DMA1 Channel 14/15 Interrupt (Memory DMA/Stream 1)</td>
<td>IVG8</td>
</tr>
<tr>
<td>DMA2 Channel 12/13 Interrupt (Memory DMA/Stream 0)</td>
<td>IVG9</td>
</tr>
<tr>
<td>DMA2 Channel 14/15 Interrupt (Memory DMA/Stream 1)</td>
<td>IVG9</td>
</tr>
<tr>
<td>IMDMA Stream 0 Interrupt</td>
<td>IVG12</td>
</tr>
<tr>
<td>IMDMA Stream 1 Interrupt</td>
<td>IVG12</td>
</tr>
<tr>
<td>Watchdog Timer Interrupt</td>
<td>IVG13</td>
</tr>
<tr>
<td>Reserved</td>
<td>IVG7</td>
</tr>
<tr>
<td>Reserved</td>
<td>IVG7</td>
</tr>
<tr>
<td>Supplemental Interrupt 0</td>
<td>IVG7</td>
</tr>
<tr>
<td>Supplemental Interrupt 1</td>
<td>IVG7</td>
</tr>
</tbody>
</table>

Event Control

The ADSP-BF561 provides the user with a very flexible mechanism to control the processing of events. In the CEC, three registers are used to coordinate and control events. Each of the registers is 16 bits wide, while each bit represents a particular event class.

- CEC Interrupt Latch Register (ILAT) – The ILAT register indicates when events have been latched. The appropriate bit is set when the processor has latched the event and cleared when the event has been accepted into the system. This register is updated automatically by the controller, but may also be written to clear (cancel) latched events. This register may be read while in supervisor mode and may only be written while in supervisor mode when the corresponding IMASK bit is cleared.

- CEC Interrupt Mask Register (IMASK) – The IMASK register controls the masking and unmasking of individual events. When a bit is set in the IMASK register, that event is unmasked and will be processed by the CEC when asserted. A cleared bit in the IMASK register masks the event, thereby preventing the processor from servicing the event.
even though the event may be latched in the ILAT register. This register may be read from or written to while in supervisor mode.

Note that general-purpose interrupts can be globally enabled and disabled with the STI and CLI instructions, respectively.

- CEC Interrupt Pending Register (IPEND) – The IPEND register keeps track of all nested events. A set bit in the IPEND register indicates the event is currently active or nested at some level. This register is updated automatically by the controller but may be read while in supervisor mode. The SIC allows further control of event processing by providing six 32-bit interrupt control and status registers. Each register contains a bit corresponding to each of the peripheral interrupt events shown in Table 2.

- SIC Interrupt Mask Registers (SIC_IMASKx) – These registers control the masking and unmasking of each peripheral interrupt event. When a bit is set in these registers, that peripheral event is unmasked and will be processed by the system when asserted. A cleared bit in these registers masks the peripheral event, thereby preventing the processor from servicing the event.

- SIC Interrupt Status Registers (SIC_ISRx) – As multiple peripherals can be mapped to a single event, these registers allow the software to determine which peripheral event source triggered the interrupt. A set bit indicates the peripheral is asserting the interrupt; a cleared bit indicates the peripheral is not asserting the event.

- SIC Interrupt Wakeup Enable Registers (SIC_IWRx) – By enabling the corresponding bit in these registers, each peripheral can be configured to wake up the processor, should the processor be in a powered-down mode when the event is generated.

Because multiple interrupt sources can map to a single general-purpose interrupt, multiple pulse assertions can occur simultaneously, before or during interrupt processing for an interrupt event already detected on this interrupt input. The IPEND register contents are monitored by the SIC as the interrupt acknowledgement.

The appropriate ILAT register bit is set when an interrupt rising edge is detected (detection requires two core clock cycles). The bit is cleared when the respective IPEND register bit is set. The IPEND bit indicates that the event has entered into the processor pipeline. At this point the CEC will recognize and queue the next rising edge event on the corresponding event input. The minimum latency from the rising edge transition of the general-purpose interrupt to the IPEND output asserted is three core clock cycles; however, the latency can be much higher, depending on the activity within and the mode of the processor.

**DMA CONTROLLERS**

The ADSP-BF561 has two independent DMA controllers that support automated data transfers with minimal overhead for the DSP cores. DMA transfers can occur between the ADSP-BF561 internal memories and any of its DMA-capable peripherals. Additionally, DMA transfers can be accomplished between any of the DMA-capable peripherals and external devices connected to the external memory interfaces, including the SDRAM controller and the asynchronous memory controller. DMA-capable peripherals include the SPORTs, SPI port, UART, and PPIs. Each individual DMA-capable peripheral has at least one dedicated DMA channel.

The ADSP-BF561 DMA controllers support both 1-dimensional (1-D) and 2-dimensional (2-D) DMA transfers. DMA transfer initialization can be implemented from registers or from sets of parameters called descriptor blocks.

The 2-D DMA capability supports arbitrary row and column sizes up to 64K elements by 64K elements, and arbitrary row and column step sizes up to ± 32K elements. Furthermore, the column step size can be less than the row step size, allowing implementation of interleaved data streams. This feature is especially useful in video applications where data can be de-interleaved on the fly.

Examples of DMA types supported by the ADSP-BF561 DMA controllers include:

- A single linear buffer that stops upon completion.
- A circular autorefreshing buffer that interrupts on each full or fractionally full buffer.
- 1-D or 2-D DMA using a linked list of descriptors.
- 2-D DMA using an array of descriptors, specifying only the base DMA address within a common page.

In addition to the dedicated peripheral DMA channels, each DMA Controller has four memory DMA channels provided for transfers between the various memories of the ADSP-BF561 system. These enable transfers of blocks of data between any of the memories—including external SDRAM, ROM, SRAM, and flash memory—with minimal processor intervention. Memory DMA transfers can be controlled by a very flexible descriptor-based methodology or by a standard register-based autobuffer mechanism.

Further, the ADSP-BF561 has a four channel Internal Memory DMA (IMDMA) Controller. The IMDMA Controller allows data transfers between any of the internal L1 and L2 memories.

**WATCHDOG TIMER**

Each ADSP-BF561 core includes a 32-bit timer, which can be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state, via generation of a hardware reset, nonmaskable interrupt (NMI), or general-purpose interrupt, if the timer expires before being reset by software. The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts to zero from the programmed value. This protects the system from remaining in an unknown state where software, which would normally reset the timer, has stopped running due to an external noise condition or software error.
After a reset, software can determine if the watchdog was the source of the hardware reset by interrogating a status bit in the timer control register, which is set only upon a watchdog generated reset.

The timer is clocked by the system clock (SCLK) at a maximum frequency of \( f_{SCLK} \).

**TIMERS**

There are 14 programmable timer units in the ADSP-BF561. Each of the 12 general-purpose timer units can be independently programmed as a Pulse Width Modulator (PWM), internally or externally clocked timer, or pulse width counter. The general-purpose timer units can be used in conjunction with the UART to measure the width of the pulses in the data stream to provide an autobaud detect function for a serial channel. The general-purpose timers can generate interrupts to the processor core providing periodic events for synchronization, either to the processor clock or to a count of external signals.

In addition to the 12 general-purpose programmable timers, another timer is also provided for each core. These extra timers are clocked by the internal processor clock (CCLK) and are typically used as a system tick clock for generation of operating system periodic interrupts.

**SERIAL PORTS (SPORTs)**

The ADSP-BF561 incorporates two dual-channel synchronous serial ports (SPORT0 and SPORT1) for serial and multiprocessor communications. The SPORTs support the following features:

- I²S capable operation.
- Bidirectional operation – Each SPORT has two sets of independent transmit and receive pins, enabling eight channels of I²S stereo audio.
- Buffered (8-deep) transmit and receive ports – Each port has a data register for transferring data words to and from other DSP components and shift registers for shifting data in and out of the data registers.
- Clocking – Each transmit and receive port can either use an external serial clock or generate its own, in frequencies ranging from \( (f_{SCLK}/131,070) \) Hz to \( (f_{SCLK}/2) \) Hz.
- Word length – Each SPORT supports serial data words from 3 bits to 32 bits in length, transferred most significant bit first or least significant bit first.
- Framing – Each transmit and receive port can run with or without frame sync signals for each data word. Frame sync signals can be generated internally or externally, active high or low, and with either of two pulse widths and early or late frame sync.
- Companding in hardware – Each SPORT can perform A-law or μ-law companding according to ITU recommendation G.711. Companding can be selected on the transmit and/or receive channel of the SPORT without additional latencies.
- DMA operations with single-cycle overhead – Each SPORT can automatically receive and transmit multiple buffers of memory data. The DSP can link or chain sequences of DMA transfers between a SPORT and memory.
- Interrupts – Each transmit and receive port generates an interrupt upon completing the transfer of a data word or after transferring an entire data buffer or buffers through DMA.
- Multichannel capability – Each SPORT supports 128 channels out of a 1,024-channel window and is compatible with the H.100, H.110, MVP-90, and HMVIP standards.

An additional 250 mV of SPORT input hysteresis can be enabled by setting Bit 15 of the PLL_CTL register. When this bit is set, all SPORT input pins have the increased hysteresis.

**SERIAL PERIPHERAL INTERFACE (SPI) PORT**

The ADSP-BF561 processor has an SPI-compatible port that enables the processor to communicate with multiple SPI-compatible devices.

The SPI interface uses three pins for transferring data: two data pins (master output-slave input, MOSI, and master input-slave output, MISO) and a clock pin (serial clock, SCK). An SPI chip select input pin (SPISS) lets other SPI devices select the processor, and seven SPI chip select output pins (SPISEL7–1) let the processor select other SPI devices. The SPI select pins are reconfigured programmable flag pins. Using these pins, the SPI port provides a full-duplex, synchronous serial interface which supports both master/slave modes and multimaster environments. The baud rate and clock phase/polarities for the SPI port are programmable, and it has an integrated DMA controller, configurable to support transmit or receive data streams. The SPI DMA controller can only service unidirectional accesses at any given time.

The SPI port clock rate is calculated as:

\[
SPI \text{ Clock Rate} = \frac{f_{SCLK}}{2 \times SPI\_BAUD}
\]

Where the 16-bit SPI_BAUD register contains a value of 2 to 65,535.

During transfers, the SPI port simultaneously transmits and receives by serially shifting data in and out on its two serial data lines. The serial clock line synchronizes the shifting and sampling of data on the two serial data lines.
UART PORT

The ADSP-BF561 processor provides a full-duplex universal asynchronous receiver/transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. The UART port includes support for 5 data bits to 8 data bits, 1 stop bit or 2 stop bits, and none, even, or odd parity. The UART port supports two modes of operation:

- PIO (programmed I/O) – The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. The UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

The baud rate, serial data format, error code generation and status, and interrupts for the UART port are programmable.

The UART programmable features include:

- Supporting bit rates ranging from \( f_{SCLK}/1,048,576 \) bits per second to \( f_{SCLK}/16 \) bits per second.
- Supporting data formats from seven bits to 12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

The UART port’s clock rate is calculated as:

\[
UART \text{ Clock Rate} = \frac{f_{SCLK}}{16 \times UART_{\text{Divisor}}}
\]

Where the 16-bit UART_Divisor comes from the UART_DLH register (most significant 8 bits) and UART_DLL register (least significant 8 bits).

In conjunction with the general-purpose timer functions, autobaud detection is supported.

The capabilities of the UART are further extended with support for the Infrared Data Association (IrDA®) serial infrared physical layer link specification (SIR) protocol.

PROGRAMMABLE FLAGS (PFx)

The ADSP-BF561 has 48 bidirectional, general-purpose I/O, programmable flag (PF47–0) pins. Some programmable flag pins are used by peripherals (see Pin Descriptions). When not used as a peripheral pin, each programmable flag can be individually controlled by manipulation of the flag control, status, and interrupt registers as follows:

- Flag direction control register – Specifies the direction of each individual PFx pin as input or output.
- Flag control and status registers – Rather than forcing the software to use a read-modify-write process to control the setting of individual flags, the ADSP-BF561 employs a “write one to set” and “write one to clear” mechanism that allows any combination of individual flags to be set or cleared in a single instruction, without affecting the level of any other flags. Two control registers are provided, one register is written-to in order to set flag values, while another register is written-to in order to clear flag values. Reading the flag status register allows software to interrogate the sense of the flags.
- Flag interrupt mask registers – These registers allow each individual PFx pin to function as an interrupt to the processor. Similar to the flag control registers that are used to set and clear individual flag values, one flag interrupt mask register sets bits to enable an interrupt function, and the other flag interrupt mask register clears bits to disable an interrupt function. PFx pins defined as inputs can be configured to generate hardware interrupts, while output PFx pins can be configured to generate software interrupts.
- Flag interrupt sensitivity registers – These registers specify whether individual PFx pins are level- or edge-sensitive and specify, if edge-sensitive, whether just the rising edge or both the rising and falling edges of the signal are significant. One register selects the type of sensitivity, and one register selects which edges are significant for edge sensitivity.

PARALLEL PERIPHERAL INTERFACE

The ADSP-BF561 processor provides two parallel peripheral interfaces (PPI0, PPI1) that can connect directly to parallel A/D and D/A converters, video encoders and decoders, and other general-purpose peripherals. The PPI consists of a dedicated input clock pin, up to 3 frame synchronization pins, and up to 16 data pins. The input clock supports parallel data rates at up to \( f_{SCLK}/2 \text{ MHz} \), and the synchronization signals can be configured as either inputs or outputs.

The PPI supports a variety of general-purpose and ITU-R 656 modes of operation. In general-purpose mode, the PPI provides half-duplex, bi-directional data transfer with up to 16 bits of data. Up to 3 frame synchronization signals are also provided. In ITU-R 656 mode, the PPI provides half-duplex, bi-directional transfer of 8- or 10-bit video data. Additionally, on-chip decode of embedded start-of-line (SOL) and start-of-field (SOF) preamble packets is supported.

General-Purpose Mode Descriptions

The general-purpose modes of the PPI are intended to suit a wide variety of data capture and transmission applications. Three distinct submodes are supported:

- Input mode – frame syncs and data are inputs into the PPI.
- Frame capture mode – frame syncs are outputs from the PPI, but data are inputs.
- Output mode – frame syncs and data are outputs from the PPI.

Input Mode

Input mode is intended for ADC applications, as well as video communication with hardware signaling. In its simplest form, PPI_FSI is an external frame sync input that controls when to
read data. The PPI_DELAY MMR allows for a delay (in PPI_CLK cycles) between reception of this frame sync and the initiation of data reads. The number of input data samples is user programmable and defined by the contents of the PPI_COUNT register. The PPI supports 8-bit, and 10-bit through 16-bit data, and are programmable in the PPI_CONTROL register.

Frame Capture Mode
Frame capture mode allows the video source(s) to act as a slave (e.g., for frame capture). The ADSP-BF561 processors control when to read from the video source(s). PPI_FS1 is an HSYNC output and PPI_FS2 is a VSYNC output.

Output Mode
Output mode is used for transmitting video or other data with up to three output frame syncs. Typically, a single frame sync is appropriate for data converter applications, whereas two or three frame syncs could be used for sending video with hardware signaling.

ITU-R 656 Mode Descriptions
The ITU-R 656 modes of the PPI are intended to suit a wide variety of video capture, processing, and transmission applications. Three distinct submodes are supported:

- Active video only mode
- Vertical blanking only mode
- Entire field mode

Active Video Only Mode
Active video only mode is used when only the active video portion of a field is of interest and not any of the blanking intervals. The PPI does not read in any data between the end of active video (EAV) and start of active video (SAV) preamble symbols, or any data present during the vertical blanking intervals. In this mode, the control byte sequences are not stored to memory; they are filtered by the PPI. After synchronizing to the start of Field 1, the PPI ignores incoming samples until it sees an SAV code. The user specifies the number of active video lines per frame (in the PPI_COUNT register).

Vertical Blanking Interval Mode
In this mode, the PPI only transfers vertical blanking interval (VBI) data.

Entire Field Mode
In this mode, the entire incoming bit stream is read in through the PPI. This includes active video, control preamble sequences, and ancillary data that may be embedded in horizontal and vertical blanking intervals. Data transfer starts immediately after synchronization to Field 1.

DYNAMIC POWER MANAGEMENT
The ADSP-BF561 provides four power management modes and one power management state, each with a different performance/power profile. In addition, dynamic power management provides the control functions to dynamically alter the processor core supply voltage, further reducing power dissipation. Control of clocking to each of the ADSP-BF561 peripherals also reduces power consumption. See Table 3 for a summary of the power settings for each mode.

Table 3. Power Settings

<table>
<thead>
<tr>
<th>Mode/State</th>
<th>PLL</th>
<th>PLL Bypassed</th>
<th>Core Clock (CCLK)</th>
<th>System Clock (SCLK)</th>
<th>Core Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full-On</td>
<td>Enabled</td>
<td>No</td>
<td>Enabled</td>
<td>Enabled</td>
<td>On</td>
</tr>
<tr>
<td>Active</td>
<td>Enabled/ Disabled</td>
<td>Yes</td>
<td>Enabled</td>
<td>Enabled</td>
<td>On</td>
</tr>
<tr>
<td>Sleep</td>
<td>Enabled</td>
<td>–</td>
<td>Disabled</td>
<td>Enabled</td>
<td>On</td>
</tr>
<tr>
<td>Deep Sleep</td>
<td>Disabled</td>
<td>–</td>
<td>Disabled</td>
<td>Disabled</td>
<td>On</td>
</tr>
<tr>
<td>Hibernate</td>
<td>Disabled</td>
<td>–</td>
<td>Disabled</td>
<td>Disabled</td>
<td>Off</td>
</tr>
</tbody>
</table>

Full-On Operating Mode—Maximum Performance
In the full-on mode, the PLL is enabled and is not bypassed, providing capability for maximum operational frequency. This is the default execution state in which maximum performance can be achieved. The processor cores and all enabled peripherals run at full speed.

Active Operating Mode—Moderate Power Savings
In the active mode, the PLL is enabled but bypassed. Because the PLL is bypassed, the processor’s core clock (CCLK) and system clock (SCLK) run at the input clock (CLKIN) frequency. In this mode, the CLKIN to CCLK multiplier ratio can be changed, although the changes are not realized until the full-on mode is entered. DMA access is available to appropriately configured L1 and L2 memories.

In the active mode, it is possible to disable the PLL through the PLL control register (PLL_CTL). If disabled, the PLL must be re-enabled before transitioning to the full-on or sleep modes.

Sleep Operating Mode—High Dynamic Power Savings
The sleep mode reduces power dissipation by disabling the clock to the processor core (CCLK). The PLL and system clock (SCLK), however, continue to operate in this mode. Typically an external event will wake up the processor. When in the sleep mode, assertion of wakeup will cause the processor to sense the value of the BYPASS bit in the PLL control register (PLL_CTL). When in the sleep mode, system DMA access is only available to external memory, not to L1 or on-chip L2 memory.

Deep Sleep Operating Mode—Maximum Dynamic Power Savings
The deep sleep mode maximizes power savings by disabling the clocks to the processor cores (CCLK) and to all synchronous peripherals (SCLK). Asynchronous peripherals will not be able to access internal resources or external memory. This powered-down mode can only be exited by assertion of the reset pin (RESET). If BYPASS is disabled, the processor will transition to the full-on mode. If BYPASS is enabled, the processor will transition to the active mode.
**Hibernate State—Maximum Static Power Savings**

The hibernate state maximizes static power savings by disabling the voltage and clocks to the processor core (CCLK) and to all the synchronous peripherals (SCLK). The internal voltage regulator for the processor can be shut off by writing b#00 to the FREQ bits of the VR_CTL register. This disables both CCLK and SCLK. Furthermore, it sets the internal power supply voltage \( V_{\text{INT}} \) to 0 V to provide the lowest static power dissipation. Any critical information stored internally (memory contents, register contents, etc.) must be written to a nonvolatile storage device prior to removing power if the processor state is to be preserved. Since \( V_{\text{EXT}} \) is still supplied in this mode, all of the external pins three-state, unless otherwise specified. This allows other devices that may be connected to the processor to have power still applied without drawing unwanted current. The internal supply regulator can be woken up by asserting the \( \text{RESET} \) pin.

**Power Savings**

As shown in Table 4, the ADSP-BF561 supports two different power domains. The use of multiple power domains maximizes flexibility, while maintaining compliance with industry standards and conventions. By isolating the internal logic of the ADSP-BF561 into its own power domain, separate from the I/O, the processor can take advantage of Dynamic Power Management, without affecting the I/O devices. There are no sequencing requirements for the various power domains.

**Table 4. ADSP-BF561 Power Domains**

<table>
<thead>
<tr>
<th>Power Domain</th>
<th>( V_{\text{DD}} ) Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>All internal logic</td>
<td>( V_{\text{DDINT}} )</td>
</tr>
<tr>
<td>I/O</td>
<td>( V_{\text{DDEXT}} )</td>
</tr>
</tbody>
</table>

The power dissipated by a processor is largely a function of the clock frequency of the processor and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in dynamic power dissipation, while reducing the voltage by 25% reduces dynamic power dissipation by more than 40%. Further, these power savings are additive in that if the clock frequency and supply voltage are both reduced, the power savings can be dramatic.

The dynamic power management feature of the ADSP-BF561 allows both the processor’s input voltage \( V_{\text{DDINT}} \) and clock frequency \( f_{\text{CCLK}} \) to be dynamically controlled.

The savings in power dissipation can be modeled using the power savings factor and % power savings calculations.

The power savings factor is calculated as:

\[
\text{power savings factor} = \frac{f_{\text{CCLKRED}}}{f_{\text{CCLKNOM}}} \times \left( \frac{V_{\text{DDINTRED}}}{V_{\text{DDINTNOM}}} \right)^2 \times \left( \frac{t_{\text{RED}}}{t_{\text{NOM}}} \right)
\]

where the variables in the equations are:

- \( f_{\text{CCLKNOM}} \) is the nominal core clock frequency
- \( f_{\text{CCLKRED}} \) is the reduced core clock frequency
- \( V_{\text{DDINTNOM}} \) is the nominal internal supply voltage
- \( V_{\text{DDINTRED}} \) is the reduced internal supply voltage
- \( t_{\text{NOM}} \) is the duration running at \( f_{\text{CCLKNOM}} \)
- \( t_{\text{RED}} \) is the duration running at \( f_{\text{CCLKRED}} \)

The percent power savings is calculated as:

\[
\% \text{ power savings} = (1 - \text{power savings factor}) \times 100\%
\]

**VOLTAGE REGULATION**

The ADSP-BF561 processor provides an on-chip voltage regulator that can generate appropriate \( V_{\text{DDINT}} \) voltage levels from the \( V_{\text{DDEXT}} \) supply. See Operating Conditions for regulator tolerances and acceptable \( V_{\text{DDINT}} \) ranges for specific models.

Figure 4 shows the typical external components required to complete the power management system. The regulator controls the internal logic voltage levels and is programmable with the voltage regulator control register (VR_CTL) in increments of 50 mV. To reduce standby power consumption, the internal voltage regulator can be programmed to remove power to the processor core while keeping I/O power \( V_{\text{DDINT}} \) supplied. While in the hibernate state, \( V_{\text{DDINT}} \) can still be applied, thus eliminating the need for external buffers. The voltage regulator can be activated from this power-down state by asserting \( \text{RESET} \), which will then initiate a boot sequence. The regulator can also be disabled and bypassed at the user’s discretion.

The internal voltage regulation feature is not available on any of the 600 MHz speed grade models. External voltage regulation is required to ensure correct operation of these parts at 600 MHz.

![Figure 4. Voltage Regulator Circuit](image_url)

**Voltage Regulator Layout Guidelines**

Regulator external component placement, board routing, and bypass capacitors all have a significant effect on noise injected into the other analog circuits on-chip. The VROUT1–0 traces and voltage regulator external components should be...
considered as noise sources when doing board layout and should not be routed or placed near sensitive circuits or components on the board. All internal and I/O power supplies should be well bypassed with bypass capacitors placed as close to the ADSP-BF561 processors as possible.

For further details on the on-chip voltage regulator and related board design guidelines, see the Switching Regulator Design Considerations for ADSP-BF533 Blackfin Processors (EE-228) applications note at www.analog.com—use site search on “EE-228”.

**CLOCK SIGNALS**

The ADSP-BF561 processor can be clocked by an external crystal, a sine wave input, or a buffered, shaped clock derived from an external clock oscillator.

If an external clock is used, it must not be halted, changed, or operated below the specified frequency during normal operation. This signal is connected to the processor’s CLKIN pin. When an external clock is used, the XTAL pin must be left unconnected.

Alternatively, because the ADSP-BF561 processor includes an on-chip oscillator circuit, an external crystal may be used. For fundamental frequency operation, use the circuit shown in Figure 5. A parallel-resonant, fundamental frequency, microprocessor-grade crystal is connected across the CLKIN and XTAL pins. The on-chip resistance between CLKIN and the XTAL pin is in the 500 kΩ range. Further parallel resistors are typically not recommended. The two capacitors and the series resistor shown in Figure 5 fine tune the phase and amplitude of the sine frequency. The capacitor and resistor values shown in Figure 5 are typical values only. The capacitor values are dependent upon the crystal manufacturer’s load capacitance recommendations and the physical PCB layout. The resistor value depends on the drive level specified by the crystal manufacturer. System designs should verify the customized values based on careful investigation on multiple devices over the allowed temperature range.

A third-overtone crystal can be used at frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone, by adding a tuned inductor circuit as shown in Figure 5.

As shown in Figure 6, the core clock (CCLK) and system peripheral clock (SCLK) are derived from the input clock (CLKIN) signal. An on-chip PLL is capable of multiplying the CLKIN signal by a user-programmable 0.5× to 64× multiplication factor. The default multiplier is 10×, but it can be modified by a software instruction sequence. On the fly frequency changes can be effected by simply writing to the PLL_DIV register.

All on-chip peripherals are clocked by the system clock (SCLK). The system clock frequency is programmable by means of the SSEL3–0 bits of the PLL_DIV register. The values programmed into the SSEL fields define a divide ratio between the PLL output (VCO) and the system clock. SCLK divider values are 1 through 15. Table 5 illustrates typical system clock ratios.

### Table 5. Example System Clock Ratios

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Divider Ratio</th>
<th>Example Frequency Ratios (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SSEL3–0</td>
<td>VCO/SCLK</td>
<td>VCO</td>
</tr>
<tr>
<td>0001</td>
<td>1:1</td>
<td>100</td>
</tr>
<tr>
<td>0110</td>
<td>6:1</td>
<td>300</td>
</tr>
<tr>
<td>1010</td>
<td>10:1</td>
<td>500</td>
</tr>
</tbody>
</table>

The maximum frequency of the system clock is $f_{SCLK}$. Note that the divisor ratio must be chosen to limit the system clock frequency to its maximum of $f_{SCLK}$. The SSEL value can be changed dynamically without any PLL lock latencies by writing the appropriate values to the PLL divisor register (PLL_DIV).
The core clock (CCLK) frequency can also be dynamically changed by means of the CSEL1–0 bits of the PLL_DIV register. Supported CCLK divider ratios are 1, 2, 4, and 8, as shown in Table 6. This programmable core clock capability is useful for fast core frequency modifications.

### Table 6. Core Clock Ratios

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Divider Ratio</th>
<th>Example Frequency Ratios (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSEL1–0</td>
<td>VCO/CCLK</td>
<td>VCO</td>
</tr>
<tr>
<td>00</td>
<td>1:1</td>
<td>500</td>
</tr>
<tr>
<td>01</td>
<td>2:1</td>
<td>500</td>
</tr>
<tr>
<td>10</td>
<td>4:1</td>
<td>200</td>
</tr>
<tr>
<td>11</td>
<td>8:1</td>
<td>200</td>
</tr>
</tbody>
</table>

The maximum PLL clock time when a change is programmed via the PLL_CTL register is 40 μs. This value should be programmed to ensure a 40 μs wakeup time when either the voltage is changed or a new MSEL value is programmed. The value should be programmed to ensure an 80 μs wakeup time when both voltage and the MSEL value are changed. The time base for the PLL_LOCKCNT register is the period of CLKN.

### BOOTING MODES

The ADSP-BF561 has three mechanisms (listed in Table 7) for automatically loading internal L1 instruction memory, L2, or external memory after a reset. A fourth mode is provided to execute from external memory, bypassing the boot sequence.

### Table 7. Booting Modes

<table>
<thead>
<tr>
<th>BMODE1–0 Description</th>
<th>Signal Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>Execute from 16-bit external memory (Bypass Boot ROM)</td>
<td>00</td>
</tr>
<tr>
<td>Boot from 8-bit/16-bit flash</td>
<td>01</td>
</tr>
<tr>
<td>Boot from SPI host slave mode</td>
<td>10</td>
</tr>
<tr>
<td>Boot from SPI serial EEPROM (16-, 24-bit addressable)</td>
<td>11</td>
</tr>
</tbody>
</table>

The BMODE pins of the reset configuration register, sampled during power-on resets and software initiated resets, implement the following modes:

- **Execute from 16-bit external memory** – Execution starts from address 0x2000 0000 with 16-bit packing. The boot ROM is bypassed in this mode. All configuration settings are set for the slowest device possible (3-cycle hold time, 15-cycle R/W access times, 4-cycle setup). Note that, in bypass mode, only Core A can execute instructions from external memory.
- **Boot from 8-bit/16-bit external flash memory** – The 8-bit/16-bit flash boot routine located in boot ROM memory space is set up using Asynchronous Memory Bank 0.

All configuration settings are set for the slowest device possible (3-cycle hold time; 15-cycle R/W access times; 4-cycle setup).

- Boot from SPI host device – The Blackfin processor operates in SPI slave mode and is configured to receive the bytes of the .LDR file from an SPI host (master) agent. To hold off the host device from transmitting while the boot ROM is busy, the Blackfin processor asserts a GPIO pin, called host wait (HWAIT), to signal the host device not to send any more bytes until the flag is deasserted. The flag is chosen by the user and this information is transferred to the Blackfin processor via bits 10:5 of the FLAG header.
- Boot from SPI serial EEPROM (16-, 24-bit addressable) – The SPI uses the PF2 output pin to select a single SPI EPROM device, submits a read command at address 0x0000, and begins clocking data into the beginning of L1 instruction memory. A 16-, 24-bit addressable SPI-compatible EPROM must be used.

For each of the boot modes, a boot loading protocol is used to transfer program and data blocks from an external memory device to their specified memory locations. Multiple memory blocks may be loaded by any boot sequence. Once all blocks are loaded, Core A program execution commences from the start of L1 instruction SRAM (0xFFA0 0000). Core B remains in a held-off state until Bit 5 of SICA_SYSCR is cleared by Core A. After that, Core B will start execution at address 0xFF60 0000.

In addition, Bit 4 of the reset configuration register can be set by application code to bypass the normal boot sequence during a software reset. For this case, the processor jumps directly to the beginning of L1 instruction memory.

### INSTRUCTION SET DESCRIPTION

The Blackfin processor family assembly language instruction set employs an algebraic syntax that was designed for ease of coding and readability. The instructions have been specifically tuned to provide a flexible, densely encoded instruction set that compiles to a very small final memory size. The instruction set also provides fully featured multifunction instructions that allow the programmer to use many of the processor core resources in a single instruction. Coupled with many features more often seen on microcontrollers, this instruction set is very efficient when compiling C and C++ source code. In addition, the architecture supports both a user (algorithm/application code) and a supervisor (O/S kernel, device drivers, debuggers, ISRs) mode of operation—allowing multiple levels of access to core processor resources.

The assembly language, which takes advantage of the processor’s unique architecture, offers the following advantages:

- Seamlessly integrated DSP/CPU features are optimized for both 8-bit and 16-bit operations.
- A multi-issue load/store modified Harvard architecture, which supports two 16-bit MAC or four 8-bit ALU plus two load/store plus two pointer updates per cycle.
• All registers, I/O, and memory are mapped into a unified 4G byte memory space providing a simplified programming model.
• Microcontroller features, such as arbitrary bit and bit-field manipulation, insertion, and extraction; integer operations on 8-, 16-, and 32-bit data types; and separate user and kernel stack pointers.
• Code density enhancements, which include intermixing of 16-bit and 32-bit instructions (no mode switching, no code segregation). Frequently used instructions are encoded as 16-bits.

DEVELOPMENT TOOLS
Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)
For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs. The newest IDE, CrossCore Embedded Studio (CCES), is based on the Eclipse framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CCES Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CCES. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board
For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on “ezkit” or “ezextender”.

EZ-KIT Lite Evaluation Kits
For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user’s PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CCES or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CCES
Analog Devices offers software add-ins which seamlessly integrate with CCES to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CCES IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware
Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the Product Download area of the product web page.

Middleware Packages
Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

  • www.analog.com/ucos3
  • www.analog.com/ucfs
  • www.analog.com/ucusbd
  • www.analog.com/lwip

Algorithmic Modules
To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CCES and VisualDSP++. For more information visit www.analog.com and search on “Blackfin software modules” or “SHARC software modules”.

Designing an Emulator-Compatible DSP Board (Target)
For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor’s internal features via the processor’s TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP’s JTAG port to the emulator.
For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the EE-68: Analog Devices JTAG Emulation Technical Reference on the Analog Devices website (www.analog.com)—use site search on “EE-68.” This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

The following publications that describe the ADSP-BF561 processors (and related processors) can be ordered from any Analog Devices sales office or accessed electronically on our website:

- Getting Started With Blackfin Processors
- ADSP-BF561 Blackfin Processor Hardware Reference
- ADSP-BF53x/BF56x Blackfin Processor Programming Reference
- ADSP-BF561 Blackfin Processor Anomaly List

RELATED SIGNAL CHAINS

A signal chain is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Application Signal Chains page in the Circuits from the Lab® site (www.analog.com/circuits) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques
PIN DESCRIPTIONS

ADSP-BF561 pin definitions are listed in Table 8. In order to maintain maximum function and reduce package size and pin count, some pins have multiple functions. In cases where pin function is reconfigurable, the default state is shown in plain text, while alternate functionality is shown in italics.

All pins are three-stated during and immediately after reset, except the external memory interface, asynchronous memory control, and synchronous memory control pins. These pins are all driven high, with the exception of CLKOUT, which toggles at the system clock rate. However if BR is active, the memory pins are also three-stated.

All I/O pins have their input buffers disabled, with the exception of the pins that need pull-ups or pull-downs if unused, as noted in Table 8.

Table 8. Pin Descriptions

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Type</th>
<th>Function</th>
<th>Driver Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADDR25–2</td>
<td>O</td>
<td>Address Bus for Async/Sync Access</td>
<td>A</td>
</tr>
<tr>
<td>DATA31–0</td>
<td>I/O</td>
<td>Data Bus for Async/Sync Access</td>
<td>A</td>
</tr>
<tr>
<td>ABES3—0/SDQM3–0</td>
<td>O</td>
<td>Byte Enables/Data Masks for Async/Sync Access</td>
<td>A</td>
</tr>
<tr>
<td>BR</td>
<td>I</td>
<td>Bus Request (This pin should be pulled HIGH if not used.)</td>
<td>A</td>
</tr>
<tr>
<td>BG</td>
<td>O</td>
<td>Bus Grant</td>
<td>A</td>
</tr>
<tr>
<td>BGH</td>
<td>O</td>
<td>Bus Grant Hang</td>
<td>A</td>
</tr>
<tr>
<td>EBIU (ASYNC)</td>
<td>O</td>
<td>Bank Select</td>
<td>A</td>
</tr>
<tr>
<td>ARDY</td>
<td>I</td>
<td>Hardware Ready Control (This pin should be pulled HIGH if not used.)</td>
<td>A</td>
</tr>
<tr>
<td>AOE</td>
<td>O</td>
<td>Output Enable</td>
<td>A</td>
</tr>
<tr>
<td>AWE</td>
<td>O</td>
<td>Write Enable</td>
<td>A</td>
</tr>
<tr>
<td>ARE</td>
<td>O</td>
<td>Read Enable</td>
<td>A</td>
</tr>
<tr>
<td>EBIU (SDRAM)</td>
<td>O</td>
<td>Row Address Strobe</td>
<td>A</td>
</tr>
<tr>
<td>SRAS</td>
<td>O</td>
<td>Column Address Strobe</td>
<td>A</td>
</tr>
<tr>
<td>SCAS</td>
<td>O</td>
<td>Write Enable</td>
<td>A</td>
</tr>
<tr>
<td>SCE</td>
<td>O</td>
<td>Clock Enable</td>
<td>A</td>
</tr>
<tr>
<td>SCLK0/CLKOUT</td>
<td>O</td>
<td>Clock Output Pin 0</td>
<td>B</td>
</tr>
<tr>
<td>SCLK1</td>
<td>O</td>
<td>Clock Output Pin 1</td>
<td>B</td>
</tr>
<tr>
<td>SA10</td>
<td>O</td>
<td>SDRAM A10 Pin</td>
<td>A</td>
</tr>
<tr>
<td>SMS3–0</td>
<td>O</td>
<td>Bank Select</td>
<td>A</td>
</tr>
</tbody>
</table>
Table 8. Pin Descriptions (Continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Type</th>
<th>Function</th>
<th>Driver Type</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>PF/SPI/TIMER</td>
<td>I/O</td>
<td>Programmable Flag/Slave SPI Select/Timer</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>PF0/SPIS1/TMR0</td>
<td>I/O</td>
<td>Programmable Flag/SPI Select/Timer</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>PF1/SPISEL1/TMR1</td>
<td>I/O</td>
<td>Programmable Flag/SPI Select/Timer</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>PF2/SPISEL2/TMR2</td>
<td>I/O</td>
<td>Programmable Flag/SPI Select/Timer</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>PF3/SPISEL3/TMR3</td>
<td>I/O</td>
<td>Programmable Flag/SPI Select/Timer</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>PF4/SPISEL4/TMR4</td>
<td>I/O</td>
<td>Programmable Flag/SPI Select/Timer</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>PF5/SPISEL5/TMR5</td>
<td>I/O</td>
<td>Programmable Flag/SPI Select/Timer</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>PF6/SPISEL6/TMR6</td>
<td>I/O</td>
<td>Programmable Flag/SPI Select/Timer</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>PF7/SPISEL7/TMR7</td>
<td>I/O</td>
<td>Programmable Flag/SPI Select/Timer</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>PF8</td>
<td>I/O</td>
<td>Programmable Flag</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>PF9</td>
<td>I/O</td>
<td>Programmable Flag</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>PF10</td>
<td>I/O</td>
<td>Programmable Flag</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>PF11</td>
<td>I/O</td>
<td>Programmable Flag</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>PF12</td>
<td>I/O</td>
<td>Programmable Flag</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>PF13</td>
<td>I/O</td>
<td>Programmable Flag</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>PF14</td>
<td>I/O</td>
<td>Programmable Flag</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>PF15/EXT CLK</td>
<td>I/O</td>
<td>Programmable Flag/External Timer Clock Input</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>PPI0</td>
<td>I/O</td>
<td>PPI Data/Programmable Flag Pins</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>PPI0D15–8/PF47–40</td>
<td>I/O</td>
<td>PPI Data/Programmable Flag Pins</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>PPI0D7–0</td>
<td>I/O</td>
<td>PPI Data Pins</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>PPI0CLK</td>
<td>I</td>
<td>PPI Clock</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>PPI0SYNC1/TMR8</td>
<td>I/O</td>
<td>PPI Sync/Timer</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>PPI0SYNC2/TMR9</td>
<td>I/O</td>
<td>PPI Sync/Timer</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>PPI0SYNC3</td>
<td>I/O</td>
<td>PPI Sync</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>PPI1</td>
<td>I/O</td>
<td>PPI Data/Programmable Flag Pins</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>PPI1D15–8/PF39–32</td>
<td>I/O</td>
<td>PPI Data/Programmable Flag Pins</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>PPI1D7–0</td>
<td>I/O</td>
<td>PPI Data Pins</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>PPI1CLK</td>
<td>I</td>
<td>PPI Clock</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>PPI1SYNC1/TMR10</td>
<td>I/O</td>
<td>PPI Sync/Timer</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>PPI1SYNC2/TMR11</td>
<td>I/O</td>
<td>PPI Sync/Timer</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>PPI1SYNC3</td>
<td>I/O</td>
<td>PPI Sync</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>SPORT0</td>
<td>I/O</td>
<td>Sport0 Receive Serial Clock/Programmable Flag</td>
<td>D</td>
<td></td>
</tr>
<tr>
<td>RSCLK/PF28</td>
<td>I/O</td>
<td>Sport0 Receive Serial Clock/Programmable Flag</td>
<td>D</td>
<td></td>
</tr>
<tr>
<td>RFS0/PF19</td>
<td>I/O</td>
<td>Sport0 Receive Frame Sync/Programmable Flag</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>DROPRI</td>
<td>I</td>
<td>Sport0 Receive Data Primary</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>DROSEC/PF20</td>
<td>I/O</td>
<td>Sport0 Receive Data Secondary/Programmable Flag</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>TSCLK/PF29</td>
<td>I/O</td>
<td>Sport0 Transmit Serial Clock/Programmable Flag</td>
<td>D</td>
<td></td>
</tr>
<tr>
<td>TSF0/PF16</td>
<td>I/O</td>
<td>Sport0 Transmit Frame Sync/Programmable Flag</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>DT0PRI/PF18</td>
<td>I/O</td>
<td>Sport0 Transmit Data Primary/Programmable Flag</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>DT0SEC/PF17</td>
<td>I/O</td>
<td>Sport0 Transmit Data Secondary/Programmable Flag</td>
<td>C</td>
<td></td>
</tr>
</tbody>
</table>
Table 8. Pin Descriptions (Continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Type</th>
<th>Function</th>
<th>Driver Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPORT1</td>
<td>I/O</td>
<td>Sport1 Receive Serial Clock/Programmable Flag</td>
<td>D</td>
</tr>
<tr>
<td>RSCLK1/PF30</td>
<td>I/O</td>
<td>Sport1 Receive Frame Sync/Programmable Flag</td>
<td>C</td>
</tr>
<tr>
<td>RF1/PF24</td>
<td>I/O</td>
<td>Sport1 Receive Data Primary</td>
<td></td>
</tr>
<tr>
<td>DR1PRI</td>
<td>I</td>
<td>Sport1 Receive Data Secondary/Programmable Flag</td>
<td>C</td>
</tr>
<tr>
<td>DR1SEC/PF25</td>
<td>I/O</td>
<td>Sport1 Transmit Serial Clock/Programmable Flag</td>
<td>D</td>
</tr>
<tr>
<td>TSCLK1/PF31</td>
<td>I/O</td>
<td>Sport1 Transmit Frame Sync/Programmable Flag</td>
<td>C</td>
</tr>
<tr>
<td>TFS1/PF21</td>
<td>I/O</td>
<td>Sport1 Transmit Data Primary/Programmable Flag</td>
<td>C</td>
</tr>
<tr>
<td>DT1PRI/PF23</td>
<td>I/O</td>
<td>Sport1 Transmit Data Secondary/Programmable Flag</td>
<td>C</td>
</tr>
<tr>
<td>SPI</td>
<td>I/O</td>
<td>Master Out Slave In</td>
<td>C</td>
</tr>
<tr>
<td>MOSI</td>
<td>I/O</td>
<td>Master In Slave Out</td>
<td>C</td>
</tr>
<tr>
<td>MISO</td>
<td>I/O</td>
<td>Master In Slave Out (This pin should be pulled HIGH through a 4.7 kΩ resistor if booting via the SPI port.)</td>
<td></td>
</tr>
<tr>
<td>SCK</td>
<td>I/O</td>
<td>SPI Clock</td>
<td>D</td>
</tr>
<tr>
<td>UART</td>
<td>I/O</td>
<td>UART Receive/Programmable Flag</td>
<td>C</td>
</tr>
<tr>
<td>RX/PF27</td>
<td>I/O</td>
<td>UART Transmit/Programmable Flag</td>
<td>C</td>
</tr>
<tr>
<td>UART</td>
<td>I/O</td>
<td>UART Transmit/Programmable Flag</td>
<td>C</td>
</tr>
<tr>
<td>JTAG</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EMU</td>
<td>O</td>
<td>Emulation Output</td>
<td>C</td>
</tr>
<tr>
<td>TCK</td>
<td>I</td>
<td>JTAG Clock</td>
<td></td>
</tr>
<tr>
<td>TDO</td>
<td>O</td>
<td>JTAG Serial Data Out</td>
<td>C</td>
</tr>
<tr>
<td>TDI</td>
<td>I</td>
<td>JTAG Serial Data In</td>
<td></td>
</tr>
<tr>
<td>TMS</td>
<td>I</td>
<td>JTAG Mode Select</td>
<td></td>
</tr>
<tr>
<td>TRST</td>
<td>I</td>
<td>JTAG Reset (This pin should be pulled LOW if JTAG is not used.)</td>
<td></td>
</tr>
<tr>
<td>Clock</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLKIN</td>
<td>I</td>
<td>Clock/Crystal Input (This pin needs to be at a level or clocking.)</td>
<td></td>
</tr>
<tr>
<td>XTAL</td>
<td>O</td>
<td>Crystal Connection</td>
<td></td>
</tr>
<tr>
<td>Mode Controls</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RESET</td>
<td>I</td>
<td>Reset (This pin is always active during core power-on.)</td>
<td></td>
</tr>
<tr>
<td>NMI0</td>
<td>I</td>
<td>Nonmaskable Interrupt Core A (This pin should be pulled LOW when not used.)</td>
<td></td>
</tr>
<tr>
<td>NMI1</td>
<td>I</td>
<td>Nonmaskable Interrupt Core B (This pin should be pulled LOW when not used.)</td>
<td></td>
</tr>
<tr>
<td>BMODE1–0</td>
<td>I</td>
<td>Boot Mode Strap (These pins must be pulled to the state required for the desired boot mode.)</td>
<td></td>
</tr>
<tr>
<td>SLEEP</td>
<td>O</td>
<td>Sleep</td>
<td></td>
</tr>
<tr>
<td>BYPASS</td>
<td>I</td>
<td>PLL BYPASS Control (Pull-up or pull-down Required.)</td>
<td></td>
</tr>
<tr>
<td>Voltage Regulator</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_Ext1–0</td>
<td>O</td>
<td>External FET Drive</td>
<td></td>
</tr>
<tr>
<td>Supplies</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VDDINT</td>
<td>P</td>
<td>Power Supply</td>
<td></td>
</tr>
<tr>
<td>VDDINT</td>
<td>P</td>
<td>Power Supply</td>
<td></td>
</tr>
<tr>
<td>GND</td>
<td>G</td>
<td>Power Supply Return</td>
<td></td>
</tr>
<tr>
<td>No Connection</td>
<td>NC</td>
<td>NC</td>
<td></td>
</tr>
</tbody>
</table>

1 Refer to Figure 32 to Figure 36.
## OPERATING CONDITIONS

Table 9 and Table 10 describe the timing requirements for the ADSP-BF561 clocks (tCCLK = 1/fCCLK). Take care in selecting MSEL, SSEL, and CSEL ratios so as not to exceed the maximum core clock, system clock, and Voltage Controlled Oscillator (VCO) operating frequencies, as described in Absolute Maximum Ratings. Table 11 describes phase-locked loop operating conditions.

### Table 9. Core Clock (CCLK) Requirements—500 MHz and 533 MHz Speed Grade Models

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Nominal</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{CCLK}$</td>
<td>CCLK Frequency (VDDINT = 1.235 V minimum)</td>
<td>350</td>
<td></td>
<td>533</td>
<td>MHz</td>
</tr>
<tr>
<td>$f_{CCLK}$</td>
<td>CCLK Frequency (VDDINT = 1.1875 V minimum)</td>
<td>300</td>
<td></td>
<td>500</td>
<td>MHz</td>
</tr>
<tr>
<td>$f_{CCLK}$</td>
<td>CCLK Frequency (VDDINT = 1.045 V minimum)</td>
<td>250</td>
<td></td>
<td>444</td>
<td>MHz</td>
</tr>
<tr>
<td>$f_{CCLK}$</td>
<td>CCLK Frequency (VDDINT = 0.95 V minimum)</td>
<td></td>
<td></td>
<td>350</td>
<td>MHz</td>
</tr>
<tr>
<td>$f_{CCLK}$</td>
<td>CCLK Frequency (VDDINT = 0.855 V minimum)</td>
<td></td>
<td></td>
<td>300</td>
<td>MHz</td>
</tr>
<tr>
<td>$f_{CCLK}$</td>
<td>CCLK Frequency (VDDINT = 0.8 V minimum)</td>
<td></td>
<td></td>
<td>250</td>
<td>MHz</td>
</tr>
</tbody>
</table>

1 See Ordering Guide.
2 Does not apply to 500 MHz speed grade models.
Table 10. Core Clock (CCLK) Requirements—600 MHz Speed Grade Models

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_{\text{CCLK}} )</td>
<td>600</td>
<td>MHz</td>
</tr>
<tr>
<td>( f_{\text{CCLK}} )</td>
<td>533</td>
<td>MHz</td>
</tr>
<tr>
<td>( f_{\text{CCLK}} )</td>
<td>500</td>
<td>MHz</td>
</tr>
<tr>
<td>( f_{\text{CCLK}} )</td>
<td>444</td>
<td>MHz</td>
</tr>
<tr>
<td>( f_{\text{CCLK}} )</td>
<td>350</td>
<td>MHz</td>
</tr>
<tr>
<td>( f_{\text{CCLK}} )</td>
<td>300</td>
<td>MHz</td>
</tr>
<tr>
<td>( f_{\text{CCLK}} )</td>
<td>250</td>
<td>MHz</td>
</tr>
</tbody>
</table>

1 See Ordering Guide.
2 External voltage regulator required to ensure proper operation at 600 MHz.

Table 11. Phase-Locked Loop Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage Controlled Oscillator (VCO) Frequency</td>
<td>50</td>
<td>Maximum</td>
<td>f_{\text{CCLK}} MHz</td>
</tr>
</tbody>
</table>

Table 12. System Clock (SCLK) Requirements

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Max ( V_{\text{DEXT}} = 2.5V/3.3V )</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_{\text{SCLK}} )</td>
<td>133²</td>
<td>MHz</td>
</tr>
<tr>
<td>( f_{\text{SCLK}} )</td>
<td>100</td>
<td>MHz</td>
</tr>
</tbody>
</table>

1 \( t_{\text{SCLK}} = 1/f_{\text{SCLK}} \) must be greater than or equal to \( t_{\text{CCLK}} \).
2 Rounded number. Guaranteed to \( t_{\text{SCLK}} = 7.5 \) ns. See Table 19.

ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{OH}} )</td>
<td>( V_{\text{DEXT}} = 3.0 ) V, ( I_{\text{OH}} = -0.5 ) mA</td>
<td>2.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{OL}} )</td>
<td>( V_{\text{DEXT}} = 3.0 ) V, ( I_{\text{OL}} = 2.0 ) mA</td>
<td>0.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( I_{\text{IH}} )</td>
<td>( V_{\text{DEXT}} ) = Maximum, ( V_{\text{IN}} = V_{\text{DD}} ) Maximum</td>
<td>10.0</td>
<td></td>
<td></td>
<td>( \mu ) A</td>
</tr>
<tr>
<td>( I_{\text{IHP}} )</td>
<td>( V_{\text{DEXT}} ) = Maximum, ( V_{\text{IN}} = 0 ) V</td>
<td>10.0</td>
<td></td>
<td></td>
<td>( \mu ) A</td>
</tr>
<tr>
<td>( I_{\text{IL}} )</td>
<td>( V_{\text{DEXT}} ) = Maximum, ( V_{\text{IN}} = 0 ) V</td>
<td>10.0</td>
<td></td>
<td></td>
<td>( \mu ) A</td>
</tr>
<tr>
<td>( C_{\text{IN}} )</td>
<td>( f_{\text{IN}} = 1 ) MHz, ( T_{\text{AMB}} = 25^\circ ) C, ( V_{\text{IN}} = 2.5 ) V</td>
<td>4</td>
<td>8²</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>( I_{\text{SLEEP/RESTART}} )</td>
<td>( V_{\text{DEXT}} ) Current in Hibernate Mode</td>
<td>50</td>
<td></td>
<td></td>
<td>( \mu ) A</td>
</tr>
<tr>
<td>( I_{\text{DDLEW}} )</td>
<td>( V_{\text{DEXT}} ) Current in Deep Sleep Mode</td>
<td>70</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( I_{\text{DDLEW}} )</td>
<td>( V_{\text{DEXT}} ) Current in Deep Sleep Mode</td>
<td>127</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( I_{\text{DDLEW}} )</td>
<td>( V_{\text{DEXT}} ) Current in Deep Sleep Mode</td>
<td>660</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( I_{\text{DDLEW}} )</td>
<td>( V_{\text{DEXT}} ) Current in Deep Sleep Mode</td>
<td>818</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

1 Applies to output and bidirectional pins.
2 Applies to input pins except JTAG inputs.
3 Applies to JTAG input pins (TCK, TDI, TMS, TRST).
4 Absolute value.
5 Applies to three-stateable pins.
6 Applies to all signal pins.
7 Guaranteed, but not tested.
8 CLKIN must be tied to \( V_{\text{DEXT}} \) or GND during hibernate.
10 Both cores executing 75% dual MAC, 25% ADD instructions with moderate data bus activity.
System designers should refer to *Estimating Power for the ADSP-BF561 (EE-293)*, which provides detailed information for optimizing designs for lowest power. All topics discussed in this section are described in detail in EE-293. Total power dissipation has two components:

1. Static, including leakage current
2. Dynamic, due to transistor switching characteristics

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor activity. *Electrical Characteristics* shows the current dissipation for internal circuitry ($V_{\text{Dmax}}$).

**ABSOLUTE MAXIMUM RATINGS**

Stresses greater than those listed in Table 13 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 13. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Internal (Core) Supply Voltage ($V_{\text{DDINT}}$)</td>
<td>$-0.3 \text{ V to } +1.42 \text{ V}$</td>
</tr>
<tr>
<td>External (I/O) Supply Voltage ($V_{\text{DDEXT}}$)</td>
<td>$-0.5 \text{ V to } +3.8 \text{ V}$</td>
</tr>
<tr>
<td>Input Voltage$^1$</td>
<td>$-0.5 \text{ V to } +3.8 \text{ V}$</td>
</tr>
<tr>
<td>Output Voltage Swing</td>
<td>$-0.5 \text{ V to } V_{\text{DDINT}} + 0.5 \text{ V}$</td>
</tr>
<tr>
<td>Load Capacitance$^2$</td>
<td>200 pF</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>$-65^\circ\text{C to } +150^\circ\text{C}$</td>
</tr>
<tr>
<td>Junction Temperature Under Bias</td>
<td>125°C</td>
</tr>
</tbody>
</table>

$^1$ Applies to 100% transient duty cycle. For other duty cycles see Table 14.

$^2$ For proper SDRAM controller operation, the maximum load capacitance is 50 pF (at 3.3 V) or 30 pF (at 2.5 V) for ADDR19–1, DATA15–0, ABE1–0/SDQM1–0, CLKOUT, SCKE, SA10, SRAS, SCAS, SWE, and SMS.

Table 14. Maximum Duty Cycle for Input Transient Voltage$^1$

<table>
<thead>
<tr>
<th>$V_{\text{in}}$ Min (V)</th>
<th>$V_{\text{in}}$ Max (V)$^2$</th>
<th>Maximum Duty Cycle</th>
</tr>
</thead>
<tbody>
<tr>
<td>$-0.50$</td>
<td>3.80</td>
<td>100%</td>
</tr>
<tr>
<td>$-0.70$</td>
<td>4.00</td>
<td>40%</td>
</tr>
<tr>
<td>$-0.80$</td>
<td>4.10</td>
<td>25%</td>
</tr>
<tr>
<td>$-0.90$</td>
<td>4.20</td>
<td>15%</td>
</tr>
<tr>
<td>$-1.00$</td>
<td>4.30</td>
<td>10%</td>
</tr>
</tbody>
</table>

$^1$ Applies to all signal pins with the exception of CLKN, XTAL, VROUT1–0.

$^2$ Only one of the listed options can apply to a particular design.
TIMING SPECIFICATIONS

Clock and Reset Timing

Table 15 and Figure 7 describe clock and reset operations. Per Absolute Maximum Ratings, combinations of CLKIN and clock multipliers must not result in core/system clocks exceeding the maximum limits allowed for the processor, including system clock restrictions related to supply voltage.

Table 15. Clock and Normal Reset Timing

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>tCKIN</td>
<td>25.0</td>
<td>100.0</td>
<td>ns</td>
</tr>
<tr>
<td>tCKINL</td>
<td>10.0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tCKINH</td>
<td>10.0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tWRST</td>
<td>11 × tckin</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

1 If DF bit in PLL_CTL register is set, tCLKIN is divided by two before going to PLL, then the tCLKIN maximum period is 50 ns and the tCLKIN minimum period is 12.5 ns.
2 Applies to PLL bypass mode and PLL nonbypass mode.
3 Combinations of the CLKIN frequency and the PLL clock multiplier must not exceed the allowed fVCO, fCCLK, and fSCLK settings discussed in Table 9 through Table 12.
4 Applies after power-up sequence is complete. See Table 16 and Figure 8 for power-up reset timing.

Figure 7. Clock and Normal Reset Timing

Table 16. Power-Up Reset Timing

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>tREST_IN_PWR</td>
<td>3500 × tckin</td>
<td></td>
<td>μs</td>
</tr>
</tbody>
</table>

Figure 8. Power-Up Reset Timing
Asynchronous Memory Read Cycle Timing

Table 17. Asynchronous Memory Read Cycle Timing

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Timing Requirements</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tSDAT</td>
<td>DATA31–0 Setup Before CLKOUT</td>
<td>2.1</td>
<td>ns</td>
</tr>
<tr>
<td>tHDAT</td>
<td>DATA31–0 Hold After CLKOUT</td>
<td>0.8</td>
<td>ns</td>
</tr>
<tr>
<td>tSARDY</td>
<td>ARDY Setup Before CLKOUT</td>
<td>4.0</td>
<td>ns</td>
</tr>
<tr>
<td>tHARDY</td>
<td>ARDY Hold After CLKOUT</td>
<td>0.0</td>
<td>ns</td>
</tr>
<tr>
<td><strong>Switching Characteristics</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tDO</td>
<td>Output Delay After CLKOUT&lt;sup&gt;1&lt;/sup&gt;</td>
<td>6.0</td>
<td>ns</td>
</tr>
<tr>
<td>tHO</td>
<td>Output Hold After CLKOUT&lt;sup&gt;1&lt;/sup&gt;</td>
<td>0.8</td>
<td>ns</td>
</tr>
</tbody>
</table>

<sup>1</sup>Output pins include AMS3–0, ABE3–0, ADDR25–2, AOE, ARE.

![Figure 9. Asynchronous Memory Read Cycle Timing](image-url)
Asynchronous Memory Write Cycle Timing

Table 18. Asynchronous Memory Write Cycle Timing

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Timing Requirements</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{SARDY} )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ARDY Setup Before CLKOUT</td>
<td>4.0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{HARDY} )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ARDY Hold After CLKOUT</td>
<td>0.0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td><strong>Switching Characteristics</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{DDAT} )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DATA31–0 Disable After CLKOUT</td>
<td></td>
<td>6.0</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{ENDAT} )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DATA31–0 Enable After CLKOUT</td>
<td>1.0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{DO} )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Delay After CLKOUT</td>
<td></td>
<td>6.0</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{HO} )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Hold After CLKOUT (^1)</td>
<td>0.8</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

\(^1\) Output pins include AMS3–0, ABE3–0, ADDR25–2, DATA31–0, AOE, AWE.

Figure 10. Asynchronous Memory Write Cycle Timing
## SDRAM Interface Timing

Table 19. SDRAM Interface Timing

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Timing Requirements</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{SDAT}$</td>
<td>DATA Setup Before CLKOUT</td>
<td>1.5</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{SDAT}$</td>
<td>DATA Hold After CLKOUT</td>
<td>0.8</td>
<td>ns</td>
</tr>
<tr>
<td><strong>Switching Characteristics</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{SCAD}$</td>
<td>Command, ADDR, Data Delay After CLKOUT&lt;sup&gt;1&lt;/sup&gt;</td>
<td>4.0</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{SCAD}$</td>
<td>Command, ADDR, Data Hold After CLKOUT&lt;sup&gt;1&lt;/sup&gt;</td>
<td>0.8</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{SDAT}$</td>
<td>Data Disable After CLKOUT</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{SDAT}$</td>
<td>Data Enable After CLKOUT</td>
<td>1.0</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{SCLK}$</td>
<td>CLKOUT Period</td>
<td>7.5</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{SCLKH}$</td>
<td>CLKOUT Width High</td>
<td>2.5</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{SCLKL}$</td>
<td>CLKOUT Width Low</td>
<td>2.5</td>
<td>ns</td>
</tr>
</tbody>
</table>

<sup>1</sup> Command pins include: SRAS, SCAS, SWE, SDQM, SMS3–0, SA10, SCKE.

![Figure 11. SDRAM Interface Timing](image-url)
## External Port Bus Request and Grant Cycle Timing

Table 20 and Figure 12 describe external port bus request and bus grant operations.

### Table 20. External Port Bus Request and Grant Cycle Timing

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Timing Requirements</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_{BS}</td>
<td>BR Asserted to CLKOUT High Setup</td>
<td>4.6</td>
<td>ns</td>
</tr>
<tr>
<td>t_{BH}</td>
<td>CLKOUT High to BR Deasserted Hold Time</td>
<td>0.0</td>
<td>ns</td>
</tr>
<tr>
<td><strong>Switching Characteristics</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_{SD}</td>
<td>CLKOUT Low to AMSx, Address and ARE/AWE Disable</td>
<td>4.5</td>
<td>ns</td>
</tr>
<tr>
<td>t_{SE}</td>
<td>CLKOUT Low to AMSx, Address and ARE/AWE Enable</td>
<td>4.5</td>
<td>ns</td>
</tr>
<tr>
<td>t_{SC}</td>
<td>CLKOUT High to BG Asserted Setup</td>
<td>3.6</td>
<td>ns</td>
</tr>
<tr>
<td>t_{SH}</td>
<td>CLKOUT High to BG Deasserted Hold Time</td>
<td>3.6</td>
<td>ns</td>
</tr>
<tr>
<td>t_{SHH}</td>
<td>CLKOUT High to BGH Asserted Setup</td>
<td>3.6</td>
<td>ns</td>
</tr>
<tr>
<td>t_{SHH}</td>
<td>CLKOUT High to BGH Deasserted Hold Time</td>
<td>3.6</td>
<td>ns</td>
</tr>
</tbody>
</table>

1 These are preliminary timing parameters that are based on worst-case operating conditions.
2 The pad loads for these timing parameters are 20 pF.

![Figure 12. External Port Bus Request and Grant Cycle Timing](image-url)
Parallel Peripheral Interface Timing

Table 21, and Figure 13 through Figure 18, describe default parallel peripheral interface operations.

Table 21. Parallel Peripheral Interface Timing

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timing Requirements</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{PCLKW} )</td>
<td>5.0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{PCLK} )</td>
<td>13.3</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{SFSPE} )</td>
<td>4.0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{HFSPE} )</td>
<td>1.0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{SDRPE} )</td>
<td>3.5</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{HDRPE} )</td>
<td>2.0</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

Switching Characteristics—GP Output and Frame Capture Modes

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{DFSPE} )</td>
<td>8.0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{HOFSPE} )</td>
<td>1.7</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{DDTPE} )</td>
<td>8.0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{HDTPE} )</td>
<td>2.0</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

1 For PPI modes that use an internally generated frame sync, the PPIxCLK frequency cannot exceed \( f_{SCLK}/2 \). For modes with no frame syncs or external frame syncs, \( PPIxCLK \) cannot exceed 75 MHz and \( f_{SCLK} \) should be equal to or greater than PPIxCLK.

2 Applies when PLL_CTL bit 4 is cleared. See Figure 15 and Figure 18.

Figure 13. PPI GP Rx Mode with Internal Frame Sync Timing

Figure 14. PPI GP Rx Mode with External Frame Sync Timing (PLL_CTL Bit 4 = 1)
Figure 15. PPI GP Rx Mode with External Frame Sync Timing (PLL_CTL Bit 4 = 0)

Figure 16. PPI GP Tx Mode with Internal Frame Sync Timing

Figure 17. PPI GP Tx Mode with External Frame Sync Timing (PLL_CTL Bit 4 = 1)
Figure 18. PPI GP Tx Mode with External Frame Sync Timing (PLL_CTL Bit 4 = 0)
### Serial Ports

Table 22 through Table 25 and Figure 19 through Figure 22 describe Serial Port operations.

#### Table 22. Serial Ports—External Clock

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Timing Requirements</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{SFS} ) TFSx/RFSx Setup Before TSCLKx/RSCLKx</td>
<td>3.0 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{HFS} ) TFSx/RFSx Hold After TSCLKx/RSCLKx</td>
<td>3.0 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{DSRE} ) Receive Data Setup Before RSCLKx</td>
<td>3.0 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{HDS} ) Receive Data Hold After RSCLKx</td>
<td>3.0 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{ULW} ) TSCLKx/RSCLKx Width</td>
<td>4.5 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{UHI} ) TSCLKx/RSCLKx Period</td>
<td>15.0 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{SUDE} ) Start-Up Delay From SPORT Enable To First External TFSx</td>
<td>( 4 \times t_{SCLKE} ) ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{SUDE} ) Start-Up Delay From SPORT Enable To First External RFSx</td>
<td>( 4 \times t_{SCLKE} ) ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Switching Characteristics</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{DFS} ) TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)</td>
<td>10.0 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{HOF} ) TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)</td>
<td>–1.0 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{DTE} ) Transmit Data Delay After TSCLKx</td>
<td>10.0 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{HDT} ) Transmit Data Hold After TSCLKx</td>
<td>–2.0 ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1 Referenced to sample edge.

2 Verified in design but untested. After being enabled, the serial port requires external clock pulses—before the first external frame sync edge—to initialize the serial port.

3 Referenced to drive edge.

#### Table 23. Serial Ports—Internal Clock

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Timing Requirements</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{IFS} ) TFSx/RFSx Setup Before TSCLKx/RSCLKx</td>
<td>8.0 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{HFS} ) TFSx/RFSx Hold After TSCLKx/RSCLKx</td>
<td>–2.0 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{DSI} ) Receive Data Setup Before RSCLKx</td>
<td>6.0 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{DS} ) Receive Data Hold After RSCLKx</td>
<td>0.0 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Switching Characteristics</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{DFS} ) TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)</td>
<td>3.0 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{HOF} ) TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)</td>
<td>–1.0 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{DTE} ) Transmit Data Delay After TSCLKx</td>
<td>3.0 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{HDT} ) Transmit Data Hold After TSCLKx</td>
<td>–2.0 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{ULW} ) TSCLKx/RSCLKx Width</td>
<td>4.5 ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1 Referenced to sample edge.

2 Referenced to drive edge.
Figure 19. Serial Ports

Figure 20. Serial Port Start Up with External Clock and Frame Sync
### Table 24. Serial Ports—Enable and Three-State

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Switching Characteristics</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{DTENE} )</td>
<td>Data Enable Delay from External TSCLKx (^1)</td>
<td>0 ns</td>
<td>0 ns</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{DDETTE} )</td>
<td>Data Disable Delay from External TSCLKx (^1, 2, 3)</td>
<td>10.0 ns</td>
<td>10.0 ns</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{DTENI} )</td>
<td>Data Enable Delay from Internal TSCLKx (^1)</td>
<td>(-2.0) ns</td>
<td>(-2.0) ns</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{DDETII} )</td>
<td>Data Disable Delay from Internal TSCLKx (^1, 2, 3)</td>
<td>3.0 ns</td>
<td>3.0 ns</td>
<td>ns</td>
</tr>
</tbody>
</table>

1 Referenced to drive edge.
2 Applicable to multichannel mode only.
3 TSCLKx is tied to RSCLKx.

![Figure 21. Enable and Three-State](image-url)
### Table 25. External Late Frame Sync

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switching Characteristics</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{DDTLE} ) Data Delay from</td>
<td></td>
<td>10.0</td>
<td>ns</td>
</tr>
<tr>
<td>Late External TFSx or External</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RFSx in multichannel mode with</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MFD = 01, 2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{DTENLFS} ) Data Enable</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>from Late FS or in multichannel</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>mode with MFD = 01, 2</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1. In multichannel mode, TFSx enable and TFSx valid follow \( t_{DDTLE} \) and \( t_{DTENLFS} \).
2. If external RFSx/TFSx setup to \( RSCLKx/TSCLKx > t_{SCLK}/2 \), then \( t_{DDTLE} \) and \( t_{DTENLFS} \) apply; otherwise \( t_{DDTLE} \) and \( t_{DTENLFS} \) apply.

---

**Figure 22. External Late Frame Sync**

EXTERNAL RFSx IN MULTI-CHANNEL MODE

- 
<table>
<thead>
<tr>
<th>DRIVE</th>
<th>SAMPLE</th>
<th>DRIVE</th>
</tr>
</thead>
<tbody>
<tr>
<td>EDGE</td>
<td>EDGE</td>
<td>EDGE</td>
</tr>
</tbody>
</table>

RFSx

- 
  | t\(_{DDTLE}\) |

DTx

- 
  | 1ST BIT |

LATE EXTERNAL TFSx

- 
<table>
<thead>
<tr>
<th>DRIVE</th>
<th>SAMPLE</th>
<th>DRIVE</th>
</tr>
</thead>
<tbody>
<tr>
<td>EDGE</td>
<td>EDGE</td>
<td>EDGE</td>
</tr>
</tbody>
</table>

TSCLKx

- 
  | t\(_{DDTLE}\) |

DTx

- 
  | 1ST BIT |
Serial Peripheral Interface (SPI) Port—Master Timing

Table 26 and Figure 23 describe SPI port master operations.

Table 26. Serial Peripheral Interface (SPI) Port—Master Timing

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timing Requirements</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{SSPIDM}$ Data Input Valid to SCK Edge (Data Input Setup)</td>
<td>7.5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{HSPIDM}$ SCK Sampling Edge to Data Input Invalid</td>
<td>-1.5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Switching Characteristics</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{SCLK}$ SPISELx Low to First SCK Edge</td>
<td>$2 \times t_{SCLK} - 1.5$</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{SCLK}$ Serial Clock High Period</td>
<td>$2 \times t_{SCLK} - 1.5$</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{SPICL}$ Serial Clock Low Period</td>
<td>$2 \times t_{SCLK} - 1.5$</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{SPICLK}$ Serial Clock Period</td>
<td>$4 \times t_{SCLK} - 1.5$</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{SCLK}$ Last SCK Edge to SPISELx High</td>
<td>$2 \times t_{SCLK} - 1.5$</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{SPITDM}$ Sequential Transfer Delay</td>
<td>$2 \times t_{SCLK} - 1.5$</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{DDSPIDM}$ SCK Edge to Data Out Valid (Data Out Delay)</td>
<td>0</td>
<td>6</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{HSPIDM}$ SCK Edge to Data Out Invalid (Data Out Hold)</td>
<td>-1.0</td>
<td>+4.0</td>
<td>ns</td>
</tr>
</tbody>
</table>

Figure 23. Serial Peripheral Interface (SPI) Port—Master Timing
Table 27 and Figure 24 describe SPI port slave operations.

Table 27. Serial Peripheral Interface (SPI) Port—Slave Timing

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Timing Requirements</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t\text{SPICHS} Serial Clock High Period</td>
<td>$2 \times t\text{SCLK} - 1.5$</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t\text{SPICLS} Serial Clock Low Period</td>
<td>$2 \times t\text{SCLK} - 1.5$</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t\text{SPICLK} Serial Clock Period</td>
<td>$4 \times t\text{SCLK}$</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t\text{HDS} Last SCK Edge to SPISS Not Asserted</td>
<td>$2 \times t\text{SCLK} - 1.5$</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t\text{SPITDS} Sequential Transfer Delay</td>
<td>$2 \times t\text{SCLK} - 1.5$</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t\text{SDSCI} SPISS Assertion to First SCK Edge</td>
<td>$2 \times t\text{SCLK} - 1.5$</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t\text{SPID} Data Input Valid to SCK Edge (Data Input Setup)</td>
<td>1.6 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t\text{SPPID} SCK Sampling Edge to Data Input Invalid</td>
<td>1.6 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Switching Characteristics</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t\text{DSOE} SPISS Assertion to Data Out Active</td>
<td>0 ns</td>
<td>8 ns</td>
<td></td>
</tr>
<tr>
<td>t\text{DSDE} SPISS Deassertion to Data High Impedance</td>
<td>0 ns</td>
<td>8 ns</td>
<td></td>
</tr>
<tr>
<td>t\text{DSPID} SCK Edge to Data Out Valid (Data Out Delay)</td>
<td>0 ns</td>
<td>10 ns</td>
<td></td>
</tr>
<tr>
<td>t\text{DSPID} SCK Edge to Data Out Invalid (Data Out Hold)</td>
<td>0 ns</td>
<td>10 ns</td>
<td></td>
</tr>
</tbody>
</table>

Figure 24. Serial Peripheral Interface (SPI) Port—Slave Timing
**Universal Asynchronous Receiver Transmitter (UART) Port—Receive and Transmit Timing**

Figure 25 describes UART port receive and transmit operations. The maximum baud rate is SCLK/16. As shown in Figure 25, there is some latency between the generation internal UART interrupts and the external data operations. These latencies are negligible at the data transmission rates for the UART.

![Figure 25. UART Port—Receive and Transmit Timing](image-url)
Programmable Flags Cycle Timing

Table 28 and Figure 26 describe programmable flag operations.

Table 28. Programmable Flags Cycle Timing

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Timing Requirement</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{WFI} ) Flag Input Pulse Width</td>
<td>( t_{SCLK} + 1 )</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td><strong>Switching Characteristic</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{DFO} ) Flag Output Delay from CLKOUT Low</td>
<td>6</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

Figure 26. Programmable Flags Cycle Timing
Timer Clock Timing

Table 29 and Figure 27 describe timer clock timing.

Table 29. Timer Clock Timing

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switching Characteristic</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tTODP</td>
<td>Timer Output Update Delay After PPI_CLK High</td>
<td></td>
<td>12</td>
</tr>
</tbody>
</table>

Figure 27. Timer Clock Timing

Timer Cycle Timing

Table 30 and Figure 28 describe timer expired operations. The input signal is asynchronous in "width capture mode" and "external clock mode" and has an absolute maximum input frequency of fSCLK/2 MHz.

Table 30. Timer Cycle Timing

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timing Characteristics</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tWL</td>
<td>Timer Pulse Width Low$^1$</td>
<td></td>
<td>$1 \times t_{SCLK}$</td>
</tr>
<tr>
<td>tWH</td>
<td>Timer Pulse Width High$^1$</td>
<td></td>
<td>$1 \times t_{SCLK}$</td>
</tr>
<tr>
<td>tTIS</td>
<td>Timer Input Setup Time Before CLKOUT Low$^2$</td>
<td></td>
<td>6.5</td>
</tr>
<tr>
<td>tTIH</td>
<td>Timer Input Hold Time After CLKOUT Low$^2$</td>
<td></td>
<td>1.5</td>
</tr>
<tr>
<td>Switching Characteristics</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tHTO</td>
<td>Timer Pulse Width Output</td>
<td></td>
<td>$1 \times t_{SCLK}$</td>
</tr>
<tr>
<td>tTOD</td>
<td>Timer Output Update Delay After CLKOUT High</td>
<td></td>
<td>$(2^{32}-1) \times t_{SCLK}$</td>
</tr>
</tbody>
</table>

$^1$The minimum pulse widths apply for TMRx input pins in width capture and external clock modes. They also apply to the PF1 or PPI_CLK input pins in PWM output mode.

$^2$Either a valid setup and hold time or a valid pulse width is sufficient. There is no need to resynchronize programmable flag inputs.

Figure 28. Timer PWM_OUT Cycle Timing
JTAG Test and Emulation Port Timing

Table 31, Figure 29, and Figure 30 describe JTAG port operations.

Table 31. JTAG Port Timing

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Timing Requirements</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t\textsubscript{TCK}</td>
<td>TCK Period</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>t\textsubscript{STAP}</td>
<td>TDI, TMS Setup Before TCK High</td>
<td>4</td>
<td>ns</td>
</tr>
<tr>
<td>t\textsubscript{HTAP}</td>
<td>TDI, TMS Hold After TCK High</td>
<td>4</td>
<td>ns</td>
</tr>
<tr>
<td>t\textsubscript{SSYS}</td>
<td>System Inputs Setup Before TCK High(^1)</td>
<td>4</td>
<td>ns</td>
</tr>
<tr>
<td>t\textsubscript{HSYS}</td>
<td>System Inputs Hold After TCK High(^1)</td>
<td>5</td>
<td>ns</td>
</tr>
<tr>
<td>t\textsubscript{TRSTW}</td>
<td>TRST Pulse Width(^2)</td>
<td>4 (\times) t\textsubscript{TCK}</td>
<td>ns</td>
</tr>
<tr>
<td><strong>Switching Characteristics</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t\textsubscript{DTDO}</td>
<td>TDO Delay from TCK Low</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t\textsubscript{SYS}</td>
<td>System Outputs Delay After TCK Low(^3)</td>
<td>0</td>
<td>12</td>
</tr>
</tbody>
</table>

\(^1\) System Inputs = DATA31–0, ARDY, PF47–0, PPI0CLK, PPI1CLK, RSLCLK0–1, RFS0–1, DR0PRI, DR0SEC, TSCLK0–1, TFS0–1, DR1PRI, DR1SEC, MOSI, MISO, SCK, RX, \texttt{RESET}, NM10, NM11, BMODE1–0, \texttt{BR}, and PPIxD7–0.

\(^2\) 50 MHz maximum

\(^3\) System Outputs = DATA31–0, ADDR25–2, AB0–3, AOE, AWE, AM03–0, SKAS, SCAS, SWE, SCKE, CLKOUT, SA10, SMS3–0, PF47–0, RSLCLK0–1, RFS0–1, TSCLK0–1, TFS0–1, DT0PRI, DT0SEC, DT1PRI, DT1SEC, MOSI, MISO, SCK, TX, \texttt{BG}, \texttt{BGH}, and PPIxD7–0.

Figure 29. JTAG Port Reset Timing

Figure 30. JTAG Port Timing
OUTPUT DRIVE CURRENTS

Figure 31 through Figure 38 show typical current voltage characteristics for the output drivers of the ADSP-BF561 processor. The curves represent the current drive capability of the output drivers as a function of output voltage. Refer to Table 8 to identify the driver type for a pin.

Figure 31. Drive Current A (Low \( V_{DDEXT} \))

Figure 32. Drive Current A (High \( V_{DDEXT} \))

Figure 33. Drive Current B (Low \( V_{DDEXT} \))

Figure 34. Drive Current B (High \( V_{DDEXT} \))

Figure 35. Drive Current C (Low \( V_{DDEXT} \))
POWER DISSIPATION

Many operating conditions can affect power dissipation. System designers should refer to Estimating Power for ADSP-BF561 Blackfin Processors (EE-293) on the Analog Devices website (www.analog.com)—use site search on “EE-293.” This document provides detailed information for optimizing your design for lowest power.

See the ADSP-BF561 Blackfin Processor Hardware Reference Manual for definitions of the various operating modes and for instructions on how to minimize system power.

TEST CONDITIONS

All timing parameters appearing in this data sheet were measured under the conditions described in this section. Figure 39 shows the measurement point for ac measurements (except output enable/disable). The measurement point $V_{\text{MEAS}}$ is 1.5 V for $V_{\text{DDEXT}}$ (nominal) = 2.5 V/3.3 V.

Output Enable Time Measurement

Output pins are considered to be enabled when they have made a transition from a high impedance state to the point when they start driving.

The output enable time $t_{\text{ENA}}$ is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving as shown on the right side of Figure 40.

The time $t_{\text{ENA,MEASURED}}$ is the interval, from when the reference signal switches, to when the output voltage reaches $V_{\text{TRIP(h)}}$ or $V_{\text{TRIP(l)}}$. $V_{\text{TRIP(h)}}$ is 2.0 V and $V_{\text{TRIP(l)}}$ is 1.0 V for $V_{\text{DDEXT}}$ (nominal) = 2.5 V/3.3 V. Time $t_{\text{TRIP}}$ is the interval from when the output starts driving to when the output reaches the $V_{\text{TRIP(h)}}$ or $V_{\text{TRIP(l)}}$ trip voltage.

Time $t_{\text{ENA}}$ is calculated as shown in the equation:

$$t_{\text{ENA}} = t_{\text{ENA,MEASURED}} - t_{\text{TRIP}}$$

If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Output Disable Time Measurement

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The output disable time $t_{\text{DIS}}$ is the difference between $t_{\text{DIS,MEASURED}}$ and $t_{\text{DECAY}}$ as shown on the left side of Figure 40.

$$t_{\text{DIS}} = t_{\text{DIS,MEASURED}} - t_{\text{DECAY}}$$
The time for the voltage on the bus to decay by $\Delta V$ is dependent on the capacitive load $C_l$ and the load current $I_l$. This decay time can be approximated by the equation:

$$t_{\text{DECAY}} = \frac{(C_l \Delta V)}{I_l}$$

The time $t_{\text{DECAY}}$ is calculated with test loads $C_l$ and $I_l$, and with $\Delta V$ equal to 0.5 V for $V_{\text{DDEXT (nominal)}} = 2.5\text{ V}/3.3\text{ V}$.

The time $t_{\text{DIS, MEASURED}}$ is the interval from when the reference signal switches, to when the output voltage decays $\Delta V$ from the measured output high or output low voltage.

**Example System Hold Time Calculation**

To determine the data output hold time in a particular system, first calculate $t_{\text{DECAY}}$ using the equation given above. Choose $\Delta V$ to be the difference between the ADSP-BF561 processor’s output voltage and the input threshold for the device requiring the hold time. $C_l$ is the total bus capacitance (per data line), and $I_l$ is the total leakage or three-state current (per data line). The hold time will be $t_{\text{DECAY}}$ plus the various output disable times as specified in the Timing Specifications (for example $t_{\text{DSDAT}}$ for an SDRAM write cycle as shown in SDRAM Interface Timing).

**Capacitive Loading**

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 41). $V_{\text{LOAD}}$ is 1.5 V for $V_{\text{DDEXT (nominal)}} = 2.5\text{ V}/3.3\text{ V}$. Figure 42 through Figure 49 show how output rise time varies with capacitance. The delay and hold specifications given should be derated by a factor derived from these figures. The graphs in these figures may not be linear outside the ranges shown.
ENVIRONMENTAL CONDITIONS

To determine the junction temperature on the application printed circuit board use:

\[ T_J = T_{CASE} + (\Psi_{JT} \times P_D) \]

where:
- \( T_J \) = junction temperature (°C).
- \( T_{CASE} \) = case temperature (°C) measured by customer at top center of package.
- \( \Psi_{JT} \) = from Table 32 through Table 34.
- \( P_D \) = power dissipation (see Power Dissipation for the method to calculate \( P_D \)).

Values of \( \theta_{JA} \) are provided for package comparison and printed circuit board design considerations. \( \theta_{JA} \) can be used for a first order approximation of \( T_J \) by the equation:

\[ T_J = T_A + (\theta_{JA} \times P_D) \]

where:
- \( T_A \) = ambient temperature (°C).
In Table 32 through Table 34, airflow measurements comply with JEDEC standards JESD51–2 and JESD51–6, and the junction-to-board measurement complies with JESD51–8. The junction-to-case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 2S2P JEDEC test board.

Thermal resistance $\theta_{JA}$ in Table 32 through Table 34 is the figure of merit relating to performance of the package and board in a convective environment. $\theta_{JMA}$ represents the thermal resistance under two conditions of airflow. $\theta_{JB}$ represents the heat extracted from the periphery of the board. $\Psi_{JT}$ represents the correlation between $T_J$ and $T_{CASE}$. Values of $\theta_{JB}$ are provided for package comparison and printed circuit board design considerations.

### Table 32. Thermal Characteristics for BC-256-4
(17 mm × 17 mm) Package

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Typical</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\theta_{JA}$</td>
<td>0 Linear m/s Airflow</td>
<td>18.1</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\theta_{JMA}$</td>
<td>1 Linear m/s Airflow</td>
<td>15.9</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\theta_{JMA}$</td>
<td>2 Linear m/s Airflow</td>
<td>15.1</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\theta_{Jc}$</td>
<td>Not Applicable</td>
<td>3.72</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\Psi_{JT}$</td>
<td>0 Linear m/s Airflow</td>
<td>0.11</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\Psi_{JT}$</td>
<td>1 Linear m/s Airflow</td>
<td>0.18</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\Psi_{JT}$</td>
<td>2 Linear m/s Airflow</td>
<td>0.18</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

### Table 33. Thermal Characteristics for BC-256-1
(12 mm × 12 mm) Package

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Typical</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\theta_{JA}$</td>
<td>0 Linear m/s Airflow</td>
<td>25.6</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\theta_{JMA}$</td>
<td>1 Linear m/s Airflow</td>
<td>22.4</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\theta_{JMA}$</td>
<td>2 Linear m/s Airflow</td>
<td>21.6</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\theta_{Jc}$</td>
<td>Not Applicable</td>
<td>18.9</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\theta_{Jc}$</td>
<td>Not Applicable</td>
<td>4.85</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\Psi_{JT}$</td>
<td>0 Linear m/s Airflow</td>
<td>0.15</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\Psi_{JT}$</td>
<td>1 Linear m/s Airflow</td>
<td>n/a</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\Psi_{JT}$</td>
<td>2 Linear m/s Airflow</td>
<td>n/a</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

### Table 34. Thermal Characteristics for B-297 Package

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Typical</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\theta_{JA}$</td>
<td>0 Linear m/s Airflow</td>
<td>20.6</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\theta_{JMA}$</td>
<td>1 Linear m/s Airflow</td>
<td>17.8</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\theta_{JMA}$</td>
<td>2 Linear m/s Airflow</td>
<td>17.4</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\theta_{Jc}$</td>
<td>Not Applicable</td>
<td>16.3</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\theta_{Jc}$</td>
<td>Not Applicable</td>
<td>7.15</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\Psi_{JT}$</td>
<td>0 Linear m/s Airflow</td>
<td>0.37</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\Psi_{JT}$</td>
<td>1 Linear m/s Airflow</td>
<td>n/a</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\Psi_{JT}$</td>
<td>2 Linear m/s Airflow</td>
<td>n/a</td>
<td>°C/W</td>
</tr>
</tbody>
</table>
# 256-BALL CSP_BGA (17 mm) BALL ASSIGNMENT

Table 35 lists the 256-Ball CSP_BGA (17 mm × 17 mm) ball assignment by ball number. Table 36 lists the ball assignment alphabetically by signal.

Table 35. 256-Ball CSP_BGA (17 mm × 17 mm) Ball Assignment (Numerically by Ball Number)

<table>
<thead>
<tr>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>VDDEXT</td>
<td>C9</td>
<td>SMS3</td>
<td>F1</td>
<td>CLkin</td>
<td>H9</td>
<td>GND</td>
</tr>
<tr>
<td>A2</td>
<td>ADDR22</td>
<td>C10</td>
<td>SWE</td>
<td>F2</td>
<td>PPI0D10</td>
<td>H10</td>
<td>GND</td>
</tr>
<tr>
<td>A3</td>
<td>ADDR18</td>
<td>C11</td>
<td>SA10</td>
<td>F3</td>
<td>RESET</td>
<td>H11</td>
<td>GND</td>
</tr>
<tr>
<td>A4</td>
<td>ADDR14</td>
<td>C12</td>
<td>ABE0</td>
<td>F4</td>
<td>BYPASS</td>
<td>H12</td>
<td>GND</td>
</tr>
<tr>
<td>A5</td>
<td>ADDR11</td>
<td>C13</td>
<td>ADDR07</td>
<td>F5</td>
<td>VDDEXT</td>
<td>H13</td>
<td>GND</td>
</tr>
<tr>
<td>A6</td>
<td>AMS3</td>
<td>C14</td>
<td>ADDR04</td>
<td>F6</td>
<td>VDDEXT</td>
<td>H14</td>
<td>DATA21</td>
</tr>
<tr>
<td>A7</td>
<td>AMS0</td>
<td>C15</td>
<td>DATA0</td>
<td>F7</td>
<td>VDDEXT</td>
<td>H15</td>
<td>DATA19</td>
</tr>
<tr>
<td>A8</td>
<td>ARDY</td>
<td>C16</td>
<td>DATA05</td>
<td>F8</td>
<td>GND</td>
<td>H16</td>
<td>DATA23</td>
</tr>
<tr>
<td>A9</td>
<td>SMS2</td>
<td>D1</td>
<td>PPI0D15</td>
<td>F9</td>
<td>GND</td>
<td>J1</td>
<td>VROUT1</td>
</tr>
<tr>
<td>A10</td>
<td>SCLK0</td>
<td>D2</td>
<td>PPI0SYNC3</td>
<td>F10</td>
<td>VDDEXT</td>
<td>J2</td>
<td>PPI0D8</td>
</tr>
<tr>
<td>A11</td>
<td>SCLK1</td>
<td>D3</td>
<td>PPI0SYNC2</td>
<td>F11</td>
<td>VDDEXT</td>
<td>J3</td>
<td>PPI0D7</td>
</tr>
<tr>
<td>A12</td>
<td>ABE2</td>
<td>D4</td>
<td>ADDR21</td>
<td>F12</td>
<td>VDDEXT</td>
<td>J4</td>
<td>PPI0D9</td>
</tr>
<tr>
<td>A13</td>
<td>ABE3</td>
<td>D5</td>
<td>ADDR15</td>
<td>F13</td>
<td>DATA11</td>
<td>J5</td>
<td>GND</td>
</tr>
<tr>
<td>A14</td>
<td>ADDR06</td>
<td>D6</td>
<td>ADDR09</td>
<td>F14</td>
<td>DATA08</td>
<td>J6</td>
<td>GND</td>
</tr>
<tr>
<td>A15</td>
<td>ADDR03</td>
<td>D7</td>
<td>AWE</td>
<td>F15</td>
<td>DATA10</td>
<td>J7</td>
<td>GND</td>
</tr>
<tr>
<td>A16</td>
<td>VDDEXT</td>
<td>D8</td>
<td>SMS0</td>
<td>F16</td>
<td>DATA16</td>
<td>J8</td>
<td>GND</td>
</tr>
<tr>
<td>B1</td>
<td>ADDR24</td>
<td>D9</td>
<td>SRAS</td>
<td>G1</td>
<td>XTAL</td>
<td>J9</td>
<td>GND</td>
</tr>
<tr>
<td>B2</td>
<td>ADDR23</td>
<td>D10</td>
<td>SCAS</td>
<td>G2</td>
<td>VDDEXT</td>
<td>J10</td>
<td>GND</td>
</tr>
<tr>
<td>B3</td>
<td>ADDR19</td>
<td>D11</td>
<td>BGH</td>
<td>G3</td>
<td>VDDEXT</td>
<td>J11</td>
<td>GND</td>
</tr>
<tr>
<td>B4</td>
<td>ADDR17</td>
<td>D12</td>
<td>ABE1</td>
<td>G4</td>
<td>GND</td>
<td>J12</td>
<td>VDDINT</td>
</tr>
<tr>
<td>B5</td>
<td>ADDR12</td>
<td>D13</td>
<td>DATA02</td>
<td>G5</td>
<td>GND</td>
<td>J13</td>
<td>VDDINT</td>
</tr>
<tr>
<td>B6</td>
<td>ADDR10</td>
<td>D14</td>
<td>DATA01</td>
<td>G6</td>
<td>VDDEXT</td>
<td>J14</td>
<td>DATA20</td>
</tr>
<tr>
<td>B7</td>
<td>AMS1</td>
<td>D15</td>
<td>DATA03</td>
<td>G7</td>
<td>GND</td>
<td>J15</td>
<td>DATA22</td>
</tr>
<tr>
<td>B8</td>
<td>AOE</td>
<td>D16</td>
<td>DATA07</td>
<td>G8</td>
<td>GND</td>
<td>J16</td>
<td>DATA24</td>
</tr>
<tr>
<td>B9</td>
<td>SMS1</td>
<td>E1</td>
<td>PPI0D11</td>
<td>G9</td>
<td>GND</td>
<td>K1</td>
<td>PPI0D6</td>
</tr>
<tr>
<td>B10</td>
<td>SCKE</td>
<td>E2</td>
<td>PPI0D13</td>
<td>G10</td>
<td>GND</td>
<td>K2</td>
<td>PPI0D5</td>
</tr>
<tr>
<td>B11</td>
<td>BR</td>
<td>E3</td>
<td>PPI0D12</td>
<td>G11</td>
<td>VDDEXT</td>
<td>K3</td>
<td>PPI0D4</td>
</tr>
<tr>
<td>B12</td>
<td>BG</td>
<td>E4</td>
<td>PPI0D14</td>
<td>G12</td>
<td>VDDEXT</td>
<td>K4</td>
<td>PPI0SYNC3</td>
</tr>
<tr>
<td>B13</td>
<td>ADDR08</td>
<td>E5</td>
<td>PPI1CLK</td>
<td>G13</td>
<td>DATA17</td>
<td>K5</td>
<td>VDDEXT</td>
</tr>
<tr>
<td>B14</td>
<td>ADDR05</td>
<td>E6</td>
<td>VDDINT</td>
<td>G14</td>
<td>DATA14</td>
<td>K6</td>
<td>VDDEXT</td>
</tr>
<tr>
<td>B15</td>
<td>ADDR02</td>
<td>E7</td>
<td>GND</td>
<td>G15</td>
<td>DATA15</td>
<td>K7</td>
<td>GND</td>
</tr>
<tr>
<td>B16</td>
<td>DATA04</td>
<td>E8</td>
<td>VDDINT</td>
<td>G16</td>
<td>DATA18</td>
<td>K8</td>
<td>GND</td>
</tr>
<tr>
<td>C1</td>
<td>PPI0SYNC1</td>
<td>E9</td>
<td>GND</td>
<td>H1</td>
<td>VROUT0</td>
<td>K9</td>
<td>GND</td>
</tr>
<tr>
<td>C2</td>
<td>ADDR25</td>
<td>E10</td>
<td>VDDINT</td>
<td>H2</td>
<td>GND</td>
<td>K10</td>
<td>GND</td>
</tr>
<tr>
<td>C3</td>
<td>PPI0CLK</td>
<td>E11</td>
<td>GND</td>
<td>H3</td>
<td>GND</td>
<td>K11</td>
<td>VDDEXT</td>
</tr>
<tr>
<td>C4</td>
<td>ADDR20</td>
<td>E12</td>
<td>VDDINT</td>
<td>H4</td>
<td>VDDINT</td>
<td>K12</td>
<td>GND</td>
</tr>
<tr>
<td>C5</td>
<td>ADDR16</td>
<td>E13</td>
<td>DATA06</td>
<td>H5</td>
<td>VDDINT</td>
<td>K13</td>
<td>GND</td>
</tr>
<tr>
<td>C6</td>
<td>ADDR13</td>
<td>E14</td>
<td>DATA13</td>
<td>H6</td>
<td>GND</td>
<td>K14</td>
<td>DATA26</td>
</tr>
<tr>
<td>C7</td>
<td>AMS2</td>
<td>E15</td>
<td>DATA09</td>
<td>H7</td>
<td>GND</td>
<td>K15</td>
<td>DATA25</td>
</tr>
<tr>
<td>C8</td>
<td>ARE</td>
<td>E16</td>
<td>DATA12</td>
<td>H8</td>
<td>GND</td>
<td>K16</td>
<td>DATA27</td>
</tr>
</tbody>
</table>
Table 35. 256-Ball CSP_BGA (17 mm × 17 mm) Ball Assignment (Numerically by Ball Number) (Continued)

<table>
<thead>
<tr>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>N9</td>
<td>GND</td>
<td>P5</td>
<td>PF01</td>
<td>R1</td>
<td>PPI1D12</td>
<td>R13</td>
<td>RSCLK1</td>
</tr>
<tr>
<td>N10</td>
<td>BMODE1</td>
<td>P6</td>
<td>PF06</td>
<td>R2</td>
<td>PPI1D11</td>
<td>R14</td>
<td>TSCLK1</td>
</tr>
<tr>
<td>N11</td>
<td>BMODE0</td>
<td>P7</td>
<td>PF08</td>
<td>R3</td>
<td>PPI1D4</td>
<td>R15</td>
<td>NC</td>
</tr>
<tr>
<td>N12</td>
<td>RX</td>
<td>P8</td>
<td>PF15</td>
<td>R4</td>
<td>PPI1D1</td>
<td>R16</td>
<td>TFS0</td>
</tr>
<tr>
<td>N13</td>
<td>DR1SEC</td>
<td>P9</td>
<td>NMI1</td>
<td>R5</td>
<td>PF02</td>
<td>T1</td>
<td>VDDEXT</td>
</tr>
<tr>
<td>N14</td>
<td>DT1SEC</td>
<td>P10</td>
<td>TMS</td>
<td>R6</td>
<td>PF07</td>
<td>T2</td>
<td>NC</td>
</tr>
<tr>
<td>N15</td>
<td>RFS0</td>
<td>P11</td>
<td>NMI0</td>
<td>R7</td>
<td>PF11</td>
<td>T3</td>
<td>PPI1D3</td>
</tr>
<tr>
<td>N16</td>
<td>DATA30</td>
<td>P12</td>
<td>SCK</td>
<td>R8</td>
<td>PF14</td>
<td>T4</td>
<td>PPI1D2</td>
</tr>
<tr>
<td>P1</td>
<td>PPI1D13</td>
<td>P13</td>
<td>RFS1</td>
<td>R9</td>
<td>TCK</td>
<td>T5</td>
<td>PF03</td>
</tr>
<tr>
<td>P2</td>
<td>PPI1D8</td>
<td>P14</td>
<td>TFS1</td>
<td>R10</td>
<td>TRST</td>
<td>T6</td>
<td>PF05</td>
</tr>
<tr>
<td>P3</td>
<td>PPI1D6</td>
<td>P15</td>
<td>DROSEC</td>
<td>R11</td>
<td>SLEEP</td>
<td>T7</td>
<td>PF10</td>
</tr>
<tr>
<td>P4</td>
<td>PPI1D0</td>
<td>P16</td>
<td>DTOSEC</td>
<td>R12</td>
<td>MOSI</td>
<td>T8</td>
<td>PF13</td>
</tr>
</tbody>
</table>
### Table 36. 256-Ball CSP_BGA (17 mm × 17 mm) Ball Assignment (Alphabetically by Signal)

<table>
<thead>
<tr>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>ABE0</td>
<td>C12</td>
<td>B</td>
<td>B11</td>
<td>DT0SEC</td>
<td>P16</td>
<td>GND</td>
<td>M9</td>
</tr>
<tr>
<td>ABE1</td>
<td>D12</td>
<td>4</td>
<td>F4</td>
<td>DT1PRI</td>
<td>T15</td>
<td>GND</td>
<td>M11</td>
</tr>
<tr>
<td>ABE2</td>
<td>A12</td>
<td>F</td>
<td>F1</td>
<td>DT1SEC</td>
<td>N14</td>
<td>GND</td>
<td>N9</td>
</tr>
<tr>
<td>ABE3</td>
<td>A13</td>
<td>C15</td>
<td>EMU</td>
<td>T11</td>
<td>MISO</td>
<td>T12</td>
<td>PP10SYNC1</td>
</tr>
<tr>
<td>ADDR02</td>
<td>B15</td>
<td>D14</td>
<td>GND</td>
<td>E7</td>
<td>MOSI</td>
<td>R12</td>
<td>PP10SYNC2</td>
</tr>
<tr>
<td>ADDR03</td>
<td>A15</td>
<td>D13</td>
<td>GND</td>
<td>E9</td>
<td>NC</td>
<td>L13</td>
<td>PP10SYNC3</td>
</tr>
<tr>
<td>ADDR04</td>
<td>C14</td>
<td>D15</td>
<td>GND</td>
<td>E11</td>
<td>NC</td>
<td>R15</td>
<td>PP11CLK</td>
</tr>
<tr>
<td>ADDR05</td>
<td>B14</td>
<td>B16</td>
<td>GND</td>
<td>F8</td>
<td>NC</td>
<td>T2</td>
<td>PP11D0</td>
</tr>
<tr>
<td>ADDR06</td>
<td>A14</td>
<td>C16</td>
<td>GND</td>
<td>F9</td>
<td>NM10</td>
<td>P11</td>
<td>PP11D1</td>
</tr>
<tr>
<td>ADDR07</td>
<td>C13</td>
<td>E13</td>
<td>GND</td>
<td>G4</td>
<td>NM1</td>
<td>P9</td>
<td>PP11D2</td>
</tr>
<tr>
<td>ADDR08</td>
<td>B13</td>
<td>D16</td>
<td>GND</td>
<td>G5</td>
<td>PF0</td>
<td>N5</td>
<td>PP11D3</td>
</tr>
<tr>
<td>ADDR09</td>
<td>D6</td>
<td>F14</td>
<td>GND</td>
<td>G7</td>
<td>PF01</td>
<td>P5</td>
<td>PP11D4</td>
</tr>
<tr>
<td>ADDR10</td>
<td>B6</td>
<td>E15</td>
<td>GND</td>
<td>G8</td>
<td>PF02</td>
<td>R5</td>
<td>PP11D5</td>
</tr>
<tr>
<td>ADDR11</td>
<td>A5</td>
<td>F15</td>
<td>GND</td>
<td>G9</td>
<td>PF03</td>
<td>T5</td>
<td>PP11D6</td>
</tr>
<tr>
<td>ADDR12</td>
<td>B5</td>
<td>F13</td>
<td>GND</td>
<td>G10</td>
<td>PF04</td>
<td>N6</td>
<td>PP11D7</td>
</tr>
<tr>
<td>ADDR13</td>
<td>C6</td>
<td>E16</td>
<td>GND</td>
<td>H2</td>
<td>PF05</td>
<td>T6</td>
<td>PP11D8</td>
</tr>
<tr>
<td>ADDR14</td>
<td>A4</td>
<td>E14</td>
<td>GND</td>
<td>H3</td>
<td>PF06</td>
<td>P6</td>
<td>PP11D9</td>
</tr>
<tr>
<td>ADDR15</td>
<td>D5</td>
<td>G14</td>
<td>GND</td>
<td>H6</td>
<td>PF07</td>
<td>R6</td>
<td>PP11D10</td>
</tr>
<tr>
<td>ADDR16</td>
<td>C5</td>
<td>G15</td>
<td>GND</td>
<td>H7</td>
<td>PF08</td>
<td>P7</td>
<td>PP11D11</td>
</tr>
<tr>
<td>ADDR17</td>
<td>B4</td>
<td>F16</td>
<td>GND</td>
<td>H8</td>
<td>PF09</td>
<td>N7</td>
<td>PP11D12</td>
</tr>
<tr>
<td>ADDR18</td>
<td>A3</td>
<td>G13</td>
<td>GND</td>
<td>H9</td>
<td>PF10</td>
<td>T7</td>
<td>PP11D13</td>
</tr>
<tr>
<td>ADDR19</td>
<td>B3</td>
<td>G16</td>
<td>GND</td>
<td>H10</td>
<td>PF11</td>
<td>R7</td>
<td>PP11D14</td>
</tr>
<tr>
<td>ADDR20</td>
<td>C4</td>
<td>H15</td>
<td>GND</td>
<td>H11</td>
<td>PF12</td>
<td>N8</td>
<td>PP11D15</td>
</tr>
<tr>
<td>ADDR21</td>
<td>D4</td>
<td>J14</td>
<td>GND</td>
<td>H12</td>
<td>PF13</td>
<td>T8</td>
<td>PP11SYNC1</td>
</tr>
<tr>
<td>ADDR22</td>
<td>A2</td>
<td>H14</td>
<td>GND</td>
<td>H13</td>
<td>PF14</td>
<td>R8</td>
<td>PP11SYNC2</td>
</tr>
<tr>
<td>ADDR23</td>
<td>B2</td>
<td>J15</td>
<td>GND</td>
<td>J5</td>
<td>PF15</td>
<td>P8</td>
<td>PP11SYNC3</td>
</tr>
<tr>
<td>ADDR24</td>
<td>B1</td>
<td>H16</td>
<td>GND</td>
<td>J6</td>
<td>PPIOCLK</td>
<td>C3</td>
<td>RESET</td>
</tr>
<tr>
<td>ADDR25</td>
<td>C2</td>
<td>J16</td>
<td>GND</td>
<td>J7</td>
<td>PPIO0</td>
<td>L4</td>
<td>RFS0</td>
</tr>
<tr>
<td>AMS0</td>
<td>A7</td>
<td>K15</td>
<td>GND</td>
<td>J8</td>
<td>PPIO1</td>
<td>L3</td>
<td>RFS1</td>
</tr>
<tr>
<td>AMS1</td>
<td>B7</td>
<td>K14</td>
<td>GND</td>
<td>J9</td>
<td>PPIO2</td>
<td>L2</td>
<td>RSCLK0</td>
</tr>
<tr>
<td>AMS2</td>
<td>C7</td>
<td>K16</td>
<td>GND</td>
<td>J10</td>
<td>PPIO3</td>
<td>L1</td>
<td>RSCLK1</td>
</tr>
<tr>
<td>AMS3</td>
<td>A6</td>
<td>L16</td>
<td>GND</td>
<td>J11</td>
<td>PPIO4</td>
<td>K3</td>
<td>RX</td>
</tr>
<tr>
<td>AOE</td>
<td>B8</td>
<td>M16</td>
<td>GND</td>
<td>K7</td>
<td>PPIO5</td>
<td>K2</td>
<td>SA10</td>
</tr>
<tr>
<td>ARDY</td>
<td>A8</td>
<td>N16</td>
<td>GND</td>
<td>K8</td>
<td>PPIO6</td>
<td>K1</td>
<td>SCAS</td>
</tr>
<tr>
<td>ARE</td>
<td>C8</td>
<td>L15</td>
<td>GND</td>
<td>K9</td>
<td>PPIO7</td>
<td>J3</td>
<td>SCK</td>
</tr>
<tr>
<td>AWE</td>
<td>D7</td>
<td>M14</td>
<td>GND</td>
<td>K10</td>
<td>PPIO8</td>
<td>J2</td>
<td>SCKE</td>
</tr>
<tr>
<td>BG</td>
<td>B12</td>
<td>P15</td>
<td>GND</td>
<td>K12</td>
<td>PPIO9</td>
<td>J4</td>
<td>SLCK0</td>
</tr>
<tr>
<td>BGH</td>
<td>D11</td>
<td>T14</td>
<td>GND</td>
<td>K13</td>
<td>PPIO10</td>
<td>F2</td>
<td>SLCK1</td>
</tr>
<tr>
<td>BMODE0</td>
<td>N11</td>
<td>N13</td>
<td>GND</td>
<td>L9</td>
<td>PPIO11</td>
<td>E1</td>
<td>SLEEP</td>
</tr>
<tr>
<td>BMODE1</td>
<td>N10</td>
<td>L14</td>
<td>GND</td>
<td>M7</td>
<td>PPIO12</td>
<td>E3</td>
<td>SMS0</td>
</tr>
<tr>
<td>--------</td>
<td>---------</td>
<td>--------</td>
<td>---------</td>
<td>--------</td>
<td>---------</td>
<td>--------</td>
<td>---------</td>
</tr>
<tr>
<td>SMS1</td>
<td>B9</td>
<td>TSCLK0</td>
<td>M15</td>
<td>VDDEXT</td>
<td>G3</td>
<td>VDDEXT</td>
<td>L11</td>
</tr>
<tr>
<td>SMS2</td>
<td>A9</td>
<td>TSCLK1</td>
<td>R14</td>
<td>VDDEXT</td>
<td>G6</td>
<td>VDDEXT</td>
<td>L12</td>
</tr>
<tr>
<td>SMS3</td>
<td>C9</td>
<td>TX</td>
<td>T13</td>
<td>VDDEXT</td>
<td>G11</td>
<td>VDDEXT</td>
<td>T1</td>
</tr>
<tr>
<td>SRA5</td>
<td>D9</td>
<td>VDDEXT</td>
<td>A1</td>
<td>VDDEXT</td>
<td>G12</td>
<td>VDDEXT</td>
<td>T16</td>
</tr>
<tr>
<td>SWE</td>
<td>C10</td>
<td>VDDEXT</td>
<td>A16</td>
<td>VDDEXT</td>
<td>K5</td>
<td>VDDINT</td>
<td>E6</td>
</tr>
<tr>
<td>TCK</td>
<td>R9</td>
<td>VDDEXT</td>
<td>F5</td>
<td>VDDEXT</td>
<td>K6</td>
<td>VDDINT</td>
<td>E8</td>
</tr>
<tr>
<td>TDI</td>
<td>T10</td>
<td>VDDEXT</td>
<td>F6</td>
<td>VDDEXT</td>
<td>K11</td>
<td>VDDINT</td>
<td>E10</td>
</tr>
<tr>
<td>TDO</td>
<td>T9</td>
<td>VDDEXT</td>
<td>F7</td>
<td>VDDEXT</td>
<td>L5</td>
<td>VDDINT</td>
<td>E12</td>
</tr>
<tr>
<td>TFS0</td>
<td>R16</td>
<td>VDDEXT</td>
<td>F10</td>
<td>VDDEXT</td>
<td>L6</td>
<td>VDDINT</td>
<td>H4</td>
</tr>
<tr>
<td>TFS1</td>
<td>P14</td>
<td>VDDEXT</td>
<td>F11</td>
<td>VDDEXT</td>
<td>L7</td>
<td>VDDINT</td>
<td>H5</td>
</tr>
<tr>
<td>TMS</td>
<td>P10</td>
<td>VDDEXT</td>
<td>F12</td>
<td>VDDEXT</td>
<td>L8</td>
<td>VDDINT</td>
<td>J12</td>
</tr>
<tr>
<td>TRST</td>
<td>R10</td>
<td>VDDEXT</td>
<td>G2</td>
<td>VDDEXT</td>
<td>L10</td>
<td>VDDINT</td>
<td>J13</td>
</tr>
</tbody>
</table>
Figure 50 lists the top view of the 256-Ball CSP_BGA (17 mm × 17 mm) ball configuration. Figure 51 lists the bottom view.

Figure 50. 256-Ball CSP_BGA Ball Configuration (Top View)

Figure 51. 256-Ball CSP_BGA Ball Configuration (Bottom View)
256-BALL CSP_BGA (12 mm) BALL ASSIGNMENT

Table 37 lists the 256-Ball CSP_BGA (12 mm × 12 mm) ball assignment by ball number. Table 38 lists the ball assignment alphabetically by signal.

Table 37. 256-Ball CSP_BGA (12 mm × 12 mm) Ball Assignment (Numerically by Ball Number)

<table>
<thead>
<tr>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>A01</td>
<td>VDDEXT</td>
<td>C09</td>
<td>SMS2</td>
<td>F01</td>
<td>CLKIN</td>
<td>H09</td>
<td>GND</td>
<td>L01</td>
<td>PPI0D0</td>
</tr>
<tr>
<td>A02</td>
<td>ADDR24</td>
<td>C10</td>
<td>A26</td>
<td>F02</td>
<td>VDDEXT</td>
<td>H10</td>
<td>GND</td>
<td>L02</td>
<td>PPI1SYNC2</td>
</tr>
<tr>
<td>A03</td>
<td>ADDR20</td>
<td>C11</td>
<td>GND</td>
<td>F03</td>
<td>RESET</td>
<td>H11</td>
<td>VDDINT</td>
<td>L03</td>
<td>GND</td>
</tr>
<tr>
<td>A04</td>
<td>VDDEXT</td>
<td>C12</td>
<td>BGH</td>
<td>F04</td>
<td>PPI0D10</td>
<td>H12</td>
<td>DATA16</td>
<td>L04</td>
<td>PPI1SYNC3</td>
</tr>
<tr>
<td>A05</td>
<td>ADDR14</td>
<td>C13</td>
<td>GND</td>
<td>F05</td>
<td>ADDR21</td>
<td>H13</td>
<td>DATA18</td>
<td>L05</td>
<td>VDDEXT</td>
</tr>
<tr>
<td>A06</td>
<td>ADDR10</td>
<td>C14</td>
<td>ADDR07</td>
<td>F06</td>
<td>ADDR17</td>
<td>H14</td>
<td>DATA20</td>
<td>L06</td>
<td>PPI1D11</td>
</tr>
<tr>
<td>A07</td>
<td>AMS3</td>
<td>C15</td>
<td>DATA1</td>
<td>F07</td>
<td>VDDINT</td>
<td>H15</td>
<td>DATA17</td>
<td>L07</td>
<td>GND</td>
</tr>
<tr>
<td>A08</td>
<td>AWE</td>
<td>C16</td>
<td>DATA3</td>
<td>F08</td>
<td>GND</td>
<td>H16</td>
<td>DATA19</td>
<td>L08</td>
<td>VDDINT</td>
</tr>
<tr>
<td>A09</td>
<td>VDDEXT</td>
<td>D01</td>
<td>PPI0D13</td>
<td>F09</td>
<td>VDDINT</td>
<td>H01</td>
<td>VROUT0</td>
<td>L09</td>
<td>GND</td>
</tr>
<tr>
<td>A10</td>
<td>AMS3</td>
<td>D02</td>
<td>PPI0D15</td>
<td>F10</td>
<td>GND</td>
<td>H02</td>
<td>VROUT1</td>
<td>L10</td>
<td>VDDEXT</td>
</tr>
<tr>
<td>A11</td>
<td>SCLK0</td>
<td>D03</td>
<td>PPI0SYNC3</td>
<td>F11</td>
<td>ADDR08</td>
<td>H03</td>
<td>PPI0D2</td>
<td>L11</td>
<td>GND</td>
</tr>
<tr>
<td>A12</td>
<td>SCLK1</td>
<td>D04</td>
<td>ADDR23</td>
<td>F12</td>
<td>DATA10</td>
<td>J01</td>
<td>PPI0D3</td>
<td>L12</td>
<td>DR0PRI</td>
</tr>
<tr>
<td>A13</td>
<td>BG</td>
<td>D05</td>
<td>GND</td>
<td>F13</td>
<td>DATA8</td>
<td>J05</td>
<td>PPI0D1</td>
<td>L13</td>
<td>TF50</td>
</tr>
<tr>
<td>A14</td>
<td>ABE2</td>
<td>D06</td>
<td>GND</td>
<td>F14</td>
<td>DATA12</td>
<td>J06</td>
<td>VDDEXT</td>
<td>L14</td>
<td>GND</td>
</tr>
<tr>
<td>A15</td>
<td>AMS3</td>
<td>D07</td>
<td>ADDR09</td>
<td>F15</td>
<td>DATA9</td>
<td>J07</td>
<td>GND</td>
<td>L15</td>
<td>DATA27</td>
</tr>
<tr>
<td>A16</td>
<td>VDDEXT</td>
<td>D08</td>
<td>GND</td>
<td>F16</td>
<td>DATA11</td>
<td>J08</td>
<td>VDDINT</td>
<td>L16</td>
<td>DATA29</td>
</tr>
<tr>
<td>B01</td>
<td>PPI1CLK</td>
<td>D09</td>
<td>ARDY</td>
<td>G01</td>
<td>XTAL</td>
<td>J09</td>
<td>VDDINT</td>
<td>M01</td>
<td>PPI1D15</td>
</tr>
<tr>
<td>B02</td>
<td>ADDR22</td>
<td>D10</td>
<td>SCAS</td>
<td>G02</td>
<td>GND</td>
<td>J10</td>
<td>VDDINT</td>
<td>M02</td>
<td>PPI1D13</td>
</tr>
<tr>
<td>B03</td>
<td>ADDR18</td>
<td>D11</td>
<td>SA10</td>
<td>G03</td>
<td>VDDEXT</td>
<td>J11</td>
<td>GND</td>
<td>M03</td>
<td>PPI1D9</td>
</tr>
<tr>
<td>B04</td>
<td>ADDR16</td>
<td>D12</td>
<td>VDDEXT</td>
<td>G04</td>
<td>BYPASS</td>
<td>J12</td>
<td>DATA30</td>
<td>M04</td>
<td>GND</td>
</tr>
<tr>
<td>B05</td>
<td>ADDR12</td>
<td>D13</td>
<td>ADDR02</td>
<td>G05</td>
<td>PPI0D14</td>
<td>J13</td>
<td>DATA22</td>
<td>M05</td>
<td>NC</td>
</tr>
<tr>
<td>B06</td>
<td>VDDEXT</td>
<td>D14</td>
<td>GND</td>
<td>G06</td>
<td>GND</td>
<td>J14</td>
<td>GND</td>
<td>M06</td>
<td>PF3</td>
</tr>
<tr>
<td>B07</td>
<td>AMS3</td>
<td>D15</td>
<td>DATA5</td>
<td>G07</td>
<td>GND</td>
<td>J15</td>
<td>DATA21</td>
<td>M07</td>
<td>PF7</td>
</tr>
<tr>
<td>B08</td>
<td>ARE</td>
<td>D16</td>
<td>DATA6</td>
<td>G08</td>
<td>GND</td>
<td>J16</td>
<td>DATA23</td>
<td>M08</td>
<td>VDDINT</td>
</tr>
<tr>
<td>B09</td>
<td>SMST</td>
<td>E01</td>
<td>GND</td>
<td>G09</td>
<td>VDDINT</td>
<td>K01</td>
<td>PPI0D6</td>
<td>M09</td>
<td>GND</td>
</tr>
<tr>
<td>B10</td>
<td>SCKE</td>
<td>E02</td>
<td>PPI0D11</td>
<td>G10</td>
<td>ADDR05</td>
<td>K02</td>
<td>PPI0D4</td>
<td>M10</td>
<td>BMODE0</td>
</tr>
<tr>
<td>B11</td>
<td>VDDEXT</td>
<td>E03</td>
<td>PPI0D12</td>
<td>G11</td>
<td>ADDR03</td>
<td>K03</td>
<td>PPI0D8</td>
<td>M11</td>
<td>SCK</td>
</tr>
<tr>
<td>B12</td>
<td>BR</td>
<td>E04</td>
<td>PPI0SYNC1</td>
<td>G12</td>
<td>DATA15</td>
<td>K04</td>
<td>PPI1SYNC1</td>
<td>M12</td>
<td>DR1PRI</td>
</tr>
<tr>
<td>B13</td>
<td>ABET</td>
<td>E05</td>
<td>ADDR15</td>
<td>G13</td>
<td>DATA14</td>
<td>K05</td>
<td>PPI1D14</td>
<td>M13</td>
<td>NC</td>
</tr>
<tr>
<td>B14</td>
<td>ADDR06</td>
<td>E06</td>
<td>ADDR13</td>
<td>G14</td>
<td>GND</td>
<td>K06</td>
<td>VDDEXT</td>
<td>M14</td>
<td>VDDEXT</td>
</tr>
<tr>
<td>B15</td>
<td>ADDR04</td>
<td>E07</td>
<td>AMS3</td>
<td>G15</td>
<td>DATA13</td>
<td>K07</td>
<td>GND</td>
<td>M15</td>
<td>DATA31</td>
</tr>
<tr>
<td>B16</td>
<td>DATA0</td>
<td>E08</td>
<td>VDDINT</td>
<td>G16</td>
<td>VDDEXT</td>
<td>K08</td>
<td>VDDINT</td>
<td>M16</td>
<td>DT0PRI</td>
</tr>
<tr>
<td>C01</td>
<td>PPI0SYNC2</td>
<td>E09</td>
<td>SMS2</td>
<td>H01</td>
<td>GND</td>
<td>K09</td>
<td>GND</td>
<td>N01</td>
<td>PPI1D12</td>
</tr>
<tr>
<td>C02</td>
<td>PPI0CLK</td>
<td>E10</td>
<td>AWE</td>
<td>H02</td>
<td>GND</td>
<td>K10</td>
<td>GND</td>
<td>N02</td>
<td>PPI1D10</td>
</tr>
<tr>
<td>C03</td>
<td>ADDR25</td>
<td>E11</td>
<td>ABE0</td>
<td>H03</td>
<td>PPI0D9</td>
<td>K11</td>
<td>VDDINT</td>
<td>N03</td>
<td>PPI1D3</td>
</tr>
<tr>
<td>C04</td>
<td>ADDR19</td>
<td>E12</td>
<td>DATA2</td>
<td>H04</td>
<td>PPI0D7</td>
<td>K12</td>
<td>DATA28</td>
<td>N04</td>
<td>PPI1D1</td>
</tr>
<tr>
<td>C05</td>
<td>GND</td>
<td>E13</td>
<td>GND</td>
<td>H05</td>
<td>PPI0D5</td>
<td>K13</td>
<td>DATA26</td>
<td>N05</td>
<td>PF1</td>
</tr>
<tr>
<td>C06</td>
<td>ADDR11</td>
<td>E14</td>
<td>DATA4</td>
<td>H06</td>
<td>VDDINT</td>
<td>K14</td>
<td>DATA24</td>
<td>N06</td>
<td>PF9</td>
</tr>
<tr>
<td>C07</td>
<td>AMS2</td>
<td>E15</td>
<td>DATA7</td>
<td>H07</td>
<td>VDDINT</td>
<td>K15</td>
<td>DATA25</td>
<td>N07</td>
<td>GND</td>
</tr>
<tr>
<td>C08</td>
<td>AMS0</td>
<td>E16</td>
<td>VDDEXT</td>
<td>H08</td>
<td>GND</td>
<td>K16</td>
<td>VDDEXT</td>
<td>N08</td>
<td>PF13</td>
</tr>
</tbody>
</table>

Rev. F | Page 51 of 63 | July 2023
Table 37. 256-Ball CSP_BGA (12 mm × 12 mm) Ball Assignment (Numerically by Ball Number) (Continued)

<table>
<thead>
<tr>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>N09</td>
<td>TDO</td>
<td>P05</td>
<td>GND</td>
<td>R01</td>
<td>PPI1D7</td>
<td>R13</td>
<td>TX/PF26</td>
<td>T09</td>
<td>TCK</td>
</tr>
<tr>
<td>N10</td>
<td>BMODE1</td>
<td>P06</td>
<td>PF5</td>
<td>R02</td>
<td>PPI1D6</td>
<td>R14</td>
<td>TSCLK1</td>
<td>T10</td>
<td>TMS</td>
</tr>
<tr>
<td>N11</td>
<td>MOSI</td>
<td>P07</td>
<td>PF11</td>
<td>R03</td>
<td>PPI1D2</td>
<td>R15</td>
<td>DT1PRI</td>
<td>T11</td>
<td>SLEEP</td>
</tr>
<tr>
<td>N12</td>
<td>GND</td>
<td>P08</td>
<td>PF15</td>
<td>R04</td>
<td>PPI1D0</td>
<td>R16</td>
<td>RFS0</td>
<td>T12</td>
<td>VDDEXT</td>
</tr>
<tr>
<td>N13</td>
<td>RFS1</td>
<td>P09</td>
<td>GND</td>
<td>R05</td>
<td>PF4</td>
<td>T01</td>
<td>VDDEXT</td>
<td>T13</td>
<td>RX/PF27</td>
</tr>
<tr>
<td>N14</td>
<td>GND</td>
<td>P10</td>
<td>TRST</td>
<td>R06</td>
<td>PF8</td>
<td>T02</td>
<td>PPI1D4</td>
<td>T14</td>
<td>DR1SEC</td>
</tr>
<tr>
<td>N15</td>
<td>DT0SEC</td>
<td>P11</td>
<td>NMI0</td>
<td>R07</td>
<td>PF10</td>
<td>T03</td>
<td>VDDEXT</td>
<td>T15</td>
<td>DT1SEC</td>
</tr>
<tr>
<td>N16</td>
<td>TSCLK0</td>
<td>P12</td>
<td>GND</td>
<td>R08</td>
<td>PF14</td>
<td>T04</td>
<td>PF2</td>
<td>T16</td>
<td>VDDEXT</td>
</tr>
<tr>
<td>P01</td>
<td>PPI1D8</td>
<td>P13</td>
<td>RSCLK1</td>
<td>R09</td>
<td>NMI1</td>
<td>T05</td>
<td>PF6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>P02</td>
<td>GND</td>
<td>P14</td>
<td>TFS1</td>
<td>R10</td>
<td>TDI</td>
<td>T06</td>
<td>VDDEXT</td>
<td></td>
<td></td>
</tr>
<tr>
<td>P03</td>
<td>PPI1D5</td>
<td>P15</td>
<td>RSCLK0</td>
<td>R11</td>
<td>EMU</td>
<td>T07</td>
<td>PF12</td>
<td></td>
<td></td>
</tr>
<tr>
<td>P04</td>
<td>PF0</td>
<td>P16</td>
<td>DR0SEC</td>
<td>R12</td>
<td>MISO</td>
<td>T08</td>
<td>VDDEXT</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## Table 38. 256-Ball CSP_BGA (12 mm × 12 mm) Ball Assignment (Alphabetically by Signal)

<table>
<thead>
<tr>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>ABE0</td>
<td>E11</td>
<td>BR</td>
<td>B12</td>
<td>DT0SEC</td>
<td>N15</td>
<td>GND</td>
<td>N14</td>
</tr>
<tr>
<td>ABE1</td>
<td>B13</td>
<td>BYPASS</td>
<td>G04</td>
<td>DT1PRI</td>
<td>R15</td>
<td>GND</td>
<td>P02</td>
</tr>
<tr>
<td>ABE2</td>
<td>A14</td>
<td>CLKIN</td>
<td>F01</td>
<td>DT1SEC</td>
<td>T15</td>
<td>GND</td>
<td>P05</td>
</tr>
<tr>
<td>ABE3</td>
<td>A15</td>
<td>DATA0</td>
<td>B16</td>
<td>EMU</td>
<td>R11</td>
<td>GND</td>
<td>P09</td>
</tr>
<tr>
<td>ADDR02</td>
<td>D13</td>
<td>DATA1</td>
<td>C15</td>
<td>GND</td>
<td>C05</td>
<td>GND</td>
<td>P12</td>
</tr>
<tr>
<td>ADDR03</td>
<td>G11</td>
<td>DATA2</td>
<td>E12</td>
<td>GND</td>
<td>C11</td>
<td>MI0</td>
<td>R12</td>
</tr>
<tr>
<td>ADDR04</td>
<td>B15</td>
<td>DATA3</td>
<td>C16</td>
<td>GND</td>
<td>C13</td>
<td>MOSI</td>
<td>N11</td>
</tr>
<tr>
<td>ADDR05</td>
<td>G10</td>
<td>DATA4</td>
<td>E14</td>
<td>GND</td>
<td>D05</td>
<td>NC</td>
<td>M05</td>
</tr>
<tr>
<td>ADDR06</td>
<td>B14</td>
<td>DATA5</td>
<td>D15</td>
<td>GND</td>
<td>D06</td>
<td>NC</td>
<td>M13</td>
</tr>
<tr>
<td>ADDR07</td>
<td>C14</td>
<td>DATA6</td>
<td>D16</td>
<td>GND</td>
<td>D08</td>
<td>NMI0</td>
<td>P11</td>
</tr>
<tr>
<td>ADDR08</td>
<td>F11</td>
<td>DATA7</td>
<td>E15</td>
<td>GND</td>
<td>D14</td>
<td>NMI1</td>
<td>R09</td>
</tr>
<tr>
<td>ADDR09</td>
<td>D07</td>
<td>DATA8</td>
<td>F13</td>
<td>GND</td>
<td>E01</td>
<td>PF0</td>
<td>P04</td>
</tr>
<tr>
<td>ADDR10</td>
<td>A06</td>
<td>DATA9</td>
<td>F15</td>
<td>GND</td>
<td>E13</td>
<td>PF1</td>
<td>N05</td>
</tr>
<tr>
<td>ADDR11</td>
<td>C06</td>
<td>DATA10</td>
<td>F12</td>
<td>GND</td>
<td>F08</td>
<td>PF2</td>
<td>T04</td>
</tr>
<tr>
<td>ADDR12</td>
<td>B05</td>
<td>DATA11</td>
<td>F16</td>
<td>GND</td>
<td>F10</td>
<td>PF3</td>
<td>M06</td>
</tr>
<tr>
<td>ADDR13</td>
<td>E06</td>
<td>DATA12</td>
<td>F14</td>
<td>GND</td>
<td>G02</td>
<td>PF4</td>
<td>R05</td>
</tr>
<tr>
<td>ADDR14</td>
<td>A05</td>
<td>DATA13</td>
<td>G15</td>
<td>GND</td>
<td>G06</td>
<td>PF5</td>
<td>P06</td>
</tr>
<tr>
<td>ADDR15</td>
<td>E05</td>
<td>DATA14</td>
<td>G13</td>
<td>GND</td>
<td>G07</td>
<td>PF6</td>
<td>T05</td>
</tr>
<tr>
<td>ADDR16</td>
<td>B04</td>
<td>DATA15</td>
<td>G12</td>
<td>GND</td>
<td>G08</td>
<td>PF7</td>
<td>M07</td>
</tr>
<tr>
<td>ADDR17</td>
<td>F06</td>
<td>DATA16</td>
<td>H12</td>
<td>GND</td>
<td>G14</td>
<td>PF8</td>
<td>R06</td>
</tr>
<tr>
<td>ADDR18</td>
<td>B03</td>
<td>DATA17</td>
<td>H15</td>
<td>GND</td>
<td>H01</td>
<td>PF9</td>
<td>N06</td>
</tr>
<tr>
<td>ADDR19</td>
<td>C04</td>
<td>DATA18</td>
<td>H13</td>
<td>GND</td>
<td>H02</td>
<td>PF10</td>
<td>R07</td>
</tr>
<tr>
<td>ADDR20</td>
<td>A03</td>
<td>DATA19</td>
<td>H16</td>
<td>GND</td>
<td>H08</td>
<td>PF11</td>
<td>P07</td>
</tr>
<tr>
<td>ADDR21</td>
<td>F05</td>
<td>DATA20</td>
<td>H14</td>
<td>GND</td>
<td>H09</td>
<td>PF12</td>
<td>T07</td>
</tr>
<tr>
<td>ADDR22</td>
<td>B02</td>
<td>DATA21</td>
<td>J15</td>
<td>GND</td>
<td>H10</td>
<td>PF13</td>
<td>N08</td>
</tr>
<tr>
<td>ADDR23</td>
<td>D04</td>
<td>DATA22</td>
<td>J13</td>
<td>GND</td>
<td>J07</td>
<td>PF14</td>
<td>R08</td>
</tr>
<tr>
<td>ADDR24</td>
<td>A02</td>
<td>DATA23</td>
<td>J16</td>
<td>GND</td>
<td>J11</td>
<td>PF15</td>
<td>P08</td>
</tr>
<tr>
<td>ADDR25</td>
<td>C03</td>
<td>DATA24</td>
<td>K14</td>
<td>GND</td>
<td>J14</td>
<td>PPI0CLK</td>
<td>C02</td>
</tr>
<tr>
<td>AMS0</td>
<td>C08</td>
<td>DATA25</td>
<td>K15</td>
<td>GND</td>
<td>K07</td>
<td>PPI0D0</td>
<td>L01</td>
</tr>
<tr>
<td>AMS1</td>
<td>B07</td>
<td>DATA26</td>
<td>K13</td>
<td>GND</td>
<td>K09</td>
<td>PPI0D1</td>
<td>J05</td>
</tr>
<tr>
<td>AMS2</td>
<td>E07</td>
<td>DATA27</td>
<td>L15</td>
<td>GND</td>
<td>K10</td>
<td>PPI0D2</td>
<td>J03</td>
</tr>
<tr>
<td>AMS3</td>
<td>A07</td>
<td>DATA28</td>
<td>K12</td>
<td>GND</td>
<td>L03</td>
<td>PPI0D3</td>
<td>J04</td>
</tr>
<tr>
<td>AOE</td>
<td>C07</td>
<td>DATA29</td>
<td>L16</td>
<td>GND</td>
<td>L07</td>
<td>PPI0D4</td>
<td>K02</td>
</tr>
<tr>
<td>ARDY</td>
<td>D09</td>
<td>DATA30</td>
<td>J12</td>
<td>GND</td>
<td>L09</td>
<td>PPI0D5</td>
<td>H05</td>
</tr>
<tr>
<td>ARE</td>
<td>B08</td>
<td>DATA31</td>
<td>M15</td>
<td>GND</td>
<td>L11</td>
<td>PPI0D6</td>
<td>K01</td>
</tr>
<tr>
<td>AWE</td>
<td>A08</td>
<td>DATA32</td>
<td>L12</td>
<td>GND</td>
<td>L14</td>
<td>PPI0D7</td>
<td>H04</td>
</tr>
<tr>
<td>BG</td>
<td>A13</td>
<td>DATA34</td>
<td>L16</td>
<td>GND</td>
<td>M04</td>
<td>PPI0D8</td>
<td>K03</td>
</tr>
<tr>
<td>BGH</td>
<td>C12</td>
<td>DR1PRI</td>
<td>M12</td>
<td>GND</td>
<td>M09</td>
<td>PPI0D9</td>
<td>H03</td>
</tr>
<tr>
<td>BMODE0</td>
<td>M10</td>
<td>DR1SEC</td>
<td>T14</td>
<td>GND</td>
<td>N07</td>
<td>PPI0D10</td>
<td>F04</td>
</tr>
<tr>
<td>BMODE1</td>
<td>N10</td>
<td>DT0PRI</td>
<td>M16</td>
<td>GND</td>
<td>N12</td>
<td>PPI0D11</td>
<td>E02</td>
</tr>
</tbody>
</table>
Table 38. 256-Ball CSP_BGA (12 mm × 12 mm) Ball Assignment (Alphabetically by Signal) (Continued)

<table>
<thead>
<tr>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>PPI0D12</td>
<td>E03</td>
<td>PPI1SYNC1</td>
<td>K04</td>
<td>TDO</td>
<td>N09</td>
<td>VDDEXT</td>
<td>M14</td>
</tr>
<tr>
<td>PPI0D13</td>
<td>D01</td>
<td>PPI1SYNC2</td>
<td>L02</td>
<td>TF50</td>
<td>L13</td>
<td>VDDEXT</td>
<td>T01</td>
</tr>
<tr>
<td>PPI0D14</td>
<td>G05</td>
<td>PPI1SYNC3</td>
<td>L04</td>
<td>TF51</td>
<td>P14</td>
<td>VDDEXT</td>
<td>T03</td>
</tr>
<tr>
<td>PPI0D15</td>
<td>D02</td>
<td>RESET</td>
<td>F03</td>
<td>TMS</td>
<td>T10</td>
<td>VDDEXT</td>
<td>T06</td>
</tr>
<tr>
<td>PPI0SYNC1</td>
<td>E04</td>
<td>RFS0</td>
<td>R16</td>
<td>TRST</td>
<td>P10</td>
<td>VDDEXT</td>
<td>T08</td>
</tr>
<tr>
<td>PPI0SYNC2</td>
<td>C01</td>
<td>RFS1</td>
<td>N13</td>
<td>TSCLK0</td>
<td>N16</td>
<td>VDDEXT</td>
<td>T12</td>
</tr>
<tr>
<td>PPI0SYNC3</td>
<td>D03</td>
<td>RSCLK0</td>
<td>P15</td>
<td>TSCLK1</td>
<td>R14</td>
<td>VDDEXT</td>
<td>T16</td>
</tr>
<tr>
<td>PPI1CLK</td>
<td>B01</td>
<td>RSCLK1</td>
<td>P13</td>
<td>TX/PF26</td>
<td>R13</td>
<td>VDDINT</td>
<td>E08</td>
</tr>
<tr>
<td>PPI1D0</td>
<td>R04</td>
<td>RX</td>
<td>T13</td>
<td>VDDEXT</td>
<td>A01</td>
<td>VDDINT</td>
<td>F07</td>
</tr>
<tr>
<td>PPI1D1</td>
<td>N04</td>
<td>SA10</td>
<td>D11</td>
<td>VDDEXT</td>
<td>A04</td>
<td>VDDINT</td>
<td>F09</td>
</tr>
<tr>
<td>PPI1D2</td>
<td>R03</td>
<td>SCAS</td>
<td>D10</td>
<td>VDDEXT</td>
<td>A09</td>
<td>VDDINT</td>
<td>G09</td>
</tr>
<tr>
<td>PPI1D3</td>
<td>N03</td>
<td>SCK</td>
<td>M11</td>
<td>VDDEXT</td>
<td>A16</td>
<td>VDDINT</td>
<td>H06</td>
</tr>
<tr>
<td>PPI1D4</td>
<td>T02</td>
<td>SCKE</td>
<td>B10</td>
<td>VDDEXT</td>
<td>B06</td>
<td>VDDINT</td>
<td>H07</td>
</tr>
<tr>
<td>PPI1D5</td>
<td>P03</td>
<td>SCLK0</td>
<td>A11</td>
<td>VDDEXT</td>
<td>B11</td>
<td>VDDINT</td>
<td>H11</td>
</tr>
<tr>
<td>PPI1D6</td>
<td>R02</td>
<td>SCLK1</td>
<td>A12</td>
<td>VDDEXT</td>
<td>D12</td>
<td>VDDINT</td>
<td>J08</td>
</tr>
<tr>
<td>PPI1D7</td>
<td>R01</td>
<td>SLEEP</td>
<td>T11</td>
<td>VDDEXT</td>
<td>E16</td>
<td>VDDINT</td>
<td>J09</td>
</tr>
<tr>
<td>PPI1D8</td>
<td>P01</td>
<td>SMS0</td>
<td>E09</td>
<td>VDDEXT</td>
<td>F02</td>
<td>VDDINT</td>
<td>J10</td>
</tr>
<tr>
<td>PPI1D9</td>
<td>M03</td>
<td>SMS1</td>
<td>B09</td>
<td>VDDEXT</td>
<td>G03</td>
<td>VDDINT</td>
<td>K08</td>
</tr>
<tr>
<td>PPI1D10</td>
<td>N02</td>
<td>SMS2</td>
<td>C09</td>
<td>VDDEXT</td>
<td>G16</td>
<td>VDDINT</td>
<td>K11</td>
</tr>
<tr>
<td>PPI1D11</td>
<td>L06</td>
<td>SMS3</td>
<td>A10</td>
<td>VDDEXT</td>
<td>J06</td>
<td>VDDINT</td>
<td>L08</td>
</tr>
<tr>
<td>PPI1D12</td>
<td>N01</td>
<td>SRAS</td>
<td>C10</td>
<td>VDDEXT</td>
<td>K06</td>
<td>VDDINT</td>
<td>M08</td>
</tr>
<tr>
<td>PPI1D13</td>
<td>M02</td>
<td>SWE</td>
<td>E10</td>
<td>VDDEXT</td>
<td>K16</td>
<td>VROUT0</td>
<td>J01</td>
</tr>
<tr>
<td>PPI1D14</td>
<td>K05</td>
<td>TCK</td>
<td>T09</td>
<td>VDDEXT</td>
<td>L05</td>
<td>VROUT1</td>
<td>J02</td>
</tr>
<tr>
<td>PPI1D15</td>
<td>M01</td>
<td>TDI</td>
<td>R10</td>
<td>VDDEXT</td>
<td>L10</td>
<td>XTAL</td>
<td>G01</td>
</tr>
</tbody>
</table>
Figure 52 lists the top view of the 256-Ball CSP_BGA (12 mm × 12 mm) ball configuration. Figure 53 lists the bottom view.

Figure 52. 256-Ball CSP_BGA Ball Configuration (Top View)

Figure 53. 256-Ball CSP_BGA Ball Configuration (Bottom View)
# 297-Ball PBGA Ball Assignment

Table 39 lists the 297-Ball PBGA ball assignment numerically by ball number. Table 40 lists the ball assignment alphabetically by signal.

## Table 39. 297-Ball PBGA Ball Assignment (Numerically by Ball Number)

<table>
<thead>
<tr>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>A01</td>
<td>GND</td>
<td>B15</td>
<td>SMST</td>
<td>G01</td>
<td>PPI0D11</td>
<td>L14</td>
<td>GND</td>
</tr>
<tr>
<td>A02</td>
<td>ADDR25</td>
<td>B16</td>
<td>SMST3</td>
<td>G02</td>
<td>PPI0D10</td>
<td>L15</td>
<td>GND</td>
</tr>
<tr>
<td>A03</td>
<td>ADDR23</td>
<td>B17</td>
<td>SCKE</td>
<td>G25</td>
<td>DATA4</td>
<td>L16</td>
<td>GND</td>
</tr>
<tr>
<td>A04</td>
<td>ADDR21</td>
<td>B18</td>
<td>SWE</td>
<td>G26</td>
<td>DATA7</td>
<td>L17</td>
<td>GND</td>
</tr>
<tr>
<td>A05</td>
<td>ADDR19</td>
<td>B19</td>
<td>SAI10</td>
<td>H01</td>
<td>BYPASS</td>
<td>L18</td>
<td>VDDINT</td>
</tr>
<tr>
<td>A06</td>
<td>ADDR17</td>
<td>B20</td>
<td>BCLK</td>
<td>H02</td>
<td>RESET</td>
<td>L25</td>
<td>DATA12</td>
</tr>
<tr>
<td>A07</td>
<td>ADDR15</td>
<td>B21</td>
<td>BG</td>
<td>H25</td>
<td>DATA6</td>
<td>L26</td>
<td>DATA15</td>
</tr>
<tr>
<td>A08</td>
<td>ADDR13</td>
<td>B22</td>
<td>ABE1</td>
<td>H26</td>
<td>DATA9</td>
<td>M01</td>
<td>VROUT0</td>
</tr>
<tr>
<td>A09</td>
<td>ADDR11</td>
<td>B23</td>
<td>ABE3</td>
<td>J01</td>
<td>CLKIN</td>
<td>M02</td>
<td>GND</td>
</tr>
<tr>
<td>A10</td>
<td>ADDR09</td>
<td>B24</td>
<td>ADDR07</td>
<td>J02</td>
<td>GND</td>
<td>M10</td>
<td>VDDINT</td>
</tr>
<tr>
<td>A11</td>
<td>AMS3</td>
<td>B25</td>
<td>GND</td>
<td>J10</td>
<td>VDDEXT</td>
<td>M11</td>
<td>GND</td>
</tr>
<tr>
<td>A12</td>
<td>AMS1</td>
<td>B26</td>
<td>ADDR05</td>
<td>J11</td>
<td>VDDEXT</td>
<td>M12</td>
<td>GND</td>
</tr>
<tr>
<td>A13</td>
<td>AWE</td>
<td>C01</td>
<td>PPI0SYNC3</td>
<td>J12</td>
<td>VDDEXT</td>
<td>M13</td>
<td>GND</td>
</tr>
<tr>
<td>A14</td>
<td>ARE</td>
<td>C02</td>
<td>PPI0CLK</td>
<td>J13</td>
<td>VDDEXT</td>
<td>M14</td>
<td>GND</td>
</tr>
<tr>
<td>A15</td>
<td>SMS0</td>
<td>C03</td>
<td>GND</td>
<td>J14</td>
<td>VDDEXT</td>
<td>M15</td>
<td>GND</td>
</tr>
<tr>
<td>A16</td>
<td>SMS2</td>
<td>C04</td>
<td>GND</td>
<td>J15</td>
<td>VDDEXT</td>
<td>M16</td>
<td>GND</td>
</tr>
<tr>
<td>A17</td>
<td>SRA5</td>
<td>C05</td>
<td>GND</td>
<td>J16</td>
<td>VDDINT</td>
<td>M17</td>
<td>GND</td>
</tr>
<tr>
<td>A18</td>
<td>SCAS</td>
<td>C22</td>
<td>GND</td>
<td>J17</td>
<td>VDDINT</td>
<td>M18</td>
<td>VDDINT</td>
</tr>
<tr>
<td>A19</td>
<td>SCLK0</td>
<td>C23</td>
<td>GND</td>
<td>J18</td>
<td>VDDINT</td>
<td>M25</td>
<td>DATA14</td>
</tr>
<tr>
<td>A20</td>
<td>SCLK1</td>
<td>C24</td>
<td>GND</td>
<td>J25</td>
<td>DATA8</td>
<td>M26</td>
<td>DATA17</td>
</tr>
<tr>
<td>A21</td>
<td>BGH</td>
<td>C25</td>
<td>ADDR04</td>
<td>J26</td>
<td>DATA11</td>
<td>N01</td>
<td>VROUT1</td>
</tr>
<tr>
<td>A22</td>
<td>ABE0</td>
<td>C26</td>
<td>ADDR03</td>
<td>K01</td>
<td>XTAL</td>
<td>N02</td>
<td>PPI0D9</td>
</tr>
<tr>
<td>A23</td>
<td>ABE2</td>
<td>D01</td>
<td>PPI0SYNC1</td>
<td>K02</td>
<td>NC</td>
<td>N10</td>
<td>VDDEXT</td>
</tr>
<tr>
<td>A24</td>
<td>ADDR08</td>
<td>D02</td>
<td>PPI0SYNC2</td>
<td>K10</td>
<td>VDDEXT</td>
<td>N11</td>
<td>GND</td>
</tr>
<tr>
<td>A25</td>
<td>ADDR06</td>
<td>D03</td>
<td>GND</td>
<td>K11</td>
<td>VDDEXT</td>
<td>N12</td>
<td>GND</td>
</tr>
<tr>
<td>A26</td>
<td>GND</td>
<td>D04</td>
<td>GND</td>
<td>K12</td>
<td>VDDEXT</td>
<td>N13</td>
<td>GND</td>
</tr>
<tr>
<td>B01</td>
<td>PPI1CLK</td>
<td>D23</td>
<td>GND</td>
<td>K13</td>
<td>VDDEXT</td>
<td>N14</td>
<td>GND</td>
</tr>
<tr>
<td>B02</td>
<td>GND</td>
<td>D24</td>
<td>GND</td>
<td>K14</td>
<td>VDDEXT</td>
<td>N15</td>
<td>GND</td>
</tr>
<tr>
<td>B03</td>
<td>ADDR24</td>
<td>D25</td>
<td>ADDR02</td>
<td>K15</td>
<td>VDDEXT</td>
<td>N16</td>
<td>GND</td>
</tr>
<tr>
<td>B04</td>
<td>ADDR22</td>
<td>D26</td>
<td>DATA1</td>
<td>K16</td>
<td>VDDINT</td>
<td>N17</td>
<td>GND</td>
</tr>
<tr>
<td>B05</td>
<td>ADDR20</td>
<td>E01</td>
<td>PPI0D15</td>
<td>K17</td>
<td>VDDINT</td>
<td>N18</td>
<td>VDDINT</td>
</tr>
<tr>
<td>B06</td>
<td>ADDR18</td>
<td>E02</td>
<td>PPI0D14</td>
<td>K18</td>
<td>VDDINT</td>
<td>N25</td>
<td>DATA16</td>
</tr>
<tr>
<td>B07</td>
<td>ADDR16</td>
<td>E03</td>
<td>GND</td>
<td>K25</td>
<td>DATA10</td>
<td>N26</td>
<td>DATA19</td>
</tr>
<tr>
<td>B08</td>
<td>ADDR14</td>
<td>E24</td>
<td>GND</td>
<td>K26</td>
<td>DATA13</td>
<td>P01</td>
<td>PPI0D7</td>
</tr>
<tr>
<td>B09</td>
<td>ADDR12</td>
<td>E25</td>
<td>DATA0</td>
<td>L01</td>
<td>NC</td>
<td>P02</td>
<td>PPI0D8</td>
</tr>
<tr>
<td>B10</td>
<td>ADDR10</td>
<td>E26</td>
<td>DATA3</td>
<td>L02</td>
<td>NC</td>
<td>P10</td>
<td>VDDEXT</td>
</tr>
<tr>
<td>B11</td>
<td>AMS2</td>
<td>F01</td>
<td>PPI0D13</td>
<td>L10</td>
<td>VDDEXT</td>
<td>P11</td>
<td>GND</td>
</tr>
<tr>
<td>B12</td>
<td>AMS0</td>
<td>F02</td>
<td>PPI0D12</td>
<td>L11</td>
<td>GND</td>
<td>P12</td>
<td>GND</td>
</tr>
<tr>
<td>B13</td>
<td>AOE</td>
<td>F25</td>
<td>DATA2</td>
<td>L12</td>
<td>GND</td>
<td>P13</td>
<td>GND</td>
</tr>
<tr>
<td>B14</td>
<td>ARDY</td>
<td>F26</td>
<td>DATA5</td>
<td>L13</td>
<td>GND</td>
<td>P14</td>
<td>GND</td>
</tr>
</tbody>
</table>
Table 39. 297-Ball PBGA Ball Assignment (Numerically by Ball Number) (Continued)

<table>
<thead>
<tr>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>P15</td>
<td>GND</td>
<td>U11</td>
<td>VDDEXT</td>
<td>AC04</td>
<td>GND</td>
<td>AE21</td>
<td>RX</td>
</tr>
<tr>
<td>P16</td>
<td>GND</td>
<td>U12</td>
<td>VDDEXT</td>
<td>AC23</td>
<td>GND</td>
<td>AE22</td>
<td>RFS1</td>
</tr>
<tr>
<td>P17</td>
<td>GND</td>
<td>U13</td>
<td>VDDEXT</td>
<td>AC24</td>
<td>GND</td>
<td>AE23</td>
<td>DR1SEC</td>
</tr>
<tr>
<td>P18</td>
<td>VDDEXT</td>
<td>U14</td>
<td>GND</td>
<td>AC25</td>
<td>DR0SEC</td>
<td>AE24</td>
<td>TFS1</td>
</tr>
<tr>
<td>P25</td>
<td>DATA18</td>
<td>U15</td>
<td>VDDEXT</td>
<td>AC26</td>
<td>RFS0</td>
<td>AE25</td>
<td>GND</td>
</tr>
<tr>
<td>P26</td>
<td>DATA21</td>
<td>U16</td>
<td>VDDEXT</td>
<td>AD01</td>
<td>PPI1D7</td>
<td>AE26</td>
<td>NC</td>
</tr>
<tr>
<td>R01</td>
<td>PPI0D5</td>
<td>U17</td>
<td>VDDEXT</td>
<td>AD02</td>
<td>PPI1D6</td>
<td>AF01</td>
<td>GND</td>
</tr>
<tr>
<td>R02</td>
<td>PPI0D6</td>
<td>U18</td>
<td>VDDEXT</td>
<td>AD03</td>
<td>GND</td>
<td>AF02</td>
<td>PPI1D4</td>
</tr>
<tr>
<td>R10</td>
<td>VDDEXT</td>
<td>U25</td>
<td>DATA24</td>
<td>AD04</td>
<td>GND</td>
<td>AF03</td>
<td>PPI1D2</td>
</tr>
<tr>
<td>R11</td>
<td>GND</td>
<td>U26</td>
<td>DATA27</td>
<td>AD05</td>
<td>GND</td>
<td>AF04</td>
<td>PPI1D0</td>
</tr>
<tr>
<td>R12</td>
<td>GND</td>
<td>V01</td>
<td>PPI1SYNC3</td>
<td>AD22</td>
<td>GND</td>
<td>AF05</td>
<td>PF1</td>
</tr>
<tr>
<td>R13</td>
<td>GND</td>
<td>V02</td>
<td>PPI0D0</td>
<td>AD23</td>
<td>GND</td>
<td>AF06</td>
<td>PF3</td>
</tr>
<tr>
<td>R14</td>
<td>GND</td>
<td>V25</td>
<td>DATA26</td>
<td>AD24</td>
<td>GND</td>
<td>AF07</td>
<td>PF5</td>
</tr>
<tr>
<td>R15</td>
<td>GND</td>
<td>V26</td>
<td>DATA29</td>
<td>AD25</td>
<td>NC</td>
<td>AF08</td>
<td>PF7</td>
</tr>
<tr>
<td>R16</td>
<td>GND</td>
<td>W01</td>
<td>PPI1SYNC1</td>
<td>AD26</td>
<td>R5CLK0</td>
<td>AF09</td>
<td>PF9</td>
</tr>
<tr>
<td>R17</td>
<td>GND</td>
<td>W02</td>
<td>PPI1SYNC2</td>
<td>AE01</td>
<td>PPI1D5</td>
<td>AF10</td>
<td>PF11</td>
</tr>
<tr>
<td>R18</td>
<td>VDDEXT</td>
<td>W25</td>
<td>DATA28</td>
<td>AE02</td>
<td>GND</td>
<td>AF11</td>
<td>PF13</td>
</tr>
<tr>
<td>R25</td>
<td>DATA20</td>
<td>W26</td>
<td>DATA31</td>
<td>AE03</td>
<td>PPI1D3</td>
<td>AF12</td>
<td>PF15</td>
</tr>
<tr>
<td>R26</td>
<td>DATA23</td>
<td>Y01</td>
<td>PPI1D15</td>
<td>AE04</td>
<td>PPI1D1</td>
<td>AF13</td>
<td>NMI1</td>
</tr>
<tr>
<td>T01</td>
<td>PPI0D3</td>
<td>Y02</td>
<td>PPI1D14</td>
<td>AE05</td>
<td>PF0</td>
<td>AF14</td>
<td>TCK</td>
</tr>
<tr>
<td>T02</td>
<td>PPI0D4</td>
<td>Y25</td>
<td>DATA30</td>
<td>AE06</td>
<td>PF2</td>
<td>AF15</td>
<td>TDI</td>
</tr>
<tr>
<td>T10</td>
<td>VDDEXT</td>
<td>Y26</td>
<td>DT0PRI</td>
<td>AE07</td>
<td>PF4</td>
<td>AF16</td>
<td>TMS</td>
</tr>
<tr>
<td>T11</td>
<td>GND</td>
<td>AA01</td>
<td>PPI1D13</td>
<td>AE08</td>
<td>PF6</td>
<td>AF17</td>
<td>SLEEP</td>
</tr>
<tr>
<td>T12</td>
<td>GND</td>
<td>AA02</td>
<td>PPI1D12</td>
<td>AE09</td>
<td>PF8</td>
<td>AF18</td>
<td>NMI0</td>
</tr>
<tr>
<td>T13</td>
<td>GND</td>
<td>AA25</td>
<td>DT0SEC</td>
<td>AE10</td>
<td>PF10</td>
<td>AF19</td>
<td>SCK</td>
</tr>
<tr>
<td>T14</td>
<td>GND</td>
<td>AA26</td>
<td>TSCLK0</td>
<td>AE11</td>
<td>PF12</td>
<td>AF20</td>
<td>TX</td>
</tr>
<tr>
<td>T15</td>
<td>GND</td>
<td>AB01</td>
<td>PPI1D11</td>
<td>AE12</td>
<td>PF14</td>
<td>AF21</td>
<td>R5CLK1</td>
</tr>
<tr>
<td>T16</td>
<td>GND</td>
<td>AB02</td>
<td>PPI1D10</td>
<td>AE13</td>
<td>NC</td>
<td>AF22</td>
<td>DR1PRI</td>
</tr>
<tr>
<td>T17</td>
<td>GND</td>
<td>AB03</td>
<td>GND</td>
<td>AE14</td>
<td>TDO</td>
<td>AF23</td>
<td>TSCLK1</td>
</tr>
<tr>
<td>T18</td>
<td>VDDEXT</td>
<td>AB24</td>
<td>GND</td>
<td>AE15</td>
<td>TRST</td>
<td>AF24</td>
<td>DT1SEC</td>
</tr>
<tr>
<td>T25</td>
<td>DATA22</td>
<td>AB25</td>
<td>TFS0</td>
<td>AE16</td>
<td>EMU</td>
<td>AF25</td>
<td>DT1PRI</td>
</tr>
<tr>
<td>T26</td>
<td>DATA25</td>
<td>AB26</td>
<td>DR0PRI</td>
<td>AE17</td>
<td>BMODE1</td>
<td>AF26</td>
<td>GND</td>
</tr>
<tr>
<td>U01</td>
<td>PPI0D1</td>
<td>AC01</td>
<td>PPI1D9</td>
<td>AE18</td>
<td>BMODE0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>U02</td>
<td>PPI0D2</td>
<td>AC02</td>
<td>PPI1D8</td>
<td>AE19</td>
<td>MIS0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>U10</td>
<td>VDDEXT</td>
<td>AC03</td>
<td>GND</td>
<td>AE20</td>
<td>MOSI</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## Table 40. 297-Ball PBGA Ball Assignment (Alphabetically by Signal)

<table>
<thead>
<tr>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>ABE0</td>
<td>A22</td>
<td>BM</td>
<td>B20</td>
<td>DT0SEC</td>
<td>AA25</td>
<td>GND</td>
<td>N15</td>
</tr>
<tr>
<td>ABE1</td>
<td>B22</td>
<td>BYPASS</td>
<td>H01</td>
<td>DT1PRI</td>
<td>AF25</td>
<td>GND</td>
<td>N16</td>
</tr>
<tr>
<td>ABE2</td>
<td>A23</td>
<td>CLKIN</td>
<td>J01</td>
<td>DT1SEC</td>
<td>AF24</td>
<td>GND</td>
<td>N17</td>
</tr>
<tr>
<td>ABE3</td>
<td>B23</td>
<td>DATA0</td>
<td>E25</td>
<td>EMU</td>
<td>AE16</td>
<td>GND</td>
<td>P11</td>
</tr>
<tr>
<td>ADDR02</td>
<td>D25</td>
<td>DATA1</td>
<td>D26</td>
<td>GND</td>
<td>A01</td>
<td>GND</td>
<td>P12</td>
</tr>
<tr>
<td>ADDR03</td>
<td>C26</td>
<td>DATA2</td>
<td>F25</td>
<td>GND</td>
<td>A26</td>
<td>GND</td>
<td>P13</td>
</tr>
<tr>
<td>ADDR04</td>
<td>C25</td>
<td>DATA3</td>
<td>E26</td>
<td>GND</td>
<td>B02</td>
<td>GND</td>
<td>P14</td>
</tr>
<tr>
<td>ADDR05</td>
<td>B26</td>
<td>DATA4</td>
<td>G25</td>
<td>GND</td>
<td>B25</td>
<td>GND</td>
<td>P15</td>
</tr>
<tr>
<td>ADDR06</td>
<td>A25</td>
<td>DATA5</td>
<td>F26</td>
<td>GND</td>
<td>C03</td>
<td>GND</td>
<td>P16</td>
</tr>
<tr>
<td>ADDR07</td>
<td>B24</td>
<td>DATA6</td>
<td>H25</td>
<td>GND</td>
<td>C04</td>
<td>GND</td>
<td>P17</td>
</tr>
<tr>
<td>ADDR08</td>
<td>A24</td>
<td>DATA7</td>
<td>G26</td>
<td>GND</td>
<td>C05</td>
<td>GND</td>
<td>R11</td>
</tr>
<tr>
<td>ADDR09</td>
<td>A10</td>
<td>DATA8</td>
<td>J25</td>
<td>GND</td>
<td>C22</td>
<td>GND</td>
<td>R12</td>
</tr>
<tr>
<td>ADDR10</td>
<td>B10</td>
<td>DATA9</td>
<td>H26</td>
<td>GND</td>
<td>C23</td>
<td>GND</td>
<td>R13</td>
</tr>
<tr>
<td>ADDR11</td>
<td>A09</td>
<td>DATA10</td>
<td>K25</td>
<td>GND</td>
<td>C24</td>
<td>GND</td>
<td>R14</td>
</tr>
<tr>
<td>ADDR12</td>
<td>B09</td>
<td>DATA11</td>
<td>J26</td>
<td>GND</td>
<td>D03</td>
<td>GND</td>
<td>R15</td>
</tr>
<tr>
<td>ADDR13</td>
<td>A08</td>
<td>DATA12</td>
<td>L25</td>
<td>GND</td>
<td>D04</td>
<td>GND</td>
<td>R16</td>
</tr>
<tr>
<td>ADDR14</td>
<td>B08</td>
<td>DATA13</td>
<td>K26</td>
<td>GND</td>
<td>D23</td>
<td>GND</td>
<td>R17</td>
</tr>
<tr>
<td>ADDR15</td>
<td>A07</td>
<td>DATA14</td>
<td>M25</td>
<td>GND</td>
<td>D24</td>
<td>GND</td>
<td>T11</td>
</tr>
<tr>
<td>ADDR16</td>
<td>B07</td>
<td>DATA15</td>
<td>L26</td>
<td>GND</td>
<td>E03</td>
<td>GND</td>
<td>T12</td>
</tr>
<tr>
<td>ADDR17</td>
<td>A06</td>
<td>DATA16</td>
<td>N25</td>
<td>GND</td>
<td>E24</td>
<td>GND</td>
<td>T13</td>
</tr>
<tr>
<td>ADDR18</td>
<td>B06</td>
<td>DATA17</td>
<td>M26</td>
<td>GND</td>
<td>J02</td>
<td>GND</td>
<td>T14</td>
</tr>
<tr>
<td>ADDR19</td>
<td>A05</td>
<td>DATA18</td>
<td>P25</td>
<td>GND</td>
<td>L11</td>
<td>GND</td>
<td>T15</td>
</tr>
<tr>
<td>ADDR20</td>
<td>B05</td>
<td>DATA19</td>
<td>N26</td>
<td>GND</td>
<td>L12</td>
<td>GND</td>
<td>T16</td>
</tr>
<tr>
<td>ADDR21</td>
<td>A04</td>
<td>DATA20</td>
<td>R25</td>
<td>GND</td>
<td>L13</td>
<td>GND</td>
<td>T17</td>
</tr>
<tr>
<td>ADDR22</td>
<td>B04</td>
<td>DATA21</td>
<td>P26</td>
<td>GND</td>
<td>L14</td>
<td>GND</td>
<td>U14</td>
</tr>
<tr>
<td>ADDR23</td>
<td>A03</td>
<td>DATA22</td>
<td>T25</td>
<td>GND</td>
<td>L15</td>
<td>GND</td>
<td>A03</td>
</tr>
<tr>
<td>ADDR24</td>
<td>B03</td>
<td>DATA23</td>
<td>R26</td>
<td>GND</td>
<td>L16</td>
<td>GND</td>
<td>A02</td>
</tr>
<tr>
<td>ADDR25</td>
<td>A02</td>
<td>DATA24</td>
<td>U25</td>
<td>GND</td>
<td>L17</td>
<td>GND</td>
<td>A03</td>
</tr>
<tr>
<td>AMS0</td>
<td>B12</td>
<td>DATA25</td>
<td>T26</td>
<td>GND</td>
<td>M02</td>
<td>GND</td>
<td>A04</td>
</tr>
<tr>
<td>AMS1</td>
<td>A12</td>
<td>DATA26</td>
<td>V25</td>
<td>GND</td>
<td>M11</td>
<td>GND</td>
<td>A23</td>
</tr>
<tr>
<td>AMS2</td>
<td>B11</td>
<td>DATA27</td>
<td>U26</td>
<td>GND</td>
<td>M12</td>
<td>GND</td>
<td>AC24</td>
</tr>
<tr>
<td>AMS3</td>
<td>A11</td>
<td>DATA28</td>
<td>W25</td>
<td>GND</td>
<td>M13</td>
<td>GND</td>
<td>AD03</td>
</tr>
<tr>
<td>AOE</td>
<td>B13</td>
<td>DATA29</td>
<td>V26</td>
<td>GND</td>
<td>M14</td>
<td>GND</td>
<td>AD04</td>
</tr>
<tr>
<td>ARDY</td>
<td>B14</td>
<td>DATA30</td>
<td>Y25</td>
<td>GND</td>
<td>M15</td>
<td>GND</td>
<td>AD05</td>
</tr>
<tr>
<td>ARE</td>
<td>A14</td>
<td>DATA31</td>
<td>W26</td>
<td>GND</td>
<td>M16</td>
<td>GND</td>
<td>AD22</td>
</tr>
<tr>
<td>AWE</td>
<td>A13</td>
<td>DR0PRI</td>
<td>AB26</td>
<td>GND</td>
<td>M17</td>
<td>GND</td>
<td>AD23</td>
</tr>
<tr>
<td>BG</td>
<td>B21</td>
<td>DR0SEC</td>
<td>AC25</td>
<td>GND</td>
<td>N11</td>
<td>GND</td>
<td>AD24</td>
</tr>
<tr>
<td>BGH</td>
<td>A21</td>
<td>DR1PRI</td>
<td>AF22</td>
<td>GND</td>
<td>N12</td>
<td>GND</td>
<td>AE02</td>
</tr>
<tr>
<td>BMODE0</td>
<td>AE18</td>
<td>DR1SEC</td>
<td>AE23</td>
<td>GND</td>
<td>N13</td>
<td>GND</td>
<td>AE25</td>
</tr>
<tr>
<td>BMODE1</td>
<td>AE17</td>
<td>DT0PRI</td>
<td>Y26</td>
<td>GND</td>
<td>N14</td>
<td>GND</td>
<td>AF01</td>
</tr>
</tbody>
</table>
Table 40. 297-Ball PBGA Ball Assignment (Alphabetically by Signal) (Continued)

<table>
<thead>
<tr>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
<th>Signal</th>
<th>Ball No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>AF26</td>
<td>PPI0D7</td>
<td>P01</td>
<td>RSLK0</td>
<td>AD26</td>
<td>VDDEXT</td>
<td>K13</td>
</tr>
<tr>
<td>MI0</td>
<td>AE19</td>
<td>PPI0D8</td>
<td>P02</td>
<td>RSLK1</td>
<td>AF21</td>
<td>VDDEXT</td>
<td>K14</td>
</tr>
<tr>
<td>MOSI</td>
<td>AE20</td>
<td>PPI0D9</td>
<td>N02</td>
<td>RX</td>
<td>AE21</td>
<td>VDDEXT</td>
<td>K15</td>
</tr>
<tr>
<td>NC</td>
<td>K02</td>
<td>PPI0D10</td>
<td>G02</td>
<td>SA10</td>
<td>B19</td>
<td>VDDEXT</td>
<td>L10</td>
</tr>
<tr>
<td>NC</td>
<td>L01</td>
<td>PPI0D11</td>
<td>G01</td>
<td>SCAS</td>
<td>A18</td>
<td>VDDEXT</td>
<td>M10</td>
</tr>
<tr>
<td>NC</td>
<td>L02</td>
<td>PPI0D12</td>
<td>F02</td>
<td>SCK</td>
<td>AF19</td>
<td>VDDEXT</td>
<td>N10</td>
</tr>
<tr>
<td>NC</td>
<td>AD25</td>
<td>PPI0D13</td>
<td>F01</td>
<td>SCKE</td>
<td>B17</td>
<td>VDDEXT</td>
<td>P10</td>
</tr>
<tr>
<td>NC</td>
<td>AE13</td>
<td>PPI0D14</td>
<td>E02</td>
<td>SCLK0</td>
<td>A19</td>
<td>VDDEXT</td>
<td>R10</td>
</tr>
<tr>
<td>NC</td>
<td>AE26</td>
<td>PPI0D15</td>
<td>E01</td>
<td>SCLK1</td>
<td>A20</td>
<td>VDDEXT</td>
<td>T10</td>
</tr>
<tr>
<td>NMI0</td>
<td>AF18</td>
<td>PPI0SYNC1</td>
<td>D01</td>
<td>SLEEP</td>
<td>AF17</td>
<td>VDDEXT</td>
<td>U10</td>
</tr>
<tr>
<td>NMI1</td>
<td>AF13</td>
<td>PPI0SYNC2</td>
<td>D02</td>
<td>SMS0</td>
<td>A15</td>
<td>VDDEXT</td>
<td>U11</td>
</tr>
<tr>
<td>PF0</td>
<td>AE05</td>
<td>PPI0SYNC3</td>
<td>C01</td>
<td>SMST</td>
<td>B15</td>
<td>VDDEXT</td>
<td>U12</td>
</tr>
<tr>
<td>PF1</td>
<td>AF05</td>
<td>PPI1CLK</td>
<td>B01</td>
<td>SMS2</td>
<td>A16</td>
<td>VDDEXT</td>
<td>U13</td>
</tr>
<tr>
<td>PF2</td>
<td>AE06</td>
<td>PPI1D0</td>
<td>AF04</td>
<td>SMS3</td>
<td>B16</td>
<td>VDDINT</td>
<td>J16</td>
</tr>
<tr>
<td>PF3</td>
<td>AF06</td>
<td>PPI1D1</td>
<td>AE04</td>
<td>SRAS</td>
<td>A17</td>
<td>VDDINT</td>
<td>J17</td>
</tr>
<tr>
<td>PF4</td>
<td>AE07</td>
<td>PPI1D2</td>
<td>AF03</td>
<td>SWE</td>
<td>B18</td>
<td>VDDINT</td>
<td>J18</td>
</tr>
<tr>
<td>PF5</td>
<td>AF07</td>
<td>PPI1D3</td>
<td>AE03</td>
<td>TCK</td>
<td>AF14</td>
<td>VDDINT</td>
<td>K16</td>
</tr>
<tr>
<td>PF6</td>
<td>AE08</td>
<td>PPI1D4</td>
<td>AF02</td>
<td>TDI</td>
<td>AF15</td>
<td>VDDINT</td>
<td>K17</td>
</tr>
<tr>
<td>PF7</td>
<td>AF08</td>
<td>PPI1D5</td>
<td>AE01</td>
<td>TDO</td>
<td>AE14</td>
<td>VDDINT</td>
<td>K18</td>
</tr>
<tr>
<td>PF8</td>
<td>AE09</td>
<td>PPI1D6</td>
<td>AD02</td>
<td>TFS0</td>
<td>AB25</td>
<td>VDDINT</td>
<td>L18</td>
</tr>
<tr>
<td>PF9</td>
<td>AF09</td>
<td>PPI1D7</td>
<td>AD01</td>
<td>TFS1</td>
<td>AE24</td>
<td>VDDINT</td>
<td>M18</td>
</tr>
<tr>
<td>PF10</td>
<td>AE10</td>
<td>PPI1D8</td>
<td>AC02</td>
<td>TMS</td>
<td>AF16</td>
<td>VDDINT</td>
<td>N18</td>
</tr>
<tr>
<td>PF11</td>
<td>AF10</td>
<td>PPI1D9</td>
<td>AC01</td>
<td>TRST</td>
<td>AE15</td>
<td>VDDINT</td>
<td>P18</td>
</tr>
<tr>
<td>PF12</td>
<td>AE11</td>
<td>PPI1D10</td>
<td>AB02</td>
<td>TSCLK0</td>
<td>AA26</td>
<td>VDDINT</td>
<td>R18</td>
</tr>
<tr>
<td>PF13</td>
<td>AF11</td>
<td>PPI1D11</td>
<td>AB01</td>
<td>TSCLK1</td>
<td>AF23</td>
<td>VDDINT</td>
<td>T18</td>
</tr>
<tr>
<td>PF14</td>
<td>AE12</td>
<td>PPI1D12</td>
<td>AA02</td>
<td>TX/PF26</td>
<td>AF20</td>
<td>VDDINT</td>
<td>U15</td>
</tr>
<tr>
<td>PF15</td>
<td>AF12</td>
<td>PPI1D13</td>
<td>AA01</td>
<td>VDDEXT</td>
<td>J10</td>
<td>VDDEXT</td>
<td>U16</td>
</tr>
<tr>
<td>PPI0CLK</td>
<td>C02</td>
<td>PPI1D14</td>
<td>Y02</td>
<td>VDDEXT</td>
<td>J11</td>
<td>VDDEXT</td>
<td>U17</td>
</tr>
<tr>
<td>PPI0D0</td>
<td>V02</td>
<td>PPI1D15</td>
<td>Y01</td>
<td>VDDEXT</td>
<td>J12</td>
<td>VDDEXT</td>
<td>U18</td>
</tr>
<tr>
<td>PPI0D1</td>
<td>U01</td>
<td>PPI1SYNC1</td>
<td>W01</td>
<td>VDDEXT</td>
<td>J13</td>
<td>VROUT0</td>
<td>M01</td>
</tr>
<tr>
<td>PPI0D2</td>
<td>U02</td>
<td>PPI1SYNC2</td>
<td>W02</td>
<td>VDDEXT</td>
<td>J14</td>
<td>VROUT1</td>
<td>N01</td>
</tr>
<tr>
<td>PPI0D3</td>
<td>T01</td>
<td>PPI1SYNC3</td>
<td>V01</td>
<td>VDDEXT</td>
<td>J15</td>
<td>XTAL</td>
<td>K01</td>
</tr>
<tr>
<td>PPI0D4</td>
<td>T02</td>
<td>RESET</td>
<td>H02</td>
<td>VDDEXT</td>
<td>K10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PPI0D5</td>
<td>R01</td>
<td>RF50</td>
<td>AC26</td>
<td>VDDEXT</td>
<td>K11</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PPI0D6</td>
<td>R02</td>
<td>RFS1</td>
<td>AE22</td>
<td>VDDEXT</td>
<td>K12</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Figure 54 lists the top view of the 297-Ball PBGA ball configuration. Figure 55 lists the bottom view.

**Figure 54. 297-Ball PBGA Ball Configuration (Top View)**

**Figure 55. 297-Ball PBGA Ball Configuration (Bottom View)**
OUTLINE DIMENSIONS

Dimensions in the outline dimension figures are shown in millimeters.

Figure 56. 256-Ball Chip Scale Package Ball Grid Array (CSP_BGA) (BC-256-4)
Figure 57. 256-Ball Chip Scale Package Ball Grid Array (CSP_BGA) (BC-256-1)

*COMPLIANT TO JEDEC STANDARDS MO-225 WITH EXCEPTION TO DIMENSIONS INDICATED BY AN ASTERISK.

Figure 58. 297-Ball Plastic Ball Grid Array (PBGA) (B-297)

COMPLIANT TO JEDEC STANDARDS MS-034-AAL-1
SURFACE-MOUNT DESIGN

Table 41 is provided as an aid to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface Mount Design and Land Pattern Standard.*

Table 41. BGA Data for Use with Surface-Mount Design

<table>
<thead>
<tr>
<th>Package</th>
<th>Ball Attach Type</th>
<th>Solder Mask Opening</th>
<th>Ball Pad Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>256-Ball CSP_BGA (BC-256-1)</td>
<td>Solder Mask Defined</td>
<td>0.30 mm diameter</td>
<td>0.43 mm diameter</td>
</tr>
<tr>
<td>256-Ball CSP_BGA (BC-256-4)</td>
<td>Solder Mask Defined</td>
<td>0.43 mm diameter</td>
<td>0.55 mm diameter</td>
</tr>
<tr>
<td>297-Ball PBGA (B-297)</td>
<td>Solder Mask Defined</td>
<td>0.43 mm diameter</td>
<td>0.58 mm diameter</td>
</tr>
</tbody>
</table>

ORDERING GUIDE

<table>
<thead>
<tr>
<th>Model</th>
<th>Temperature Range</th>
<th>Speed Grade (Max)</th>
<th>Package Description</th>
<th>Package Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADSP-BF561SKBCZ-6V</td>
<td>0°C to 70°C</td>
<td>600 MHz</td>
<td>256-Ball CSP_BGA</td>
<td>BC-256-1</td>
</tr>
<tr>
<td>ADSP-BF561SKBCZ-5V</td>
<td>0°C to 70°C</td>
<td>533 MHz</td>
<td>256-Ball CSP_BGA</td>
<td>BC-256-1</td>
</tr>
<tr>
<td>ADSP-BF561SKBCZ500</td>
<td>0°C to 70°C</td>
<td>500 MHz</td>
<td>256-Ball CSP_BGA</td>
<td>BC-256-1</td>
</tr>
<tr>
<td>ADSP-BF561SKBZ600</td>
<td>0°C to 70°C</td>
<td>600 MHz</td>
<td>297-Ball PBGA</td>
<td>B-297</td>
</tr>
<tr>
<td>ADSP-BF561SBZ500</td>
<td>–40°C to +85°C</td>
<td>500 MHz</td>
<td>297-Ball PBGA</td>
<td>B-297</td>
</tr>
<tr>
<td>ADSP-BF561SKBCZ-6A</td>
<td>0°C to 70°C</td>
<td>600 MHz</td>
<td>256-Ball CSP_BGA</td>
<td>BC-256-4</td>
</tr>
<tr>
<td>ADSP-BF561SKBCZ-5A</td>
<td>0°C to 70°C</td>
<td>500 MHz</td>
<td>256-Ball CSP_BGA</td>
<td>BC-256-4</td>
</tr>
<tr>
<td>ADSP-BF561SBBCZ-5A</td>
<td>–40°C to +85°C</td>
<td>500 MHz</td>
<td>256-Ball CSP_BGA</td>
<td>BC-256-4</td>
</tr>
</tbody>
</table>

1 Z = RoHS compliant part.

2 Referenced temperature is ambient temperature.