**ADSP-2185**

**FEATURES**

### PERFORMANCE
- 30 ns Instruction Cycle Time
- 33 MIPS Sustained Performance

### SINGLE-CYCLE INSTRUCTION EXECUTION
- Single-Cycle Context Switch
- 3-Bus Architecture Allows Dual Operand Fetches in Every Instruction Cycle

### MULTIFUNCTION INSTRUCTIONS
- Power-Down Mode Featuring Low CMOS Standby
- Power Dissipation with 100 Cycle Recovery from Power-Down Condition
- Low Power Dissipation in Idle Mode

### INTEGRATION
- ADSP-2100 Family Code Compatible, with Instruction Set Extensions
- 80K Bytes of On-Chip RAM, Configured as 16K Words On-Chip Program Memory RAM and 16K Words On-Chip Data Memory RAM
- Dual Purpose Program Memory for Both Instruction and Data Storage
- Independent ALU, Multiplier/Accumulator and Barrel Shifter Computational Units
- Two Independent Data Address Generators
- Powerful Program Sequencer Provides Zero Overhead Looping Conditional Instruction Execution
- Programmable 16-Bit Interval Timer with Prescaler
- 100-Lead TQFP

### SYSTEM INTERFACE
- 16-Bit Internal DMA Port for High Speed Access to On-Chip Memory (Mode Selectable)
- 4 MByte Byte Memory Interface for Storage of Data Tables & Program Overlays
- 8-Bit DMA to Byte Memory for Transparent Program and Data Memory Transfers (Mode Selectable)
- I/O Memory Interface with 2048 Locations Supports Parallel Peripherals (Mode Selectable)
- Programmable Memory Strobe & Separate I/O Memory Space Permits "Glueless" System Design (Mode Selectable)
- Programmable Wait State Generation
- Two Double-Buffered Serial Ports with Comping Hardware and Automatic Data Buffering
- Automatic Booting of On-Chip Program Memory from Byte-Wide External Memory, e.g., EPROM, or Through Internal DMA Port

### GENERAL NOTE

This data sheet represents production grade specifications for the ADSP-2185 (5 V).

### GENERAL DESCRIPTION

The ADSP-2185 is a single-chip microcomputer optimized for digital signal processing (DSP) and other high speed numeric processing applications.

The ADSP-2185 combines the ADSP-2100 family base architecture (three computational units, data address generators and a program sequencer) with two serial ports, a 16-bit internal DMA port, a byte DMA port, a programmable timer, flag I/O, extensive interrupt capabilities and on-chip program and data memory.

The ADSP-2185 integrates 80K bytes of on-chip memory configured as 16K words (24-bit) of program RAM and 16K words (16-bit) of data RAM. Power-down circuitry is also provided to meet the low power needs of battery operated portable equipment. The ADSP-2185 is available in 100-pin TQFP package.

In addition, the ADSP-2185 supports new instructions, which include bit manipulations—bit set, bit clear, bit toggle, bit test—new ALU constants, new multiplication instruction (x squared), biased rounding, result free ALU operations, I/O memory transfers and global interrupt masking, for increased flexibility.

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

• EZ-ICE® Serial Emulator for ADSP-218x Processor Family
• EZ-KIT Lite Evaluation Kit for ADSP-218x Processor

DOCUMENTATION

Application Notes

• AN-227: Digital Control System Design with the ADSP-2100 Family
• AN-227: Digital Control System Design with the ADSP-2100 Family
• AN-334: Digital Signal Processing Techniques
• AN-524: ADV601/ADV611 Bin Width Calculation in ADSP-21xx DSP
• EE-06: ADSP-21xx Serial Port Startup Issues
• EE-100: ADSP-218x External Overlay Memory
• EE-102: Mode D and ADSP-218x Pin Compatibility - the FAQs
• EE-103: Performing Level Conversion Between 5v and 3.3v IC’s
• EE-104: Setting Up Streams with the VisualDSP Debugger
• EE-11: ADSP-2181 Priority Chain & IDMA Holdoffs
• EE-110: A Quick Primer on ELF and DWARF File Formats
• EE-115: ADSP-2189 IDMA Interface to Motorola MC68300 Family of Microprocessors
• EE-12: Interrupts and Programmable Flags on the ADSP-2185/2186
• EE-121: Porting Code from ADSP-21xx to ADSP-219x
• EE-122: Coding for Performance on the ADSP-219x
• EE-123: An Overview of the ADSP-219x Pipeline
• EE-124: Booting up the ADSP-2192
• EE-125: ADSP-218x Embedded System Software Management and In-System-Programming (ISP)
• EE-128: DSP in C++: Calling Assembly Class Member Functions From C++
• EE-129: ADSP-2192 Interprocessor Communication
• EE-130: Making Fast Transition from ADSP-21xx to ADSP-219x
• EE-131: Booting the ADSP-2191/95/96 DSPs
• EE-133: Converting From Legacy Architecture Files To Linker Description Files for the ADSP-218x
• EE-139: Interfacing the ADSP-2191 to an AD7476 via the SPI Port
• EE-142: Autobuffering, C and FFTs on the ADSP-218x
• EE-144: Creating a Master-Slave SPI Interface Between Two ADSP-2191 DSPs
• EE-145: SPI Booting of the ADSP-2191 using the Atmel AD25020N on an EZ-KIT Lite Evaluation Board
• EE-146: Implementing a Boot Manager for ADSP-218x Family DSPs
• EE-152: Using Software Overlays with the ADSP-219x and VisualDSP 2.0+
• EE-153: ADSP-2191 Programmable PLL
• EE-154: ADSP-2191 Host Port Interface
• EE-156: Support for the H.100 protocol on the ADSP-2191
• EE-158: ADSP-2181 EZ-Kit Lite IDMA to PC Printer Port Interface
• EE-159: Initializing DSP System & Control Registers From C and C++
• EE-164: Advanced EPROM Boot and No-boot Scenarios with ADSP-219x DSPs
• EE-168: Using Third Overtone Crystals with the ADSP-218x DSP
• EE-17: ADSP-2187L Memory Organization
• EE-18: Choosing and Using FFTs for ADSP-21xx
• EE-188: Using C To Implement Interrupt-Driven Systems On ADSP-219x DSPs
• EE-2: Using ADSP-218x I/O Space
• EE-226: ADSP-2191 DSP Host Port Booting
• EE-227: CAN Configuration Procedure for ADSP-21992 DSPs
• EE-249: Implementing Software Overlays on ADSP-218x DSPs with VisualDSP++
• EE-32: Language Extensions: Memory Storage Types, ASM & Inline Constructs
• EE-33: Programming The ADSP-21xx Timer In C
• EE-35: Troubleshooting your ADSP-218x EZ-ICE
• EE-356: Emulator and Evaluation Hardware Troubleshooting Guide for CCES Users
• EE-36: ADSP-21xx Interface to the IOM-2 bus
• EE-38: ADSP-2181 IDMA Port - Cycle Steal Timing
• EE-39: Interfacing 5V Flash Memory to an ADSP-218x (Byte Programming Algorithm)
• EE-48: Converting Legacy 21xx Systems To A 218x System Design
• EE-5: ADSP-218x Full Memory Mode vs. Host Memory Mode
• EE-60: Simulating an RS-232 UART Using the Synchronous Serial Ports on the ADSP-21xx Family DSPs
• EE-64: Setting Mode Pins on Reset
• EE-68: Analog Devices JTAG Emulation Technical Reference
• EE-71: Minimum Rise Time Specs for Critical Interrupt and Clock Signals on the ADSP-21x1/21x5
• EE-74: Analog Devices Serial Port Development and Troubleshooting Guide
• EE-78: BDMA Usage on 100 pin ADSP-218x DSPs Configured for IDMA Use
• EE-79: EPROM Booting In Host Mode with 100 Pin 218x Processors
• EE-82: Using an ADSP-2181 DSP’s IO Space to IDMA Boot Another ADSP-2181
• EE-89: Implementing A Software UART on the ADSP-2181 EZ-Kit-Lite
• EE-90: Using the 21xx C-FFT Library
• EE-96: Interfacing Two AD73311 Codecs to the ADSP-218x

Data Sheet
• ADSP-2185: 16-bit, 33 MIPS, 5 v, 2 Serial Ports, Host Port, 80 KB RAM Data Sheet

Emulator Manuals
• ADSP-218X Family EZ-ICE Hardware Installation Guide

Integrated Circuit Anomalies
• ADSP-2185 Anomaly List for Revision 0.0

Processor Manuals
• ADSP 21xx Processors: Manuals
• ADSP-218x DSP Hardware Reference
• ADSP-218x DSP Instruction Set Reference
• Using the ADSP-2100 Family Volume 2

Software Manuals
• CrossCore Embedded Studio 2.5.0 C/C++ Library Manual for SHARC Processors
• VisualDSP++ 3.5 Assembler and Preprocessor Manual for ADSP-218x and ADSP-219x DSPs
• VisualDSP++ 3.5 C Compiler and Library Manual for ADSP-218x DSPs
• VisualDSP++ 3.5 C/C++ Compiler and Library Manual for ADSP-219x Processors
• VisualDSP++ 3.5 Linker and Utilities Manual for 16-Bit Processors
• VisualDSP++ 3.5 Loader Manual for 16-Bit Processors

SOFTWARE AND SYSTEMS REQUIREMENTS
• Software and Tools Anomalies Search

TOOLS AND SIMULATIONS
• ADSP-21xx Processors: Software and Tools
DESIGN RESOURCES

- ADSP-2185 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADSP-2185 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

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Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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ADSP-2185

Fabricated in a high speed, double metal, low power, 0.5 µm CMOS process, the ADSP-2185 operates with a 30 ns instruction cycle time. Every instruction can execute in a single processor cycle.

The ADSP-2185’s flexible architecture and comprehensive instruction set allow the processor to perform multiple operations in parallel. In one processor cycle the ADSP-2185 can:

- generate the next program address
- fetch the next instruction
- perform one or two data moves
- update one or two data address pointers
- perform a computational operation

This takes place while the processor continues to:

- receive and transmit data through the two serial ports
- receive and/or transmit data through the internal DMA port
- receive and/or transmit data through the byte DMA port
- decrement timer

Development System

The ADSP-2100 Family Development Software, a complete set of tools for software and hardware system development, supports the ADSP-2185. The System Builder provides a high level method for defining the architecture of systems under development. The Assembler has an algebraic syntax that is easy to program and debug. The Linker combines object files into an executable file. The Simulator provides an interactive instruction-level simulation with a reconfigurable user interface to display different portions of the hardware environment. A PROM Splitter generates PROM programmer compatible files. The C Compiler, based on the Free Software Foundation’s GNU C Compiler, generates ADSP-2185 assembly source code. The source code debugger allows programs to be corrected in the C environment. The Runtime Library includes over 100 ANSI-standard mathematical and DSP-specific functions.

The EZ-KIT Lite is a hardware/software kit offering a complete development environment for the entire ADSP-21xx family: an ADSP-218x based evaluation board with PC monitor software plus Assembler, Linker, Simulator and PROM Splitter software. The ADSP-21xx EZ-KIT Lite is a low cost, easy to use hardware platform on which you can quickly get started with your DSP software design. The EZ-KIT Lite includes the following features:

- 33 MHz ADSP-2181
- Full 16-bit Stereo Audio I/O with AD1847 SoundPort™ Codec
- RS-232 Interface to PC with Windows® 3.1 Control Software
- Stand-Alone Operation with Socketed EPROM
- EZ-ICE®™ Connector for Emulator Control
- DSP Demo Programs

The ADSP-218x EZ-ICE® Emulator aids in the hardware debugging of an ADSP-2185 system. The emulator consists of hardware, host computer resident software, and the target board connector. The ADSP-2185 integrates on-chip emulation support with a 14-pin ICE-PORT™ + interface. This interface provides a simpler target board connection that requires fewer mechanical clearance considerations than other ADSP-2100 Family EZ-ICE®™s. The ADSP-2185 device need not be removed from the target system when using the EZ-ICE®™, nor are any adapters needed. Due to the small footprint of the EZ-ICE®™ connector, emulation can be supported in final board designs.

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The EZ-ICE®™ performs a full range of functions, including:

- In-target operation
- Up to 20 breakpoints
- Single-step or full-speed operation
- Registers and memory values can be examined and altered
- PC upload and download functions
- Instruction-level emulation of program booting and execution
- Complete assembly and disassembly of instructions
- C source-level debugging

See Designing An EZ-ICE®™-Compatible Target System in the ADSP-2100 Family EZ-Tools Manual (ADSP-2181 sections) as well as the Target Board Connector for EZ-ICE®™ Probe section of this data sheet for the exact specifications of the EZ-ICE®™ target board connector.

Additional Information

This data sheet provides a general overview of ADSP-2185 functionality. For additional information on the architecture and instruction set of the processor, refer to the ADSP-2100 Family User’s Manual. For more information about the development tools, refer to the ADSP-2100 Family Development Tools Data Sheet.

ARCHITECTURE OVERVIEW

The ADSP-2185 instruction set provides flexible data moves and multifunction (one or two data moves with a computation) instructions. Every instruction can be executed in a single processor cycle. The ADSP-2185 assembly language uses an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development.

Figure 1. Block Diagram

Figure 1 is an overall block diagram of the ADSP-2185. The processor contains three independent computational units: the ALU, the multiplier/accumulator (MAC) and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add and multiply/subtract operations with 40 bits of accumulation. The shifter performs logical and arithmetic shifts, normalization, denormalization and derive exponent operations.

The shifter can be used to efficiently implement numeric format control including multiword and block floating-point representations.
The internal result (R) bus connects the computational units so the output of any unit may be the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient delivery of operands to these computational units. The sequencer supports conditional jumps, subroutine calls and returns in a single cycle. With internal loop counters and loop stacks, the ADSP-2185 executes looped code with zero overhead; no explicit jump instructions are required to maintain loops.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches from data memory and program memory. Each DAG maintains and updates four address pointers. Whenever the pointer is used to access data (indirect addressing), it is post-modified by the value of one of four possible modify registers. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers.

Efficient data transfer is achieved with the use of five internal buses:

- Program Memory Address (PMA) Bus
- Program Memory Data (PMD) Bus
- Data Memory Address (DMA) Bus
- Data Memory Data (DMD) Bus
- Result (R) Bus

The two address buses (PMA and DMA) share a single external address bus, allowing memory to be expanded off-chip, and the two data buses (PMD and DMD) share a single external data bus. Byte memory space and I/O memory space also share the external buses.

Program memory can store both instructions and data, permitting the ADSP-2185 to fetch two operands in a single cycle, one from program memory and one from data memory. The ADSP-2185 can fetch an operand from program memory and the next instruction in the same cycle.

When configured in host mode, the ADSP-2185 has a 16-bit Internal DMA port (IDMA port) for connection to external systems. The IDMA port is made up of 16 data/address pins and five control pins. The IDMA port provides transparent, direct access to the DSPs on-chip program and data RAM.

An interface to low cost byte-wide memory is provided by the Byte DMA port (BDMA port). The BDMA port is bidirectional and can directly address up to four megabytes of external RAM or ROM for off-chip storage of program overlays or data tables.

The byte memory and I/O memory space interface supports slow memories and I/O memory-mapped peripherals with programmable wait state generation. External devices can gain control of external buses with bus request/grant signals (BR, BGH and BG). One execution mode (GO Mode) allows the ADSP-2185 to continue running from on-chip memory. Normal execution mode requires the processor to halt while buses are granted.

The ADSP-2185 can respond to eleven interrupts. There can be up to six external interrupts (one edge-sensitive, two level-sensitive and three configurable) and seven internal interrupts generated by the timer, the serial ports (SPORTs), the Byte DMA port and the power-down circuitry. There is also a master RESET signal. The two serial ports provide a complete synchronous serial interface with optional companding in hardware and a

wide variety of framed or frameless data transmit and receive modes of operation.

Each port can generate an internal programmable serial clock or accept an external serial clock.

The ADSP-2185 provides up to 13 general-purpose flag pins. The data input and output pins on SPORT1 can be alternatively configured as an input flag and an output flag. In addition, eight flags are programmable as inputs or outputs, and three flags are always outputs.

A programmable interval timer generates periodic interrupts. A 16-bit count register (TCOUNT) decrements every n processor cycle, where n is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

**Serial Ports**

The ADSP-2185 incorporates two complete synchronous serial ports (SPORT0 and SPORT1) for serial communications and multiprocessor communication.

Here is a brief list of the capabilities of the ADSP-2185 SPORTs. For additional information on Serial Ports, refer to the ADSP-2100 Family User's Manual.

- SPORTs are bidirectional and have a separate, double-buffered transmit and receive section.
- SPORTs can use an external serial clock or generate their own serial clock internally.
- SPORTs have independent framing for the receive and transmit sections. Sections run in a frameless mode or with frame synchronization signals internally or externally generated. Frame sync signals are active high or inverted, with either of two pulse widths and timings.
- SPORTs support serial data word lengths from 3 to 16 bits and provide optional A-law and µ-law companding according to CCITT recommendation G.711.
- SPORT receive and transmit sections can generate unique interrupts on completing a data word transfer.
- SPORTs can receive and transmit an entire circular buffer of data with only one overhead cycle per data word. An interrupt is generated after a data buffer transfer.
- SPORT0 has a multichannel interface to selectively receive and transmit a 24 or 32 word, time-division multiplexed, serial bitstream.
- SPORT1 can be configured to have two external interrupts (IRQ0 and IRQ1) and the Flag In and Flag Out signals. The internally generated serial clock may still be used in this configuration.

**PIN DESCRIPTIONS**

The ADSP-2185 will be available in a 100-lead TQFP package. In order to maintain maximum functionality and reduce packaging size and pin count, some serial port, programmable flag, interrupt and external bus pins have dual, multiplexed functionality. The external bus pins are configured during RESET only, while serial port pins are software configurable during program execution. Flag and interrupt functionality is retained concurrently on multiplexed pins. In cases where pin functionality is reconfigurable, the default state is shown in plain text; alternate functionality is shown in italics.
### Common-Mode Pins

<table>
<thead>
<tr>
<th>Pin Name(s)</th>
<th># of Pins</th>
<th>Input/Output</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>RESET</td>
<td>1</td>
<td>I</td>
<td>Processor Reset Input</td>
</tr>
<tr>
<td>BR</td>
<td>1</td>
<td>I</td>
<td>Bus Request Input</td>
</tr>
<tr>
<td>BG</td>
<td>1</td>
<td>O</td>
<td>Bus Grant Output</td>
</tr>
<tr>
<td>BGD</td>
<td>1</td>
<td>O</td>
<td>Bus Grant Hung Output</td>
</tr>
<tr>
<td>DMS</td>
<td>1</td>
<td>O</td>
<td>Data Memory Select Output</td>
</tr>
<tr>
<td>PMS</td>
<td>1</td>
<td>O</td>
<td>Program Memory Select Output</td>
</tr>
<tr>
<td>IOMS</td>
<td>1</td>
<td>O</td>
<td>Memory Select Output</td>
</tr>
<tr>
<td>BMS</td>
<td>1</td>
<td>O</td>
<td>Byte Memory Select Output</td>
</tr>
<tr>
<td>CMS</td>
<td>1</td>
<td>O</td>
<td>Combined Memory Select Output</td>
</tr>
<tr>
<td>RD</td>
<td>1</td>
<td>O</td>
<td>Memory Read Enable Output</td>
</tr>
<tr>
<td>WR</td>
<td>1</td>
<td>O</td>
<td>Memory Write Enable Output</td>
</tr>
<tr>
<td>IRQ2/</td>
<td>1</td>
<td>I</td>
<td>Edge- or Level-Sensitive Interrupt Request¹</td>
</tr>
<tr>
<td>PF7</td>
<td></td>
<td>I/O</td>
<td>Programmable I/O Pin</td>
</tr>
<tr>
<td>IRQ0/</td>
<td>1</td>
<td>I</td>
<td>Level-Sensitive Interrupt Request¹</td>
</tr>
<tr>
<td>PF5</td>
<td></td>
<td>I/O</td>
<td>Programmable I/O Pin</td>
</tr>
<tr>
<td>IRQ1/</td>
<td>1</td>
<td>I</td>
<td>Level-Sensitive Interrupt Request¹</td>
</tr>
<tr>
<td>PF6</td>
<td></td>
<td>I/O</td>
<td>Programmable I/O Pin</td>
</tr>
<tr>
<td>IRQE/</td>
<td>1</td>
<td>I</td>
<td>Edge-Sensitive Interrupt Request¹</td>
</tr>
<tr>
<td>PF4</td>
<td></td>
<td>I/O</td>
<td>Programmable I/O Pin</td>
</tr>
<tr>
<td>Mode C/</td>
<td>1</td>
<td>I</td>
<td>Mode Select Input—Checked only During RESET</td>
</tr>
<tr>
<td>PF2</td>
<td></td>
<td>I/O</td>
<td>Programmable I/O Pin During Normal Operation</td>
</tr>
<tr>
<td>Mode B/</td>
<td>1</td>
<td>I</td>
<td>Mode Select Input—Checked only During RESET</td>
</tr>
<tr>
<td>PF1</td>
<td></td>
<td>I/O</td>
<td>Programmable I/O Pin During Normal Operation</td>
</tr>
<tr>
<td>Mode A/</td>
<td>1</td>
<td>I</td>
<td>Mode Select Input—Checked only During RESET</td>
</tr>
<tr>
<td>PF0</td>
<td></td>
<td>I/O</td>
<td>Programmable I/O Pin During Normal Operation</td>
</tr>
<tr>
<td>CLKIN, XTAL</td>
<td>2</td>
<td>I</td>
<td>Clock or Quartz Crystal Input</td>
</tr>
<tr>
<td>CLKOUT</td>
<td>1</td>
<td>O</td>
<td>Processor Clock Output</td>
</tr>
<tr>
<td>SPORT0</td>
<td>5</td>
<td>I/O</td>
<td>Serial Port I/O Pins</td>
</tr>
<tr>
<td>SPORT1/</td>
<td>5</td>
<td>I/O</td>
<td>Serial Port I/O Pins</td>
</tr>
<tr>
<td>IRQ0/</td>
<td></td>
<td></td>
<td>Edge- or Level-Sensitive Interrupts, Flag In, Flag Out²</td>
</tr>
<tr>
<td>F1, F0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PWD</td>
<td>1</td>
<td>I</td>
<td>Power-Down Control Input</td>
</tr>
<tr>
<td>PWDACK</td>
<td>1</td>
<td>O</td>
<td>Power-Down Control Output</td>
</tr>
<tr>
<td>FL0, FL1, FL2</td>
<td>3</td>
<td>O</td>
<td>Output Flags</td>
</tr>
<tr>
<td>VDD and GND</td>
<td>16</td>
<td>I</td>
<td>Power and Ground</td>
</tr>
<tr>
<td>EZ-Port</td>
<td>9</td>
<td>I/O</td>
<td>For Emulation Use</td>
</tr>
</tbody>
</table>

### Memory Interface Pins

The ADSP-2185 processor can be used in one of two modes, Full Memory Mode, which allows BDMA operation with full external overlay memory and I/O capability, or Host Mode, which allows IDMA operation with limited external addressing capabilities. The operating mode is determined by the state of the Mode C pin during RESET and cannot be changed while the processor is running.

### Full Memory Mode Pins (Mode C = 0)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th># of Pins</th>
<th>Input/Output</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>A13:0</td>
<td>14</td>
<td>O</td>
<td>Address Output Pins for Program, Data, and I/O Spaces</td>
</tr>
<tr>
<td>D23:0</td>
<td>24</td>
<td>I/O</td>
<td>Data I/O Pins for Program, Data, Byte and I/O Spaces (8 MB Are Also Used as Byte Memory Addresses)</td>
</tr>
</tbody>
</table>

### Host Mode Pins (Mode C = 1)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th># of Pins</th>
<th>Input/Output</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>IAD 15:0</td>
<td>16</td>
<td>I/O</td>
<td>IDMA Port Address/Data Bus</td>
</tr>
<tr>
<td>A0</td>
<td>1</td>
<td>O</td>
<td>Address Pin for External I/O, Program, Data, or Byte Access</td>
</tr>
<tr>
<td>D23:8</td>
<td>16</td>
<td>I/O</td>
<td>Data I/O Pins for Program, Data Byte and I/O Spaces</td>
</tr>
<tr>
<td>IWR</td>
<td>1</td>
<td>I</td>
<td>IDMA Write Enable</td>
</tr>
<tr>
<td>IRD</td>
<td>1</td>
<td>I</td>
<td>IDMA Read Enable</td>
</tr>
<tr>
<td>IAL</td>
<td>1</td>
<td>I</td>
<td>IDMA Address Latch Pin</td>
</tr>
<tr>
<td>IS</td>
<td>1</td>
<td>I</td>
<td>IDMA Select</td>
</tr>
<tr>
<td>IACK</td>
<td>1</td>
<td>O</td>
<td>IDMA Port Acknowledge</td>
</tr>
</tbody>
</table>

### Setting Memory Mode

Memory Mode selection for the ADSP-2185 is made during chip reset through the use of the Mode C pin. This pin is multiplexed with the DSP’s PF2 pin, so care must be taken in how the mode selection is made. The two methods for selecting the value of Mode C are active and passive.

Passive configuration involves the use of a pull-up or pull-down resistor connected to the Mode C pin. To minimize power consumption, or if the PF2 pin is to be used as an output in the DSP application, a weak pull-up or pull-down, on the order of 100 kΩ, can be used. This value should be sufficient to pull the pin to the desired level and still allow the pin to operate as a programmable flag output without undue strain on the processor’s output driver. For minimum power consumption during power-down, reconfigure PF2 to be an input as the pull-up or pull-down will hold the pin in a known state and will not switch.

Active configuration involves the use of a three-stateable external driver connected to the Mode C pin. A driver’s output enable should be connected to the DSP’s RESET signal such that it only drives the PF2 pin when RESET is active (low). After...
RESET is deasserted, the driver should three-state, thus allowing full use of the PF 2 pin as either an input or output.

To minimize power consumption during power-down, configure the programmable flag as an output when connected to a three-stated buffer. This ensures that the pin will be held at a constant level and not oscillate should the three-state driver's level hover around the logic switching point.

Interrupts

The interrupt controller allows the processor to respond to the eleven possible interrupts and reset with minimum overhead. The ADSP-2185 provides four dedicated external interrupt input pins, IRQ2, IRQL0, IRQL1, and IRQE (shared with the PF 7:4 pins). In addition, SPORT 1 may be reconfigured for IRQ0, IRQ1, FLAG_IN, and FLAG_OUT, for a total of six external interrupts. The ADSP-2185 also supports internal interrupts from the timer, the byte DMA port, the two serial ports, software and the power-down control circuit. The interrupt levels are internally prioritized and individually maskable (except power-down and reset). The IRQ2, IRQ0, and IRQ1 input pins can be programmed to be either level- or edge-sensitive. IRQL0 and IRQL1 are level-sensitive and IRQE is edge-sensitive. The priorities and vector addresses of all interrupts are shown in Table I.

Table I. Interrupt Priority & Interrupt Vector Addresses

<table>
<thead>
<tr>
<th>Source Of Interrupt</th>
<th>Interrupt Vector Address (Hex)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reset (or Power-Up with</td>
<td>0000 (Highest Priority)</td>
</tr>
<tr>
<td>PUCR = 1)</td>
<td></td>
</tr>
<tr>
<td>Power-down (Nonmaskable)</td>
<td>002C</td>
</tr>
<tr>
<td>IRQ2</td>
<td>0004</td>
</tr>
<tr>
<td>IRQL1</td>
<td>0008</td>
</tr>
<tr>
<td>IRQL0</td>
<td>000C</td>
</tr>
<tr>
<td>SPORT 0 Transmit</td>
<td>0010</td>
</tr>
<tr>
<td>SPORT 0 Receive</td>
<td>0014</td>
</tr>
<tr>
<td>IRQE</td>
<td>0018</td>
</tr>
<tr>
<td>BDMA Interrupt</td>
<td>001C</td>
</tr>
<tr>
<td>SPORT 1 Transmit or IRQ1</td>
<td>0020</td>
</tr>
<tr>
<td>SPORT 1 Receive or IRQ0</td>
<td>0024</td>
</tr>
<tr>
<td>Timer</td>
<td>0028 (Lowest Priority)</td>
</tr>
</tbody>
</table>

Interrupt routines can either be nested, with higher priority interrupts taking precedence, or processed sequentially. Interrupts can be masked or unmasked with the IMASK register. Individual interrupt requests are logically ANDed with the bits in IMASK; the highest priority unmasked interrupt is then selected. The power-down interrupt is nonmaskable.

The ADSP-2185 masks all interrupts for one instruction cycle following the execution of an instruction that modifies the IMASK register. This does not affect serial port autobuffering or DMA transfers.

The interrupt control register, ICNTL, controls interrupt nesting and defines the IRQ0, IRQ1, and IRQ2 external interrupts to be either edge- or level-sensitive. The IRQE pin is an external edge-sensitive interrupt and can be forced and cleared. The IRQL0 and IRQL1 pins are external level-sensitive interrupts.

The IFC register is a write-only register used to force and clear interrupts. On-chip stacks preserve the processor status and are automatically maintained during interrupt handling. The stacks are twelve levels deep to allow interrupt, loop and subroutine nesting.

The following instructions allow global enable or disable servicing of the interrupts (including power-down), regardless of the state of IMASK. Disabling the interrupts does not affect serial port autobuffering or DMA.

ENA INTS;
DIS INTS;

When the processor is reset, interrupt servicing is enabled.

LOW POWER OPERATION

The ADSP-2185 has three low power modes that significantly reduce the power dissipation when the device operates under standby conditions. These modes are:

- Power-Down
- Idle
- Slow Idle

The CLKOUT pin may also be disabled to reduce external power dissipation.

Power-Down

The ADSP-2185 processor has a low power feature that lets the processor enter a very low power dormant state through hardware or software control. Here is a brief list of power-down features. Refer to the ADSP-2100 Family User’s Manual, “System Interface” chapter, for detailed information about the power-down feature.

- Quick recovery from power-down. The processor begins executing instructions in as few as 100 CLKIN cycles.
- Support for an externally generated TTL or CMOS processor clock. The external clock can continue running during power-down without affecting the lowest power rating and 100 CLKIN cycle recovery.
- Support for crystal operation includes disabling the oscillator to save power (the processor automatically waits approximately 4096 CLKIN cycles for the crystal oscillator to start or stabilize), and letting the oscillator run to allow 100 CLKIN cycle start-up.
- Power-down is initiated by either the power-down pin (PWD) or the software power-down force bit.
- Interrupt support allows an unlimited number of instructions to be executed before optionally powering down. The power-down interrupt also can be used as a nonmaskable, edge-sensitive interrupt.
- Context clear/save control allows the processor to continue where it left off or start with a clean context when leaving the power-down state.
- The RESET pin also can be used to terminate power-down.
- Power-down acknowledge pin indicates when the processor has entered power-down.
ADSP-2185

Idle
When the ADSP-2185 is in the Idle Mode, the processor waits indefinitely in a low power state until an interrupt occurs. When an unmasked interrupt occurs, it is serviced; execution then continues with the instruction following the IDLE instruction. In Idle mode IDM A, BD M A and autobuffer cycle steals still occur.

Slow Idle
The IDLE instruction is enhanced on the ADSP-2185 to let the processor’s internal clock signal be slowed, further reducing power consumption. The reduced clock frequency, a programmable fraction of the normal clock rate, is specified by a selectable divisor given in the IDLE instruction. The format of the instruction is

\[ \text{IDLE}(n) \]

where \( n = 16, 32, 64 \) or 128. This instruction keeps the processor fully functional, but operating at the slower clock rate. While it is in this state, the processor’s other internal clock signals, such as SCLK, CLKOUT and timer clock, are reduced by the same ratio. The default form of the instruction, when no clock divisor is given, is the standard IDLE instruction.

When the IDLE \((n)\) instruction is used, it effectively slows down the processor’s internal clock and thus its response time to incoming interrupts. The one-cycle response time of the standard idle state is increased by \( n \), the clock divisor. When an enabled interrupt is received, the ADSP-2185 will remain in the idle state for up to a maximum of \( n \) processor cycles \((n = 16, 32, 64 \) or 128\) before resuming normal operation.

When the IDLE \((n)\) instruction is used in systems that have an externally generated serial clock (SCLK), the serial clock rate may be faster than the processor’s reduced internal clock rate. Under these conditions, interrupts must not be generated at a faster rate than can be serviced, due to the additional time the processor takes to come out of the idle state (a maximum of \( n \) processor cycles).

SYSTEM INTERFACE
Figure 2 shows typical basic system configurations with the ADSP-2185, two serial devices, a byte-wide EPROM and optional external program and data overlay memories (mode selectable). Programmable wait state generation allows the processor to easily connect to slow peripheral devices. The ADSP-2185 also provides four external interrupts and two serial ports or six external interrupts and one serial port.

Host Memory mode allows access to the full external data bus, but limits addressing to a single address bit (A0). Additional system peripherals can be added in this mode through the use of external hardware to generate and latch address signals.
The ADSP-2185 uses an input clock with a frequency equal to half the instruction rate; a 16.67 MHz input clock yields a 30 ns processor cycle (which is equivalent to 33 MHz). Normally, instructions are executed in a single processor cycle. All device timing is relative to the internal instruction clock rate, which is indicated by the CLKOUT signal when enabled.

Because the ADSP-2185 includes an on-chip oscillator circuit, an external crystal may be used. The crystal should be connected across the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 3. Capacitor values are dependent on crystal type and should be specified by the crystal manufacturer. A parallel-resonant, fundamental frequency, microprocessor-grade crystal should be used.

A clock output (CLKOUT) signal is generated by the processor at the processor's cycle rate. This can be enabled and disabled by the CLKDIS bit in the SPORT0 Autobuffer Control Register.

**Figure 3. External Crystal Connections**

**Reset**

The RESET signal initiates a master reset of the ADSP-2185. The RESET signal must be asserted during the power-up sequence to assure proper initialization. **RESET** during initial power-up must be held long enough to allow the internal clock to stabilize. If **RESET** is activated any time after power-up, the clock continues to run and does not require stabilization time.

The power-up sequence is defined as the total time required for the crystal oscillator circuit to stabilize after a valid VDD is applied to the processor, and for the internal phase-locked loop (PLL) to lock onto the specific crystal frequency. A minimum of 2000 CLKIN cycles ensures that the PLL has locked, but does not include the crystal oscillator start-up time. During this power-up sequence the **RESET** signal should be held low. On any subsequent resets, the **RESET** signal must meet the minimum pulse width specification, t_{RP}.

The **RESET** input contains some hysteresis; however, if you use an RC circuit to generate your **RESET** signal, the use of an external Schmidt trigger is recommended.

The master reset sets all internal stack pointers to the empty stack condition, masks all interrupts and clears the MSTAT register. When **RESET** is released, if there is no pending bus request and the chip is configured for booting, the boot-loading sequence is performed. The first instruction is fetched from on-chip program memory location 0x0000 once boot loading completes.

**MEMORY ARCHITECTURE**

The ADSP-2185 provides a variety of memory and peripheral interface options. The key functional groups are Program Memory, Data Memory, Byte Memory and I/O.

**Program Memory** is a 24-bit-wide space for storing both instruction opcodes and data. The ADSP-2185 has 16K words of Program memory RAM on chip, and the capability of accessing up to two 8K external memory overlay spaces using the external data bus. Both an instruction opcode and a data value can be read from on-chip program memory in a single cycle.

**Data Memory** is a 16-bit-wide space used for the storage of data variables and for memory-mapped control registers. The ADSP-2185 has 16K words of Data memory RAM on chip, consisting of 16,352 user-accessible locations and 32 memory-mapped registers. Support also exists for up to two 8K external memory overlay spaces through the external data bus.

**Byte Memory (Full Memory Mode)** provides access to an 8-bit wide memory space through the Byte DMA (BDMA) port. The Byte memory interface provides access to 4 MBytes of memory by utilizing eight data lines as additional address lines. This gives the BDMA Port an effective 22-bit address range. On power-up, the DSP can automatically load bootstrap code from byte memory.

**I/O Space (Full Memory Mode)** allows access to 2048 locations of 16-bit-wide data. It is intended to be used to communicate with parallel peripheral devices such as data converters and external registers or latches.

**Program Memory**

The ADSP-2185 contains a 16K × 24 on-chip program RAM. The on-chip program memory is designed to allow up to two accesses each cycle so that all operations can complete in a single cycle. In addition, the ADSP-2185 allows the use of 8K external memory overlays.

The program memory space organization is controlled by the Mode B pin and the PMOVLAY register. Normally, the ADSP-2185 is configured with Mode B = 0 and program memory organized as shown in Figure 4.

<table>
<thead>
<tr>
<th>PROGRAM MEMORY</th>
<th>ADDRESS</th>
</tr>
</thead>
<tbody>
<tr>
<td>8K INTERNAL (PMOVLAY = 0, MODE B = 0)</td>
<td>0x3FFF</td>
</tr>
<tr>
<td>OR</td>
<td></td>
</tr>
<tr>
<td>EXTERNAL 8K (PMOVLAY = 1 or 2, MODE B = 0)</td>
<td>0x2000</td>
</tr>
<tr>
<td>8K INTERNAL</td>
<td>0x1FFF</td>
</tr>
<tr>
<td></td>
<td>0x0000</td>
</tr>
</tbody>
</table>

**Figure 4. Program Memory (Mode B = 0)**

There are 16K words of memory accessible internally when the PMOVLAY register is set to 0. When PMOVLAY is set to something other than 0, external accesses occur at addresses 0x2000 through 0x3FFF. The external address is generated as shown in Table II.
Table II.

<table>
<thead>
<tr>
<th>PMOVLAY</th>
<th>Memory</th>
<th>A13</th>
<th>A12:0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Internal</td>
<td>Not Applicable</td>
<td>Not Applicable</td>
</tr>
<tr>
<td>1</td>
<td>External</td>
<td>0</td>
<td>13 LSBs of Address Between 0x2000 and 0x3FFF</td>
</tr>
<tr>
<td>2</td>
<td>External</td>
<td>1</td>
<td>13 LSBs of Address Between 0x2000 and 0x3FFF</td>
</tr>
</tbody>
</table>

This organization provides for two external 8K overlay segments using only the normal 14 address bits. This allows for simple program overlays using one of the two external segments in place of the on-chip memory. Care must be taken in using this overlay space in that the processor core (i.e., the sequencer) does not take into account the PMOVLAY register value. For example, if a loop operation was occurring on one of the external overlays and the program changes to another external overlay or internal memory, an incorrect loop operation could occur. In addition, care must be taken in interrupt service routines as the overlay registers are not automatically saved and restored on the processor mode stack.

When Mode B = 1, booting is disabled and overlay memory is disabled (PMOVLAY must be 0). Figure 5 shows the memory map in this configuration.

Figure 5. Program Memory (Mode B = 1)

Data Memory
The ADSP-2185 has 16,352 16-bit words of internal data memory. In addition, the ADSP-2185 allows the use of 8K external memory overlays. Figure 6 shows the organization of the data memory.

Table III.

<table>
<thead>
<tr>
<th>DMOVLAY</th>
<th>Memory</th>
<th>A13</th>
<th>A12:0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Internal</td>
<td>Not Applicable</td>
<td>Not Applicable</td>
</tr>
<tr>
<td>1</td>
<td>External</td>
<td>0</td>
<td>13 LSBs of Address Between 0x2000 and 0x3FFF</td>
</tr>
<tr>
<td>2</td>
<td>External</td>
<td>1</td>
<td>13 LSBs of Address Between 0x2000 and 0x3FFF</td>
</tr>
</tbody>
</table>

This organization allows for two external 8K overlays using only the normal 14 address bits. All internal accesses complete in one cycle. Accesses to external memory are timed using the wait states specified by the DWAIT register.

I/O Space (Full Memory Mode)
The ADSP-2185 supports an additional external memory space called I/O space. This space is designed to support simple connections to peripherals or to bus interface ASIC data registers. I/O space supports 2048 locations. The lower eleven bits of the external address bus are used; the upper three bits are undefined. Two instructions were added to the core ADSP-2100 Family instruction set to read from and write to I/O memory space. The I/O space also has four dedicated 3-bit wait state registers, IOWAIT0-3, which specify up to seven wait states to be automatically generated for each of four regions. The wait states act on address ranges as shown in Table IV.

Table IV.

<table>
<thead>
<tr>
<th>Address Range</th>
<th>Wait State Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000-0x1FF</td>
<td>IOWAIT0</td>
</tr>
<tr>
<td>0x200-0x3FF</td>
<td>IOWAIT1</td>
</tr>
<tr>
<td>0x400-0x5FF</td>
<td>IOWAIT2</td>
</tr>
<tr>
<td>0x600-0x7FF</td>
<td>IOWAIT3</td>
</tr>
</tbody>
</table>

Composite Memory Select (CMS)
The ADSP-2185 has a programmable memory select signal that is useful for generating memory select signals for memories mapped to more than one space. The CMS signal is generated to have the same timing as each of the individual memory select signals (PMS, DMS, BMS, IOMS), but can combine their functionality.

When set, each bit in the CMSSEL register causes the CMS signal to be asserted when the selected memory select is asserted. For example, to use a 32K word memory to act as both program and data memory, set the PMS and DMS bits in the CMSSEL register and use the CMS pin to drive the chip select of the memory and use either DMS or PMS as the additional address bit.

The CMS pin functions as the other memory select signals, with the same timing and bus request logic. A 1 in the enable bit causes the assertion of the CMS signal at the same time as the
selected memory select signal. All enable bits, except the BMS bit, default to 1 at reset.

**Byte Memory**
The byte memory space is a bidirectional, 8-bit-wide, external memory space used to store programs and data. Byte memory is accessed using the BDMA feature. The byte memory space consists of 256 pages, each of which is 16K × 8.

The byte memory space on the ADSP-2185 supports read and write operations as well as four different data formats. The byte memory uses data bits 15:8 for data. The byte memory uses data bits 23:16 and address bits 13:0 to create a 22-bit address. This allows up to a 4 meg × 8 (32 megabit) ROM or RAM to be used without glue logic. All byte memory accesses are timed by the BM_WAIT register.

**Byte Memory DMA (BDMA, Full Memory Mode)**
The Byte memory DMA controller allows loading and storing of program instructions and data using the byte memory space. The BDMA circuit is able to access the byte memory space while the processor is operating normally and steals only one DSP cycle per 8-, 16- or 24-bit word transferred.

The BDMA circuit supports four different data formats, which are selected by the BTYPE register field. The appropriate number of 8-bit accesses are done from the byte memory space to build the word size selected. Table V shows the data formats supported by the BDMA circuit.

**Table V.**

<table>
<thead>
<tr>
<th>BTYPE</th>
<th>Internal Memory Space</th>
<th>Word Size</th>
<th>Alignment</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Program Memory</td>
<td>24</td>
<td>Full Word</td>
</tr>
<tr>
<td>01</td>
<td>Data Memory</td>
<td>16</td>
<td>Full Word</td>
</tr>
<tr>
<td>10</td>
<td>Data Memory</td>
<td>8</td>
<td>MSBs</td>
</tr>
<tr>
<td>11</td>
<td>Data Memory</td>
<td>8</td>
<td>LSBs</td>
</tr>
</tbody>
</table>

Unused bits in the 8-bit data memory formats are filled with 0s. The BIAD register field is used to specify the starting address for the on-chip memory involved with the transfer. The 14-bit BEAD register specifies the starting address for the external byte memory space. The 8-bit BM_PAGE register specifies the starting page for the external byte memory space. The BDIR register field selects the direction of the transfer. Finally the 14-bit BW_COUNT register specifies the number of DSP words to transfer and initiates the BDMA circuit transfers.

BDMA accesses can cross page boundaries during sequential addressing. A BDMA interrupt is generated on the completion of the number of transfers specified by the BW_COUNT register. The BW_COUNT register is updated after each transfer so it can be used to check the status of the transfers. When it reaches zero, the transfers have finished and a BDMA interrupt is generated. The BM_PAGE and BEAD registers must not be accessed by the DSP during BDMA operations.

The source or destination of a BDMA transfer will always be on-chip program or data memory, regardless of the values of Mode B, PMOVLAY or DM OVLAY.

When the BW_COUNT register is written with a nonzero value, the BDMA circuit starts executing byte memory accesses with wait states set by BM_WAIT. These accesses continue until the count reaches zero. When enough accesses have occurred to create a destination word, it is transferred to or from on-chip memory. The transfer takes one DSP cycle. DSP accesses to external memory have priority over BDMA byte memory accesses.

The BDMA Context Reset bit (BCR) controls whether the processor is held off while the BDMA accesses are occurring. Setting the BCR bit to 0 allows the processor to continue operations. Setting the BCR bit to 1 causes the processor to stop execution while the BDMA accesses are occurring, to clear the context of the processor and to start execution at address 0 when the BDMA accesses have completed.

**Internal Memory DMA Port (IDMA Port; Host Memory Mode)**
The IDMA Port provides an efficient means of communication between a host system and the ADSP-2185. The port is used to access the on-chip program memory and data memory of the DSP with only one DSP cycle per word overhead. The IDMA port cannot, however, be used to write to the DSP’s memory-mapped control registers.

The IDMA port has a 16-bit multiplexed address and data bus and supports 24-bit program memory. The IDMA port is completely asynchronous and can be written to while the ADSP-2185 is operating at full speed.

The DSP memory address is latched and then automatically incremented after each IDMA transaction. An external device can therefore access a block of sequentially addressed memory by specifying only the starting address of the block. This increases throughput as the address does not have to be sent for each memory access.

IDMA Port access occurs in two phases. The first is the IDMA Address Latch cycle. When the acknowledge is asserted, a 14-bit address and 1-bit destination type can be driven onto the bus by an external device. The address specifies an on-chip memory location, the destination type specifies whether it is a D M or PM access. The falling edge of the address latch signal latches this value into the IDMA A register.

Once the address is stored, data can then be either read from or written to the ADSP-2185’s on-chip memory. Asserting the select line (IS) and the appropriate read or write line (IRD and IWR respectively) signals the ADSP-2185 that a particular transaction is required. In either case, there is a one-processor-cycle delay for synchronization. The memory access consumes one additional processor cycle.

Once an access has occurred, the latched address is automatically incremented and another access can occur.

Through the IDMA A register, the DSP can also specify the starting address and data format for DMA operation.

**Bootstrap Loading (Booting)**
The ADSP-2185 has two mechanisms to allow automatic loading of the internal program memory after reset. The method for booting is controlled by the Mode A, B and C configuration bits as shown in Table VI. These four states can be compressed into two-state bits by allowing an IDMA boot with Mode C = 1.

However, three bits are used to ensure future compatibility with parts containing internal program memory ROM.

**BDMA Booting**

When the Mode pins specify BDMA booting, the ADSP-2185 initiates a BDMA boot sequence when RESET is released.
ADSP-2185

Table VI. Boot Summary Table

<table>
<thead>
<tr>
<th>MODE C</th>
<th>MODE B</th>
<th>MODE A</th>
<th>Booting Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Full Memory Mode.</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>No Automatic boot operations occur. Program execution starts at external memory location 0. Chip is configured in Full Memory Mode. BDMA can still be used but the processor does not automatically use or wait for these operations.</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Host Mode. Additional interface hardware is required.</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>IDMA feature is used to load any internal memory as desired. Program execution is held off until internal program memory location 0 is written to. Chip is configured in Host Mode.</td>
</tr>
</tbody>
</table>

The BDMA interface is set up during reset to the following defaults when BDMA booting is specified: the BD IR, BM PAGE, BIAD and BEAD registers are set to 0; the BTYPE register is set to 0 to specify program memory 24 bit words; and the BWCOUNT register is set to 32. This causes 32 words of on-chip program memory to be loaded from byte memory. These 32 words are used to set up the BDMA to load in the remaining program code. The BCR bit is also set to 1, which causes program execution to be held off until all 32 words are loaded into on-chip program memory. Execution then begins at address 0.

The ADSP-2100 Family development software (Revision 5.02 and later) fully supports the BDMA booting feature and can generate IDMA compatible boot code. The IDLE instruction can also be used to allow the processor to hold off execution while booting continues through the BDMA interface. For BDMA accesses while in Host Mode, the addresses to boot memory must be constructed externally to the ADSP-2185. The only memory address bit provided by the processor is A0.

IDMA Port Booting
The ADSP-2185 can also boot programs through its Internal DMA port. If Mode C = 1, Mode B = 0 and Mode A = 1, the ADSP-2185 boots from the IDMA port. IDMA feature can load as much on-chip memory as desired. Program execution is held off until on-chip program memory location 0 is written to.

The ADSP-2100 Family development software (Revision 5.02 and later) can generate IDMA compatible boot code.

Bus Request & Bus Grant
The ADSP-2185 can relinquish control of the data and address buses to an external device. When the external device requires access to memory, it asserts the bus request (BR) signal. If the ADSP-2185 is not performing an external memory access, it responds to the active BR input in the following processor cycle by:
- Three-stating the data and address buses and the PMS, DMS, BMS, CMS, IOMS, RD, WR output drivers,
- Asserting the bus grant (BG) signal and
- Halting program execution.

If Go Mode is enabled, the ADSP-2185 will not halt program execution until it encounters an instruction that requires an external memory access.

If the ADSP-2185 is performing an external memory access when the external device asserts the BR signal, then it will not three-state the memory interfaces or assert the BG signal until the processor cycle after the access completes. The instruction does not need to be completed when the bus is granted. If a single instruction requires two external memory accesses, the bus will be granted between the two accesses.

When the BR signal is released, the processor releases the BG signal, reenables the output drivers and continues program execution from the point where it stopped.

The bus request feature operates at all times, including when the processor is booting and when RESET is active.

The BGH pin is asserted when the ADSP-2185 is ready to execute an instruction but is stopped because the external bus is already granted to another device. The other device can release the bus by deasserting bus request. Once the bus is released, the ADSP-2185 deasserts BG and BGH and executes the external memory access.

Flag I/O Pins
The ADSP-2185 has eight general purpose programmable input/output flag pins. They are controlled by two memory mapped registers. The PTYPE register determines the direction, 1 = output and 0 = input. The PFDATA register is used to read and write the values on the pins. Data being read from a pin configured as an input is synchronized to the ADSP-2185's clock. Bits that are programmed as outputs will read the value being output. The PF pins default to input during reset.

In addition to the programmable flags, the ADSP-2185 has five fixed-mode flags, FLAG_IN, FLAG_OUT, FL0, FL1 and FL2. FL0-FL2 are dedicated output flags. FLAG_IN and FLAG_OUT are available as an alternate configuration of SPORT1.

Note: Pins PF0, PF1 and PF2 are also used for device configuration during reset.
BIASED ROUNDING
A mode is available on the ADSP-2185 to allow biased rounding in addition to the normal unbiased rounding. When the BIASRND bit is set to 0, the normal unbiased rounding operations occur. When the BIASRND bit is set to 1, biased rounding occurs instead of the normal unbiased rounding. When operating in biased rounding mode all rounding operations with MR0 set to 0x8000 will round up, rather than only rounding up odd MR1 values.

For example:

<table>
<thead>
<tr>
<th>MR Value Before RND</th>
<th>Biased RND Result</th>
<th>Unbiased RND Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>00-0000-8000</td>
<td>00-0001-8000</td>
<td>00-0000-8000</td>
</tr>
<tr>
<td>00-0001-8000</td>
<td>00-0002-8000</td>
<td>00-0001-8000</td>
</tr>
<tr>
<td>00-0000-8001</td>
<td>00-0001-8001</td>
<td>00-0000-8001</td>
</tr>
<tr>
<td>00-0001-8001</td>
<td>00-0002-8001</td>
<td>00-0001-8001</td>
</tr>
<tr>
<td>00-0000-7FFF</td>
<td>00-0000-7FFF</td>
<td>00-0000-7FFF</td>
</tr>
<tr>
<td>00-0001-7FFF</td>
<td>00-0001-7FFF</td>
<td>00-0001-7FFF</td>
</tr>
</tbody>
</table>

This mode only has an effect when the MR0 register contains 0x8000; all other rounding operations work normally. This mode allows more efficient implementation of bit-specified algorithms that use biased rounding, for example the GSM speech compression routines. Unbiased rounding is preferred for most algorithms.

Note: BIASRND bit is Bit 12 of the SPORT0 Autobuffer Control register.

Instruction Set Description
The ADSP-2185 assembly language instruction set has an algebraic syntax that was designed for ease of coding and readability. The assembly language, which takes full advantage of the processor’s unique architecture, offers the following benefits:

- The algebraic syntax eliminates the need to remember cryptic assembler mnemonics. For example, a typical arithmetic add instruction, such as AR = AX0 + AY0, resembles a simple equation.

- Every instruction assembles into a single, 24-bit word that can execute in a single instruction cycle.

- The syntax is a superset ADSP-2100 Family assembly language and is completely source and object code compatible with other family members. Programs may need to be relocated to use on-chip memory and conform to the ADSP-2185’s interrupt vector and reset vector map.

- Sixteen condition codes are available. For conditional jump, call, return or arithmetic instructions, the condition can be checked and the operation executed in the same instruction cycle.

- Multifunction instructions allow parallel execution of an arithmetic instruction with up to two fetches or one write to processor memory space during a single instruction cycle.

I/O Space Instructions
The instructions used to access the ADSP-2185’s I/O memory space are as follows:

Syntax: IO(addr) = dreg
          dreg = IO(addr);

where addr is an address value between 0 and 2047 and dreg is any of the 16 data registers.

Examples: IO(23) = AR0;
          AR1 = IO(17);

Description: The I/O space read and write instructions move data between the data registers and the I/O memory space.

DESIGNING AN EZ-ICE®-COMPATIBLE SYSTEM
The ADSP-2185 has on-chip emulation support and an ICE-Port™*, a special set of pins that interface to the EZ-ICE®*. These features allow in-circuit emulation without replacing the target system processor by using only a 14-pin connection from the target system to the EZ-ICE®*. Target systems must have a 14-pin connector to accept the EZ-ICE®’s in-circuit probe, a 14-pin plug. See the ADSP-2100 Family EZ-Tools data sheet for complete information on ICE products.

The ICE-Port™* interface consists of the following ADSP-2185 pins:

- EBR
- EBG
- ERESET
- EMS
- EINT
- ECLK
- ELIN
- EOUT
- EE

These ADSP-2185 pins must be connected only to the EZ-ICE®’s connector in the target system. These pins have no function except during emulation, and do not require pull-up or pull-down resistors. The traces for these signals between the ADSP-2185 and the connector must be kept as short as possible, no longer than three inches.

The following pins are also used by the EZ-ICE®:

- BR
- BG
- RESET
- GND

The EZ-ICE® uses the EE (emulator enable) signal to take control of the ADSP-2185 in the target system. This causes the processor to use its ERESET, EBR and EBG pins instead of the RESET, BR and BG pins. The BG output is three-stated. These signals do not need to be jumper-isolated in your system.

The EZ-ICE® connects to your target system via a ribbon cable and a 14-pin female plug. The female plug is plugged onto the 14-pin connector (a pin strip header) on the target board.
ADSP-2185

Target Board Connector for EZ-ICE®* Probe
The EZ-ICE®* connector (a standard pin strip header) is shown in Figure 7. You must add this connector to your target board design if you intend to use the EZ-ICE®*. Be sure to allow enough room in your system to fit the EZ-ICE®* probe onto the 14-pin connector.

![Figure 7. Target Board Connector for EZ-ICE®*](image)

Key:
- GND
- EBG
- EBR
- KEY (NO PIN)
- EOUT
- EE
- RESET
- 1G
- 2
- 3
- 4
- 5
- 6
- 7
- 8
- 9
- 10
- 11
- 12
- 13
- 14
- BR
- ECLK
- EMS
- ERESET
- TOP VIEW

Target Memory Interface
For your target system to be compatible with the EZ-ICE®* emulator, it must comply with the memory interface guidelines listed below.

PM, DM, BM, IOM and CM
Design your Program Memory (PM), Data Memory (DM), Byte Memory (BM), I/O Memory (IOM) and Composite Memory (CM) external interfaces to comply with worst case device timing requirements and switching characteristics as specified in this DSP's data sheet. The performance of the EZ-ICE®* may approach published worst case specification for some memory access timing requirements and switching characteristics.

Note: If your target does not meet the worst case chip specification for memory access parameters, you may not be able to emulate your circuitry at the desired CLKIN frequency. Depending on the severity of the specification violation, you may have trouble manufacturing your system as DSP components statistically vary in switching characteristic and timing requirements within published limits.

Restriction: All memory strobe signals on the ADSP-2185 (RD, WR, PMS, DMS, BMS, CMS and IOMS) used in your target system must have 10 kΩ pull-up resistors connected when the EZ-ICE®* is being used. The pull-up resistors are necessary because there are no internal pull-ups to guarantee their state during prolonged three-state conditions resulting from typical EZ-ICE®* debugging sessions. These resistors may be removed at your option when the EZ-ICE®* is not being used.

Target System Interface Signals
When the EZ-ICE®* board is installed, the performance on some system signals change. Design your system to be compatible with the following system interface signal changes introduced by the EZ-ICE®* board:

- EZ-ICE®* emulation introduces an 8 ns propagation delay between your target circuitry and the DSP on the RESET signal.
- EZ-ICE®* emulation introduces an 8 ns propagation delay between your target circuitry and the DSP on the BR signal.
- EZ-ICE®* emulation ignores RESET and BR when single-stepping.
- EZ-ICE®* emulation ignores the state of target BR in certain modes. As a result, the target system may take control of the DSP's external memory bus only if bus grant (BG) is asserted by the EZ-ICE®* board's DSP.
### RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>K Grade</th>
<th>B Grade</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>4.5</td>
<td>4.5</td>
</tr>
<tr>
<td>$T_{AMB}$</td>
<td>0</td>
<td>-40</td>
</tr>
</tbody>
</table>

### ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>K/B Grades</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>Hi-Level Input Voltage$^{1,2}$</td>
<td>$V_{DD} = \text{max}$</td>
<td>2.0</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Lo-Level Input Voltage$^{1,3}$</td>
<td>$V_{DD} = \text{max}$</td>
<td>2.2</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Hi-Level Output Voltage$^{1,4,5}$</td>
<td>$I_{OH} = -0.5 \text{mA}$</td>
<td>2.4</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Lo-Level Output Voltage$^{1,4,5}$</td>
<td>$V_{DD} = \text{min}$</td>
<td>0.4</td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>Hi-LevelInput Current$^{3}$</td>
<td>$V_{IN} = V_{DD} \text{max}$</td>
<td>10</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Lo-Level Input Current$^{3}$</td>
<td>$V_{IN} = 0 \text{V}$</td>
<td>10</td>
</tr>
<tr>
<td>$I_{OZH}$</td>
<td>Three-State Leakage Current$^{7}$</td>
<td>$V_{DD} = \text{max}$</td>
<td>10</td>
</tr>
<tr>
<td>$I_{OZL}$</td>
<td>Three-State Leakage Current$^{7}$</td>
<td>$V_{DD} = 0 \text{V}$</td>
<td>10</td>
</tr>
<tr>
<td>$I_{DD}$</td>
<td>Supply Current (Idle)$^{9}$</td>
<td>$V_{DD} = 5.0$</td>
<td>12.4</td>
</tr>
<tr>
<td>$I_{DD}$</td>
<td>Supply Current (Dynamic)$^{10}$</td>
<td>$T_{AMB} = +25^\circ \text{C}$</td>
<td>63</td>
</tr>
<tr>
<td>$C_{I}$</td>
<td>Input Pin Capacitance$^{3,6,12}$</td>
<td>$V_{IN} = 2.5 \text{V}$</td>
<td>8</td>
</tr>
<tr>
<td>$C_{O}$</td>
<td>Output Pin Capacitance$^{6,7,12,13}$</td>
<td>$T_{AMB} = +25^\circ \text{C}$</td>
<td>8</td>
</tr>
</tbody>
</table>

### NOTES

1. Bidirectional pins: D0–D23, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A1–A13, PF0–PF7.
2. Input only pins: BR, DR0, DR1, PWD.
3. Input only pins: CLKIN, REF, BR, DR0, DR1, PWD.
4. Output pins: BG, PMS, DM, BMS, IOMS, CMS, RD, WR, PWDACK, A0, DT0, DT1, CLKOUT, FL2-0, BGH.
5. Although specified for TTL outputs, all ADSP-2185 outputs are CMOS-compatible and will drive to $V_{DD}$ and GND, assuming no dc loads.
6. Guaranteed but not tested.
7. Guaranteed but not tested.
8. Three-statable pins: A0–A13, D0–D23, PMS, DM, BMS, IOMS, CMS, RD, WR, DT0, DT1, SCLK0, SCLK1, TFS0, TFS1, RSF0, RSF1, PF0–PF7.
9. Output pin capacitance is the capacitive load for any three-stated output pin.

Specifications subject to change without notice.
**ADSP-2185**

**ABSOLUTE MAXIMUM RATINGS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>-0.3 V to +7 V</td>
</tr>
<tr>
<td>Input Voltage</td>
<td>-0.3 V to +VDD + 0.3 V</td>
</tr>
<tr>
<td>Output Voltage Swing</td>
<td>-0.3 V to +VDD + 0.3 V</td>
</tr>
<tr>
<td>Operating Temperature (Ambient)</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
</tr>
<tr>
<td>Lead Temperature (5 sec)</td>
<td>TQFP +280°C</td>
</tr>
</tbody>
</table>

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**ESD SENSITIVITY**

The ADSP-2185 is an ESD (electrostatic discharge) sensitive device. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur to devices subjected to high energy electrostatic discharges.

The ADSP-2185 features proprietary ESD protection circuitry to dissipate high energy discharges (Human Body Model) per method 3015 of MIL-STD-883. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination before devices are removed.

**ADSP-2185 TIMING PARAMETERS**

**GENERAL NOTES**

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add up parameters to derive longer times.

**TIMING NOTES**

Switching characteristics specify how the processor changes its signals. You have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell you what the processor will do in a given circumstance. You can also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

**MEMORY TIMING SPECIFICATIONS**

The table below shows common memory device specifications and the corresponding ADSP-2185 timing parameters, for your convenience.

<table>
<thead>
<tr>
<th>Memory Device Specification</th>
<th>ADSP-2185 Timing Parameter</th>
<th>Timing Parameter Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Address Setup to Write Start</td>
<td>tASW</td>
<td>A0-A13, xMS Setup before WR Low</td>
</tr>
<tr>
<td>Address Setup to Write End</td>
<td>tAW</td>
<td>A0-A13, xMS Setup before WR D asserted</td>
</tr>
<tr>
<td>Address Hold Time</td>
<td>tWRA</td>
<td>A0-A13, xMS Hold before WR Low</td>
</tr>
<tr>
<td>Data Setup Time</td>
<td>tDW</td>
<td>Data Setup before WR High</td>
</tr>
<tr>
<td>Data Hold Time</td>
<td>tDH</td>
<td>Data Hold after WR High</td>
</tr>
<tr>
<td>OE to Data Valid</td>
<td>tRDD</td>
<td>RD Low to Data Valid</td>
</tr>
<tr>
<td>Address Access Time</td>
<td>tRA</td>
<td>A0-A13, xMS to Data Valid</td>
</tr>
</tbody>
</table>

**FREQUENCY DEPENDENCY FOR TIMING SPECIFICATIONS**

\[ t_{CK} = 0.5t_{CKI} \]

The ADSP-2185 uses an input clock with a frequency equal to half the instruction rate: a 16.67 MHz input clock (which is equivalent to 60 ns) yields a 30 ns processor cycle (equivalent to 33 MHz). \( t_{CK} \) values within the range of 0.5\( t_{CKI} \) period should be substituted for all relevant timing parameters to obtain the specification value.

Example: \( t_{CKH} = 0.5t_{CK} - 7 \text{ ns} = 0.5 (30 \text{ ns}) - 7 \text{ ns} = 8 \text{ ns} \)
ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating:

\[ T_{\text{AMB}} = T_{\text{CASE}} - (PD \times \theta_{\text{CA}}) \]

- \( T_{\text{AMB}} \): Ambient temperature in \(^\circ\text{C}\)
- \( T_{\text{CASE}} \): Case temperature in \(^\circ\text{C}\)
- \( PD \): Power Dissipation in W
- \( \theta_{\text{CA}} \): Thermal Resistance (Case-to-Ambient)
- \( \theta_{\text{JA}} \): Thermal Resistance (Junction-to-Ambient)
- \( \theta_{\text{JC}} \): Thermal Resistance (Junction-to-Case)

Package

<table>
<thead>
<tr>
<th>Package</th>
<th>( \theta_{\text{JA}} )</th>
<th>( \theta_{\text{JC}} )</th>
<th>( \theta_{\text{CA}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>TQFP</td>
<td>50°C/W</td>
<td>2°C/W</td>
<td>48°C/W</td>
</tr>
</tbody>
</table>

POWER DISSIPATION

To determine total power dissipation in a specific application, the following equation should be applied for each output:

\[ P_{\text{INT}} + (C \times V_{\text{DD}}^2 \times \frac{1}{f}) \]

- \( C \): Load capacitance
- \( f \): Output switching frequency

**Example:**

In an application where external data memory is used and no other outputs are active, power dissipation is calculated as follows:

**Assumptions:**
- External data memory is accessed every cycle with 50% of the address pins switching.
- External data memory writes occur every other cycle with 50% of the data pins switching.
- Each address and data pin has a 10 pF total load at the pin.
- The application operates at \( V_{\text{DD}} = 5.0 \) V and \( t_{\text{CK}} = 30 \) ns.

**Total Power Dissipation:**

\[ P_{\text{INT}} = \text{internal power dissipation from Power vs. Frequency graph (Figure 8).} \]

\[ (C \times V_{\text{DD}}^2 \times \frac{1}{f}) \text{ is calculated for each output:} \]

<table>
<thead>
<tr>
<th># of Pins</th>
<th>( C )</th>
<th>( V_{\text{DD}}^2 \times \frac{1}{f} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Address, DMS</td>
<td>8 ( \times 10 ) pF ( \times 5^2 ) V ( \times 33.3 ) MHz</td>
<td>66.6 mW</td>
</tr>
<tr>
<td>Data Output, WR</td>
<td>9 ( \times 10 ) pF ( \times 5^2 ) V ( \times 16.67 ) M Hz</td>
<td>37.5 mW</td>
</tr>
<tr>
<td>RD</td>
<td>1 ( \times 10 ) pF ( \times 5^2 ) V ( \times 16.67 ) M Hz</td>
<td>4.2 mW</td>
</tr>
<tr>
<td>CLKOUT</td>
<td>1 ( \times 10 ) pF ( \times 5^2 ) V ( \times 33.3 ) M Hz</td>
<td>8.3 mW</td>
</tr>
</tbody>
</table>

Total power dissipation for this example is \( P_{\text{INT}} + 116.6 \) mW.

Figure 8. Power vs. Frequency
CAPACITIVE LOADING

Figures 9 and 10 show the capacitive loading characteristics of the ADSP-2185.

**Figure 9.** Typical Output Rise Time vs. Load Capacitance, $C_L$ (at Maximum Ambient Operating Temperature)

**Figure 10.** Typical Output Valid Delay or Hold vs. Load Capacitance, $C_L$ (at Maximum Ambient Operating Temperature)

**TEST CONDITIONS**

**Output Disable Time**

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high impedance state. The output disable time ($t_{DIS}$) is the difference of $t_{MEASURED}$ and $t_{DECAY}$, as shown in the Output Enable/Disable diagram. The time is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage. The decay time, $t_{DECAY}$, is dependent on the capacitive load, $C_L$, and the current load, $I_L$, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \times 0.5V}{I_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

**Output Enable Time**

Output pins are considered to be enabled when they have made a transition from a high-impedance state to when they start driving. The output enable time ($t_{ENA}$) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

**Figure 11.** Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

**Figure 12.** Output Enable/Disable

**Figure 13.** Equivalent Device Loading for AC Measurements (Including All Fixtures)
## TIMING PARAMETERS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Clock Signals and Reset</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(t_{CKI})</td>
<td>60</td>
<td>150</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{CKIL})</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>(t_{CKIH})</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

Switching Characteristics:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(t_{CKL})</td>
<td>0.5 (t_{CK}) - 7</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>(t_{CKH})</td>
<td>0.5 (t_{CK}) - 7</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>(t_{CKOH})</td>
<td>0</td>
<td>20</td>
<td>ns</td>
</tr>
</tbody>
</table>

**Control Signals**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(t_{RSP})</td>
<td>5 (t_{CK})</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>(t_{MS})</td>
<td>2</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>(t_{MH})</td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

### NOTE

\(^1\) Applies after power-up sequence is complete. Internal phase lock loop requires no more than 2000 \(t_{CKI}\) cycles assuming stable \(t_{CKI}\) (not including crystal oscillator start-up time).

---

![Figure 14. Clock Signals](image-url)
### Parameter

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Interrupts and Flag</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tIFS, IRQx, FI, or PFx Setup before CLKOUT Low</td>
<td>0.25 tCK + 15 ns</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tIFH, IRQx, FI, or PFx Hold after CLKOUT High</td>
<td>0.25 tCK ns</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

**Switching Characteristics:**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>tFOH, Flag Output Hold after CLKOUT Low</td>
<td>0.5 tCK – 7 ns</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tFOD, Flag Output Delay from CLKOUT Low</td>
<td>0.25 tCK + 5 ns</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

**NOTES**

1. If IRQx and FI inputs meet tIFS and tIFH setup/hold requirements, they will be recognized during the current clock cycle; otherwise the signals will be recognized on the following cycle. (Refer to “Interrupt Controller Operation” in the Program Control chapter of the ADSP-2100 Family User’s Manual for further information on interrupt servicing.)

2. Edge-sensitive interrupts require pulse widths greater than 10 ns; level-sensitive interrupts must be held low until serviced.

3. tIFS = IRQ0, IRQ1, IRQ2, IRQL0, IRQL1, IRQE.

4. PFx = PF0, PF1, PF2, PF3, PF4, PF5, PF6, PF7.

5. Flag outputs = PFx, FL0, FL1, FL2, Flag_out.

---

*Figure 15. Interrupts and Flags*
### Bus Request/Grant

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Timing Requirements:</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{BH}$</td>
<td>BR Hold after CLKOUT High$^1$</td>
<td>$0.25 \ t_{CK} + 2$</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{BS}$</td>
<td>BR Setup before CLKOUT Low$^1$</td>
<td>$0.25 \ t_{CK} + 17$</td>
<td>ns</td>
</tr>
<tr>
<td><strong>Switching Characteristics:</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{SD}$</td>
<td>CLKOUT High to $xMS$, RD, WR Disable</td>
<td>$0.25 \ t_{CK} + 10$</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{SDB}$</td>
<td>$xMS$, RD, WR Disable to BG Low</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{SE}$</td>
<td>BG High to $xMS$, RD, WR Enable</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{SEC}$</td>
<td>$xMS$, RD, WR Enable to CLKOUT Hig</td>
<td>$0.25 \ t_{CK} - 7$</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{SDBH}$</td>
<td>$xMS$, RD, WR Disable to BGH Low$^2$</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{SEH}$</td>
<td>BGH High to $xMS$, RD, WR Enable$^2$</td>
<td>0</td>
<td>ns</td>
</tr>
</tbody>
</table>

**NOTES**

$xMS = PMS, DMS, CMS, IOMS, BMS$

$^1$BR is an asynchronous signal. If BR meets the setup/hold requirements, it will be recognized during the current clock cycle; otherwise the signal will be recognized on the following cycle. Refer to the ADSP-2100 Family User’s Manual for BR/BG cycle relationships.

$^2$BGH is asserted when the bus is granted and the processor requires control of the bus to continue.

![Figure 16. Bus Request-Bus Grant](image-url)
Parameter | Min | Max | Unit
--- | --- | --- | ---
Memory Read | | | |
Timing Requirements:
\( t_{RD\text{D}} \) | RD Low to Data Valid | 0.5 \( t_{CK} \) - 9 + w | ns
\( t_{AA} \) | A0-A13, xMS to Data Valid | 0.75 \( t_{CK} \) - 10.5 + w | ns
\( t_{RD\text{H}} \) | Data Hold from RD High | 0 | ns
Switching Characteristics:
\( t_{RP} \) | RD Pulse Width | 0.5 \( t_{CK} \) - 5 + w | ns
\( t_{CRD} \) | CLKOUT High to RD Low | 0.25 \( t_{CK} \) - 5 | 0.25 \( t_{CK} \) + 7 | ns
\( t_{ASR} \) | A0-A13, xMS Setup before RD Low | 0.25 \( t_{CK} \) - 6 | ns
\( t_{RDA} \) | A0-A13, xMS Hold after RD Deasserted | 0.25 \( t_{CK} \) - 3 | ns
\( t_{RWR} \) | RD High to RD or WR Low | 0.5 \( t_{CK} \) - 5 | ns

\( w = \text{wait states} \times t_{CK} \)

\( xMS = \text{PMS, DMS, CMS, IOMS, BMS} \)

Figure 17. Memory Read
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Data Setup before WR High</strong></td>
<td>0.5 tₜₜₜₜₜ - 7 + w</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td><strong>Data Hold after WR High</strong></td>
<td>0.25 tₜₜₜₜₜ - 2</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td><strong>WR Pulse Width</strong></td>
<td>0.5 tₜₜₜₜₜ - 5 + w</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td><strong>WR Low to Data Enabled</strong></td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td><strong>A0–A13, xMS Setup before WR Low</strong></td>
<td>0.25 tₜₜₜₜₜ - 6</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td><strong>Data Disable before WR or RD Low</strong></td>
<td>0.25 tₜₜₜₜₜ - 7</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td><strong>CLKOUT High to WR Low</strong></td>
<td>0.25 tₜₜₜₜₜ - 5</td>
<td>0.25 tₜₜₜₜₜ + 7</td>
<td>ns</td>
</tr>
<tr>
<td><strong>A0–A13, xMS, Setup before WR D asserted</strong></td>
<td>0.75 tₜₜₜₜₜ - 9 + w</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td><strong>A0–A13, xMS Hold after WR D asserted</strong></td>
<td>0.25 tₜₜₜₜₜ - 3</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td><strong>WR High to RD or WR Low</strong></td>
<td>0.5 tₜₜₜₜₜ - 5</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

w = wait states × tₜₜₜₜₜ
xMS = PMS, DMS, CMS, IOMS, BMS

Figure 18. Memory Write
## Serial Ports

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
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<tbody>
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<td><strong>Timing Requirements</strong></td>
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<tr>
<td>tSCK</td>
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<td>tSCS</td>
<td>4</td>
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<td>tSCH</td>
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<td>ns</td>
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<td>tSCP</td>
<td>20</td>
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<td><strong>Switching Characteristics</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tCC</td>
<td></td>
<td>0.25 tCK</td>
<td>0.25 tCK + 10</td>
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<tr>
<td>tSCDE</td>
<td></td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>tSCDV</td>
<td></td>
<td>15</td>
<td>ns</td>
</tr>
<tr>
<td>tRH</td>
<td></td>
<td>0</td>
<td>ns</td>
</tr>
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<td>tRD</td>
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<td>15</td>
<td>ns</td>
</tr>
<tr>
<td>tSCDH</td>
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<td>ns</td>
</tr>
<tr>
<td>tTDE</td>
<td></td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>tTDV</td>
<td></td>
<td>14</td>
<td>ns</td>
</tr>
<tr>
<td>tSCDD</td>
<td></td>
<td>15</td>
<td>ns</td>
</tr>
<tr>
<td>tRDV</td>
<td></td>
<td>15</td>
<td>ns</td>
</tr>
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</table>

Figure 19. Serial Ports
## IDMA Address Latch

### Timing Requirements:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{IALP}$</td>
<td></td>
<td>10</td>
<td>ns</td>
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<tr>
<td>$t_{IASU}$</td>
<td>5</td>
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<td>ns</td>
</tr>
<tr>
<td>$t_{IAH}$</td>
<td>2</td>
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<td>ns</td>
</tr>
<tr>
<td>$t_{IKA}$</td>
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<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{IALS}$</td>
<td>3</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

### Notes:

1. Start of Address Latch = $IS$ Low and $IAL$ High.
2. Start of Write or Read = $IS$ Low and $IWR$ Low or $IRD$ Low.
3. End of Address Latch = $IS$ High or $IAL$ Low.

![Diagram of IDMA Address Latch](image)

**Figure 20. IDMA Address Latch**
**Parameter** | **Min** | **Max** | **Unit**
--- | --- | --- | ---
**IDMA Write, Short Write Cycle**
Timing Requirements:
\( t_{IKW} \) IACK Low before Start of Write\(^3\) | 0 | ns
\( t_{IWP} \) Duration of Write\(^1, 2\) | 15 | ns
\( t_{IDSU} \) IAD 15–0 Data Setup before End of Write\(^2, 3, 4\) | 5 | ns
\( t_{IDH} \) IAD 15–0 Data Hold after End of Write\(^2, 3, 4\) | 2 | ns
Switching Characteristics:
\( t_{IKHW} \) Start of Write to IACK High | 15 | ns

**NOTES**
\(^1\)Start of Write = \( IS \) Low and \( IWR \) Low.
\(^2\)End of Write = \( IS \) High or \( IWR \) High.
\(^3\)If Write Pulse ends before IACK Low, use specifications \( t_{IDSU} \), \( t_{IDH} \).
\(^4\)If Write Pulse ends after IACK Low, use specifications \( t_{IKSU} \), \( t_{IKH} \).

---

**Figure 21. IDMA Write, Short Write Cycle**
Parameter Min Max Unit

**IDMA Write, Long Write Cycle**

Timing Requirements:
- $t_{IKW}$: IACK Low before Start of Write\(^1\) 0 ns
- $t_{IKSU}$: IAD 15-0 Data Setup before IACK Low\(^2, 3, 4\) 0.5 $t_{CK}$ + 10 ns
- $t_{IKH}$: IAD 15-0 Data Hold after IACK Low\(^2, 3, 4\) 2 ns

Switching Characteristics:
- $t_{IKLW}$: Start of Write to IACK Low\(^4\) 1.5 $t_{CK}$ ns
- $t_{IKHW}$: Start of Write to IACK High 15 ns

**NOTES**

1. Start of Write = IS Low and IWR Low.
2. If Write Pulse ends before IACK Low, use specifications $t_{IDSU}$, $t_{IDH}$.
3. If Write Pulse ends after IACK Low, use specifications $t_{IKSU}$, $t_{IKH}$.
4. This is the earliest time for IACK Low from Start of Write. For IDMA Write cycle relationships, please refer to the ADSP-2100 Family User’s Manual.

![Figure 22. IDMA Write, Long Write Cycle](image-url)
### Parameter

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>IDMA Read, Long Read Cycle</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Timing Requirements:</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{IKR}$</td>
<td>IACK Low before Start of Read$^1$</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{IRP}$</td>
<td>Duration of Read$^1$</td>
<td>15</td>
<td>ns</td>
</tr>
<tr>
<td><strong>Switching Characteristics:</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{IKHR}$</td>
<td>IACK High after Start of Read$^1$</td>
<td>15</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{IKDS}$</td>
<td>IAD 15–0 Data Setup before IACK Low</td>
<td>0.5 $t_{CK}$ – 10</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{IKDH}$</td>
<td>IAD 15–0 Data Hold after End of Read$^2$</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{IKDD}$</td>
<td>IAD 15–0 Data Disabled after End of Read$^2$</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{IRDV}$</td>
<td>IAD 15–0 Previous Data Enabled after Start of Read</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{RDE}$</td>
<td>IAD 15–0 Previous Data Valid after Start of Read</td>
<td>15</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{RDH1}$</td>
<td>IAD 15–0 Previous Data Hold after Start of Read (DM/PM1)$^3$</td>
<td>2 $t_{CK}$ – 5</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{RDD2}$</td>
<td>IAD 15–0 Previous Data Hold after Start of Read (PM2)$^4$</td>
<td>$t_{CK}$ – 5</td>
<td>ns</td>
</tr>
</tbody>
</table>

**NOTES**

$^1$Start of Read = IS Low and IRD Low.

$^2$End of Read = IS High or IRD High.

$^3$DM read or first half of PM read.

$^4$Second half of PM read.

---

**Figure 23. IDMA Read, Long Read Cycle**
### IDMA Read, Short Read Cycle

**Timing Requirements:**
- **$t_{IKR}$** IACK Low before Start of Read\(^1\)  
  - Min: 0  
  - Max: 15  
  - Unit: ns

- **$t_{IRP}$** Duration of Read  
  - Min: 15  
  - Max: 15  
  - Unit: ns

**Switching Characteristics:**
- **$t_{IKHR}$** IACK High after Start of Read\(^1\)  
  - Min: 0  
  - Max: 15  
  - Unit: ns

- **$t_{KDH}$** IAD 15–0 Data Hold after End of Read\(^2\)  
  - Min: 0  
  - Max: 10  
  - Unit: ns

- **$t_{KDD}$** IAD 15–0 Data Disabled after End of Read\(^2\)  
  - Min: 0  
  - Max: 10  
  - Unit: ns

- **$t_{RDE}$** IAD 15–0 Previous Data Enabled after Start of Read  
  - Min: 0  
  - Max: 15  
  - Unit: ns

- **$t_{RDV}$** IAD 15–0 Previous Data Valid after Start of Read  
  - Min: 0  
  - Max: 15  
  - Unit: ns

**NOTES**
- \(^1\)Start of Read = IS Low and IRD Low.
- \(^2\)End of Read = IS High or IRD High.

---

![Diagram](image-url)

*Figure 24. IDMA Read, Short Read Cycle*
The ADSP-2185 package pinout is shown in the table below. Pin names in **bold** text replace the plain text named functions when Mode C = 1. A + sign separates two functions when either function can be active for either major I/O mode. Signals enclosed in brackets [ ] are state bits latched from the value of the pin at the deassertion of RESET.

### TQFP Pin Configurations

<table>
<thead>
<tr>
<th>TQFP Number</th>
<th>Pin Name</th>
<th>TQFP Number</th>
<th>Pin Name</th>
<th>TQFP Number</th>
<th>Pin Name</th>
<th>TQFP Number</th>
<th>Pin Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>A4/IAD3</td>
<td>26</td>
<td>IRQE + PF4</td>
<td>51</td>
<td>EBR</td>
<td>76</td>
<td>D16</td>
</tr>
<tr>
<td>2</td>
<td>A5/IAD4</td>
<td>27</td>
<td>IRQLO + PF5</td>
<td>52</td>
<td>BR</td>
<td>77</td>
<td>D17</td>
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<tr>
<td>3</td>
<td>GND</td>
<td>28</td>
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<td>53</td>
<td>EBG</td>
<td>78</td>
<td>D18</td>
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<td>4</td>
<td>A6/IAD5</td>
<td>29</td>
<td>IRQ1 + PF6</td>
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<td>BG</td>
<td>79</td>
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<td>5</td>
<td>A7/IAD6</td>
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<td>IRQ2 + PF7</td>
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<td>D0/IAD13</td>
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<td>6</td>
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<td>DT0</td>
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<td>D1/IAD14</td>
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<td>A9/IAD8</td>
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<td>TFS0</td>
<td>57</td>
<td>D2/IAD15</td>
<td>82</td>
<td>D21</td>
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<td>8</td>
<td>A10/IAD9</td>
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<td>RFS0</td>
<td>58</td>
<td>D3/IACK</td>
<td>83</td>
<td>D22</td>
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<td>9</td>
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<td>DR0</td>
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<td>VDD</td>
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<td>VDD</td>
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<td>D4/I5</td>
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<td>DT1</td>
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<td>D5/I5AL</td>
<td>87</td>
<td>FL0</td>
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<td>D6/I5RD</td>
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<td>18</td>
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<td>D9</td>
<td>93</td>
<td>PF1 [Mode B]</td>
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<td>75</td>
<td>D15</td>
<td>100</td>
<td>A3/IAD2</td>
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</table>
**ADSP-2185**

**OUTLINE DIMENSIONS**

Dimensions shown in inches and millimeters.

**100-Lead Metric Thin Plastic Quad Flatpack (TQFP) (ST-100)**

---

**OUTLINE DIMENSIONS**

Dimensions shown in inches and millimeters.

**100-Lead Metric Thin Plastic Quad Flatpack (TQFP) (ST-100)**

---

**ORDERING GUIDE**

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Ambient Temperature Range</th>
<th>Instruction Rate (MHz)</th>
<th>Package Description</th>
<th>Package Option*</th>
</tr>
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<tbody>
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<td>ADSP-2185KST-115</td>
<td>0°C to +70°C</td>
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<td>ST-100</td>
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<td>100-Lead TQFP</td>
<td>ST-100</td>
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<td>100-Lead TQFP</td>
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<td>33.3</td>
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<td>ST-100</td>
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*ST = Plastic Thin Quad Flatpack (TQFP).