SHARC DSP Microcomputer

Enhanced Product

ADSP-21065L-EP

SUMMARY

High performance signal computer for communications, audio, automotive, instrumentation, medical, military, and industrial applications

Super Harvard Architecture Computer (SHARC) — four independent buses for dual data, instruction, and I/O fetch on a single cycle

32-bit fixed-point arithmetic; 32-bit and 40-bit floating-point arithmetic

544K bits on-chip SRAM memory and integrated I/O peripheral

I^2S support, for eight simultaneous receive and transmit channels

ENHANCED PRODUCT (EP) FEATURES

Supports defense and aerospace applications (AQEC standard)

Extended temperature range –55°C to +110°C

Controlled manufacturing baseline

One package assembly/test site

One wafer fabrication site

Enhanced product change notification

Qualification data available upon request

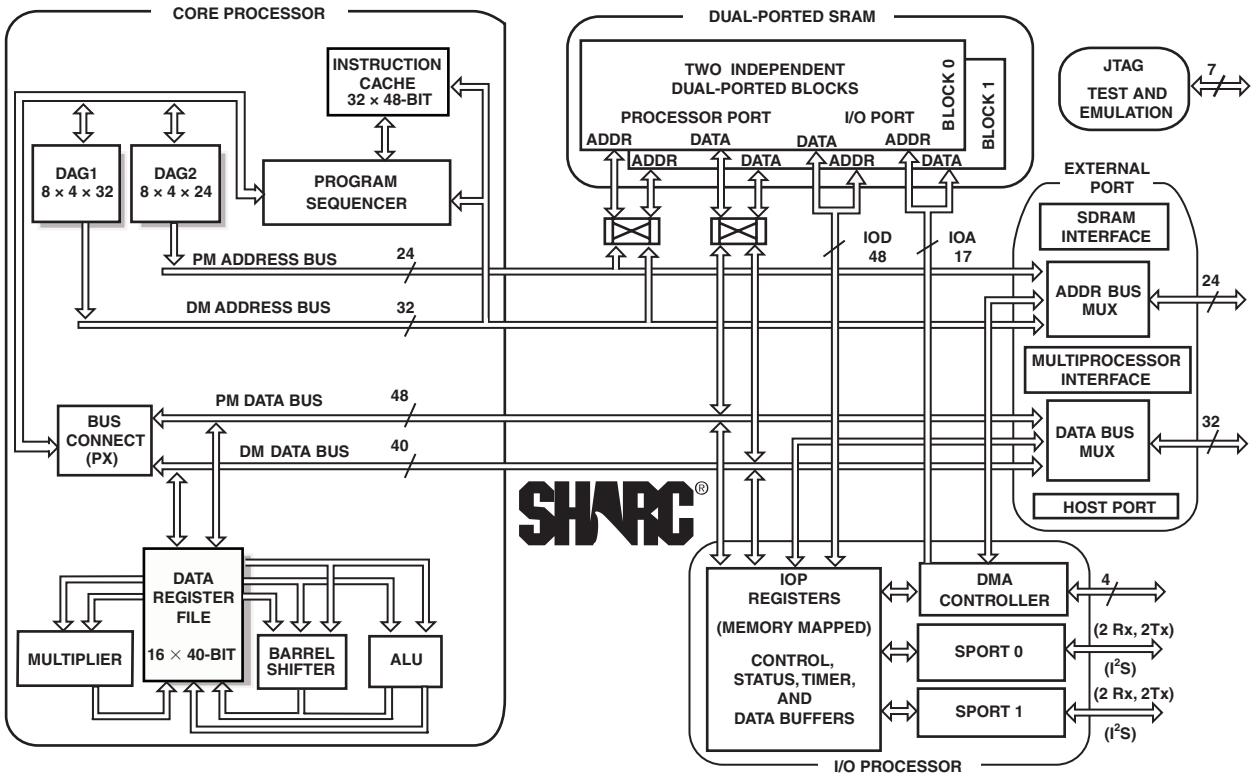

Figure 1. Functional Block Diagram

Rev. B Document Feedback

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Tel: 781.329.4700 **Technical Support** **www.analog.com**

FEATURES

60 MIPS, 180 MFLOPS peak, 120 MFLOPS sustained performance
User-configurable 544K bits on-chip SRAM memory
Two external port, DMA channels and eight serial port, DMA channels
SDRAM controller for glueless interface to low cost external memory (@ 60 MHz)
64M words external address range
12 programmable I/O pins and two timers with event capture options
Code-compatible with ADSP-2106x family
208-lead MQFP package
Matte tin terminal finish
3.3 Volt operation

Flexible Data Formats and 40-Bit Extended Precision
32-bit single-precision and 40-bit extended-precision IEEE floating-point data formats
32-bit fixed-point data format, integer and fractional, with dual 80-bit accumulators

Parallel Computations
Single-cycle multiply and ALU operations in parallel with dual memory read/writes and instruction fetch
Multiply with add and subtract for accelerated FFT butterfly computation
1024-point complex FFT benchmark: 301 µs (18,221 cycles)

544K bits Configurable On-Chip SRAM
Dual-ported for independent access by core processor and DMA
Configurable in combinations of 16-, 32-, 48-bit data and program words in Block 0 and Block 1

DMA Controller
Ten DMA channels—two dedicated to the external port and eight dedicated to the serial ports
Background DMA transfers at up to 60 MHz, in parallel with full speed processor execution
Performs transfers between:
Internal RAM and host
Internal RAM and serial ports
Internal RAM and master or slave SHARC
Internal RAM and external memory or I/O devices
External memory and external devices

Host Processor Interface
Efficient interface to 8-, 16-, and 32-bit microprocessors
Host can directly read/write ADSP-21065L-EP IOP registers

Multiprocessing
Distributed on-chip bus arbitration for glueless, parallel bus connect between two ADSP-21065L-EP processors plus host
120M bytes/sec transfer rate over parallel bus

Serial Ports
Independent transmit and receive functions
Programmable 3-bit to 32-bit serial word width
I^2S support allowing eight transmit and eight receive channels
Glueless interface to industry standard codecs
TDM multichannel mode with µ-law/A-law hardware companding
Multichannel signaling protocol

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REVISION HISTORY

9/2017—Rev. A to Rev. B

Change to Features 2
Change to Endnote 1, Ordering Guide 13

GENERAL DESCRIPTION

The ADSP-21065L-EP is a powerful member of the SHARC® family of 32-bit processors optimized for cost sensitive applications. The SHARC (Super Harvard Architecture) processors offer the highest levels of performance and memory integration of any 32-bit DSP in the industry—they are also the only DSPs in the industry that offer both fixed and floating-point capabilities, without compromising precision or performance.

The ADSP-21065L-EP is fabricated in a high speed, low power CMOS process, 0.35 µm technology. With its on-chip instruction cache, the processor can execute every instruction in a single cycle. Table 1 lists the performance benchmarks for the ADSP-21065L-EP.

The ADSP-21065L-EP SHARC combines a floating-point DSP core with integrated, on-chip system features, including a 544K bit SRAM memory, host processor interface, DMA controller, SDRAM controller, and enhanced serial ports.

Figure 1 shows a block diagram of the ADSP-21065L-EP, illustrating the following architectural features:

- Computation units (ALU, multiplier, and shifter) with a shared data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- Timers with event capture modes
- On-chip, dual-ported SRAM
- External port for interfacing to off-chip memory and peripherals
- Host port and SDRAM interface
- DMA controller
- Enhanced serial ports
- JTAG test access port

Table 1. Performance Benchmarks

Benchmark	Timing	Cycles
Cycle Time	16.5 ns	1
1024-Point Complex FFT (Radix 4, with Digit Reverse)	301 µs	18,221
Matrix Multiply (Pipelined)		
[3 × 3] × [3 × 1]	148.5 ns	9
[4 × 4] × [4 × 1]	264 ns	16
FIR Filter (per Tap)	16.5 ns	1
IIR Filter (per Biquad)	66 ns	4
Divide (y/x)	99 ns	6
Inverse Square Root	148.5 ns	9
DMA Transfers	240M bytes/s	

Full details about this enhanced product are available in the ADSP-21065L data sheet, which should be used in conjunction with this data sheet.

PIN FUNCTION DESCRIPTIONS

The ADSP-21065L-EP pin definitions are listed below. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$).

Unused inputs should be tied or pulled to VDD or GND, except for $ADDR_{23-0}$, $DATA_{31-0}$, $FLAG_{11-0}$, $\overline{\text{SW}}$, and inputs that have internal pull-up or pull-down resistors ($\overline{\text{CPA}}$, ACK, DTxX, DRxX, TCLKx, RCLKx, TMS, and TDI)—these pins can be left floating. These pins have a logic-level hold circuit that prevents the input from floating internally.

Table 2. Pin Descriptions

Pin	Type	Function
$ADDR_{23-0}$	I/O/T	**External Bus Address.** The ADSP-21065L-EP outputs addresses for external memory and peripherals on these pins. In a multiprocessor system, the bus master outputs addresses for read/writes of the IOP registers of the other ADSP-21065L-EP processors. The ADSP-21065L-EP inputs addresses when a host processor or multiprocessing bus master is reading or writing its IOP registers.
$DATA_{31-0}$	I/O/T	**External Bus Data.** The ADSP-21065L-EP inputs and outputs data and instructions on these pins. The external data bus transfers 32-bit single-precision floating-point data and 32-bit fixed-point data over bits 31–0. 16-bit short word data is transferred over bits 15–0 of the bus. Pull-up resistors on unused DATA pins are not necessary.
$\overline{\text{MS}}_{3-0}$	I/O/T	**Memory Select Lines.** These lines are asserted as chip selects for the corresponding banks of external memory. Internal $ADDR_{25-24}$ are decoded into $\overline{\text{MS}}_{3-0}$. The $\overline{\text{MS}}_{3-0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the $\overline{\text{MS}}_{3-0}$ lines are inactive; they are active, however, when a conditional memory access instruction is executed, whether or not the condition is true. Additionally, an $\overline{\text{MS}}_{3-0}$ line which is mapped to SDRAM may be asserted even when no SDRAM access is active. In a multiprocessor system, the $\overline{\text{MS}}_{3-0}$ lines are output by the bus master.
$\overline{\text{RD}}$	I/O/T	**Memory Read Strobe.** This pin is asserted when the ADSP-21065L-EP reads from external memory devices or from the IOP register of another ADSP-21065L-EP. External devices (including another ADSP-21065L-EP) must assert $\overline{\text{RD}}$ to read from the ADSP-21065L-EP's IOP registers. In a multiprocessing system, $\overline{\text{RD}}$ is output by the bus master and is input by another ADSP-21065L-EP.
$\overline{\text{WR}}$	I/O/T	**Memory Write Strobe.** This pin is asserted when the ADSP-21065L-EP writes to external memory devices or to the IOP register of another ADSP-21065L-EP. External devices must assert $\overline{\text{WR}}$ to write to the ADSP-21065L-EP's IOP registers. In a multiprocessing system, $\overline{\text{WR}}$ is output by the bus master and is input by the other ADSP-21065L-EP.
$\overline{\text{SW}}$	I/O/T	**Synchronous Write Select.** This signal interfaces the ADSP-21065L-EP to synchronous memory devices (including another ADSP-21065L-EP). The ADSP-21065L-EP asserts $\overline{\text{SW}}$ to provide an early indication of an impending write cycle, which can be aborted if $\overline{\text{WR}}$ is not later asserted (e.g., in a conditional write instruction). In a multiprocessing system, $\overline{\text{SW}}$ is output by the bus master and is input by the other ADSP-21065L-EP to determine if the multiprocessor access is a read or write. $\overline{\text{SW}}$ is asserted at the same time as the address output.
ACK	I/O/S	**Memory Acknowledge.** External devices can deassert ACK to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access. The ADSP-21065L-EP deasserts ACK as an output to add waitstates to a synchronous access of its IOP registers. In a multiprocessing system, a slave ADSP-21065L-EP deasserts the bus master's ACK input to add wait state(s) to an access of its IOP registers. The bus master has a keeper latch on its ACK pin that maintains the input at the level to which it was last driven.
$\overline{\text{SBTS}}$	I/S	**Suspend Bus Three-State.** External devices can assert $\overline{\text{SBTS}}$ to place the external bus address, data, selects, and strobes—but not SDRAM control pins—in a high impedance state for the following cycle. If the ADSP-21065L-EP attempts to access external memory while $\overline{\text{SBTS}}$ is asserted, the processor will halt and the memory access will not finish until $\overline{\text{SBTS}}$ is deasserted. $\overline{\text{SBTS}}$ should only be used to recover from host processor/ADSP-21065L-EP deadlock.
$\overline{\text{IRQ}}_{2-0}$	I/A	**Interrupt Request Lines.** May be either edge-triggered or level-sensitive.

A = Asynchronous, G = Ground, I = Input, O = Output, P = Power Supply, S = Synchronous, (A/D) = Active Drive, (O/D) = Open Drain, T = Three-State (when $\overline{\text{SBTS}}$ is asserted, or when the ADSP-21065L-EP is a bus slave)

Table 2. Pin Descriptions (Continued)

Pin	Type	Function
$FLAG_{11-0}$	I/O/A	**Flag Pins.** Each is configured via control bits as either an input or output. As an input, they can be tested as a condition. As an output, they can be used to signal external peripherals.
$\overline{HBR}$	I/A	**Host Bus Request.** This pin must be asserted by a host processor to request control of the ADSP-21065L-EP's external bus. When $\overline{HBR}$ is asserted in a multiprocessing system, the ADSP-21065L-EP that is bus master will relinquish the bus and assert $\overline{HBG}$. To relinquish the bus, the ADSP-21065L-EP places the address, data, select, and strobe lines in a high impedance state. It does, however, continue to drive the SDRAM control pins. $\overline{HBR}$ has priority over all ADSP-21065L-EP bus requests ($\overline{BR}_{2-1}$) in a multiprocessing system.
$\overline{HBG}$	I/O	**Host Bus Grant.** Acknowledges an $\overline{HBR}$ bus request, indicating that the host processor may take control of the external bus. $\overline{HBG}$ is asserted by the ADSP-21065L-EP until $\overline{HBR}$ is released. In a multiprocessing system, $\overline{HBG}$ is output by the ADSP-21065L-EP bus master.
$\overline{CS}$	I/A	**Chip Select.** Asserted by host processor to select the ADSP-21065L-EP.
REDY (O/D)	O	**Host Bus Acknowledge.** The ADSP-21065L-EP deasserts REDY to add wait states to an asynchronous access of its internal memory or IOP registers by a host. This pin is an open-drain output (O/D) by default; it can be programmed in the ADREDY bit of the SYSCON register to be active drive (A/D). REDY will only be output if the $\overline{CS}$ and $\overline{HBR}$ inputs are asserted.
$\overline{DMAR}_1$	I/A	**DMA Request 1** (DMA Channel 9).
$\overline{DMAR}_2$	I/A	**DMA Request 2** (DMA Channel 8).
$\overline{DMAG}_1$	O/T	**DMA Grant 1** (DMA Channel 9).
$\overline{DMAG}_2$	O/T	**DMA Grant 2** (DMA Channel 8).
$\overline{BR}_{2-1}$	I/O/S	**Multiprocessing Bus Requests.** Used by multiprocessing ADSP-21065L-EP processors to arbitrate for bus master-ship. An ADSP-21065L-EP only drives its own $\overline{BR}$x line (corresponding to the value of its ID_{2-0} inputs) and monitors all others. In a uniprocessor system, tie both $\overline{BR}$x pins to VDD.
ID_{1-0}	I	**Multiprocessing ID.** Determines which multiprocessor bus request ($\overline{BR}_1$–$\overline{BR}_2$) is used by the ADSP-21065L-EP. ID = 01 corresponds to $\overline{BR}_1$, ID = 10 corresponds to $\overline{BR}_2$. ID = 00 in single-processor systems. These lines are a system configuration selection that should be hardwired or changed at reset only.
$\overline{CPA}$ (O/D)	I/O	**Core Priority Access.** Asserting its $\overline{CPA}$ pin allows the core processor of an ADSP-21065L-EP bus slave to interrupt background DMA transfers and gain access to the external bus. $\overline{CPA}$ is an open-drain output that is connected to all ADSP-21065L-EP processors in the system. The $\overline{CPA}$ pin has an internal 5 kΩ pull-up resistor. If core access priority is not required in a system, the $\overline{CPA}$ pin should be left unconnected.
DTxX	O	**Data Transmit (Serial Ports 0, 1; Channels A, B).** Each DTxX pin has a 50 kΩ internal pull-up resistor.
DRxX	I	**Data Receive (Serial Ports 0, 1; Channels A, B).** Each DRxX pin has a 50 kΩ internal pull-up resistor.
TCLKx	I/O	**Transmit Clock (Serial Ports 0, 1).** Each TCLK pin has a 50 kΩ internal pull-up resistor.
RCLKx	I/O	**Receive Clock (Serial Ports 0, 1).** Each RCLK pin has a 50 kΩ internal pull-up resistor.
TFSx	I/O	**Transmit Frame Sync (Serial Ports 0, 1).**
RFSx	I/O	**Receive Frame Sync (Serial Ports 0, 1).**
BSEL	I	**EPROM Boot Select.** When BSEL is high, the ADSP-21065L-EP is configured for booting from an 8-bit EPROM. When BSEL is low, the BSEL and $\overline{BMS}$ inputs determine booting mode. See $\overline{BMS}$ pin description below for details. This signal is a system configuration selection that should be hardwired.
$\overline{BMS}$	I/O/T*	**Boot Memory Select.** *Output*: Used as chip select for boot EPROM devices (when BSEL = 1). In a multiprocessor system, $\overline{BMS}$ is output by the bus master. *Input:* When low, indicates that no booting will occur and that ADSP-21065L-EP will begin executing instructions from external memory. See table below. This input is a system configuration selection that should be hardwired. *Three-statable only in EPROM boot mode (when $\overline{BMS}$ is an output). **BSEL** / **$\overline{BMS}$** / **Booting Mode** 1 / Output / EPROM (connect $\overline{BMS}$ to EPROM chip select.) 0 / 1 (Input) / Host processor (HBW [SYSCON] bit selects host bus width). 0 / 0 (Input) / No booting. Processor executes from external memory.

A = Asynchronous, G = Ground, I = Input, O = Output, P = Power Supply, S = Synchronous, (A/D) = Active Drive, (O/D) = Open Drain, T = Three-State (when $\overline{SBTS}$ is asserted, or when the ADSP-21065L-EP is a bus slave)

Table 2. Pin Descriptions (Continued)

Pin	Type	Function
CLKIN	I	**Clock In.** Used in conjunction with XTAL, configures the ADSP-21065L-EP to use either its internal clock generator or an external clock source. The external crystal should be rated at 1× frequency. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. The ADSP-21065L-EP's internal clock generator multiplies the 1× clock to generate 2× clock for its core and SDRAM. It drives 2× clock out on the SDCLKx pins for the SDRAM interface to use. See also SDCLKx. Connecting the 1× external clock to CLKIN while leaving XTAL unconnected configures the ADSP-21065L-EP to use the external clock source. The instruction cycle rate is equal to 2× CLKIN. CLKIN may not be halted, changed, or operated below the specified frequency.
$\overline{\text{RESET}}$	I/A	**Processor Reset.** Resets the ADSP-21065L-EP to a known state and begins execution at the program memory location specified by the hardware reset vector address. This input must be asserted at power-up.
TCK	I	**Test Clock (JTAG).** Provides an asynchronous clock for JTAG boundary scan.
TMS	I/S	**Test Mode Select (JTAG).** Used to control the test state machine. TMS has a 20 kΩ internal pull-up resistor.
TDI	I/S	**Test Data Input (JTAG).** Provides serial data for the boundary scan logic. TDI has a 20 kΩ internal pull-up resistor.
TDO	O	**Test Data Output (JTAG).** Serial scan output of the boundary scan path.
$\overline{\text{TRST}}$	I/A	**Test Reset (JTAG).** Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-21065L-EP. $\overline{\text{TRST}}$ has a 20 kΩ internal pull-up resistor.
$\overline{\text{EMU}}$ (O/D)	O	**Emulation Status.** Must be connected to the ADSP-21065L-EP EZ-ICE target board connector only.
BMSTR	O	**Bus Master Output.** In a multiprocessor system, indicates whether the ADSP-21065L-EP is current bus master of the shared external bus. The ADSP-21065L-EP drives BMSTR high only while it is the bus master. In a single-processor system (ID = 00), the processor drives this pin high.
$\overline{\text{CAS}}$	I/O/T	**SDRAM Column Access Strobe.** Provides the column address. In conjunction with $\overline{\text{RAS}}$, $\overline{\text{MS}}$x, $\overline{\text{SDWE}}$, SDCLKx, and sometimes SDA10, defines the operation for the SDRAM to perform.
$\overline{\text{RAS}}$	I/O/T	**SDRAM Row Access Strobe.** Provides the row address. In conjunction with $\overline{\text{CAS}}$, $\overline{\text{MS}}$x, $\overline{\text{SDWE}}$, SDCLKx, and sometimes SDA10, defines the operation for the SDRAM to perform.
$\overline{\text{SDWE}}$	I/O/T	**SDRAM Write Enable.** In conjunction with $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, $\overline{\text{MS}}$x, SDCLKx, and sometimes SDA10, defines the operation for the SDRAM to perform.
DQM	O/T	**SDRAM Data Mask.** In write mode, DQM has a latency of zero and is used to block write operations.
$\text{SDCLK}_{1\text{-}0}$	I/O/S/T	**SDRAM 2× Clock Output.** In systems with multiple SDRAM devices connected in parallel, supports the corresponding increased clock load requirements, eliminating need of off-chip clock buffers. Either SDCLK_1 or both SDCLKx pins can be three-stated.
SDCKE	I/O/T	**SDRAM Clock Enable.** Enables and disables the CLK signal. For details, see the data sheet supplied with your SDRAM device.
SDA10	O/T	**SDRAM A10 Pin.** Enables applications to refresh an SDRAM in parallel with a host access.
$\overline{\text{XTAL}}$	O	**Crystal Oscillator Terminal.** Used in conjunction with CLKIN to enable the ADSP-21065L-EP's internal clock generator or to disable it to use an external clock source. See CLKIN.
$\overline{\text{PWM\_EVENT}}_{1\text{-}0}$	I/O/A	**PWM Output/Event Capture.** In PWMOUT mode, is an output pin and functions as a timer counter. In WIDTH_CNT mode, is an input pin and functions as a pulse counter/event capture.
VDD	P	**Power Supply.** Nominally +3.3 V dc. (33 pins)
GND	G	**Power Supply Return.** (37 pins)
NC		**Do Not Connect.** Reserved pins which must be left open and unconnected. (7 pins)

A = Asynchronous, G = Ground, I = Input, O = Output, P = Power Supply, S = Synchronous, (A/D) = Active Drive, (O/D) = Open Drain, T = Three-State (when $\overline{\text{SBTS}}$ is asserted, or when the ADSP-21065L-EP is a bus slave)

SPECIFICATIONS

Note that component specifications are subject to change without notice. See Environmental Conditions for information on thermal specifications.

OPERATING CONDITIONS

Parameter	Description	Min	Max	Unit
V_{DD}	Supply Voltage	3.13	3.60	V
T_{CASE}	Case Operating Temperature	–55	+110	°C
V_{IH}	High Level Input Voltage @ V_{DD} = Max	2.0	V_{DD} + 0.5	V
V_{IL1}	Low Level Input Voltage @ V_{DD} = Max[1]	–0.5	0.8	V
V_{IL2}	Low Level Input Voltage @ V_{DD} = Min[2]	–0.5	0.7	V

[1] Applies to input and bidirectional pins: $DATA_{31–0}$, $ADDR_{23–0}$, BSEL, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $\overline{SBTS}$, $\overline{IRQ}_{2–0}$, $FLAG_{11–0}$, $\overline{HGB}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR}_{2–1}$, $\overline{ID}_{2–0}$, RPBA, $\overline{CPA}$, $\overline{TFS0}$, $\overline{TFS1}$, $\overline{RFS0}$, $\overline{RFS1}$, $\overline{BMS}$, TMS, TDI, TCK, $\overline{HBR}$, DR0A, DR1A, DR0B, DR1B, TCLK0, TCLK1, RCLK0, RCLK1, $\overline{RESET}$, $\overline{TRST}$, PWM_EVENT0, PWM_EVENT1, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, $\overline{SDCKE}$.

[2] Applies to input pin CLKIN.

ABSOLUTE MAXIMUM RATINGS

Stresses at or above those listed in Table 3 may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 3. Absolute Maximum Ratings

Parameter	Rating
Supply Voltage (V_{DD})	–0.3 V to +4.6 V
Input Voltage	–0.5 V to V_{DD} + 0.5 V
Output Voltage Swing	–0.5 V to V_{DD} + 0.5 V
Load Capacitance	200 pF
Storage Temperature Range	–65°C to +150°C
Lead Temperature (5 seconds)	280°C
Junction Temperature Under Bias	150°C

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE MARKING INFORMATION

Figure 2 and Table 4 provide information on detail contained within the package marking for the ADSP-21065L-EP processor (actual marking format may vary). For a complete listing of product availability, see Ordering Guide on Page 13.

Figure 2. Typical Package Brand

Table 4. Package Brand Information

Brand Key	Field Description
t	Temperature Range
pp	Package Type
ccc	See Ordering Guide
EP	Enhanced Processing
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
yyww	Date Code

ENVIRONMENTAL CONDITIONS

The ADSP-21065L-EP processor is rated for performance under T_{CASE} environmental conditions specified in the Operating Conditions on Page 8.

Thermal Characteristics

The ADSP-21060L-EP is offered in a 208-lead MQFP package.

The ADSP-21065L-EP is specified for a case temperature (T_{CASE}). To ensure that the T_{CASE} is not exceeded, an airflow source may be used.

$$T_{CASE} = T_{AMB} + (PD \times \theta_{CA})$$

T_{CASE} = Case temperature (measured on top surface of package)

PD = Power dissipation in W (this value depends upon the specific application)

θ_{JC} = 7.1°C/W

Table 5. Thermal Characteristics (208-Lead MQFP)

Parameter	Airflow (Linear Ft./Min.)	Typical	Unit
θ_{CA}	0	24	°C/W
θ_{CA}	100	20	°C/W
θ_{CA}	200	19	°C/W
θ_{CA}	400	17	°C/W
θ_{CA}	600	13	°C/W

208-LEAD MQFP PIN CONFIGURATION

Table 6. 208-Lead MQFP Pin Configuration

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	VDD	43	$\overline{CAS}$	85	VDD	127	DATA28	169	ADDR17
2	RFS0	44	$\overline{SDWE}$	86	DATA3	128	DATA29	170	ADDR16
3	GND	45	VDD	87	DATA4	129	GND	171	ADDR15
4	RCLK0	46	DQM	88	DATA5	130	VDD	172	VDD
5	DR0A	47	SDCKE	89	GND	131	VDD	173	ADDR14
6	DR0B	48	SDA10	90	DATA6	132	DATA30	174	ADDR13
7	TFS0	49	GND	91	DATA7	133	DATA31	175	ADDR12
8	TCLK0	50	$\overline{DMAG1}$	92	DATA8	134	FLAG7	176	VDD
9	VDD	51	$\overline{DMAG2}$	93	VDD	135	GND	177	GND
10	GND	52	$\overline{HBG}$	94	GND	136	FLAG6	178	ADDR11
11	DT0A	53	BMSTR	95	VDD	137	FLAG5	179	ADDR10
12	DT0B	54	VDD	96	DATA9	138	FLAG4	180	ADDR9
13	RFS1	55	$\overline{CS}$	97	DATA10	139	GND	181	GND
14	GND	56	$\overline{SBTS}$	98	DATA11	140	VDD	182	VDD
15	RCLK1	57	GND	99	GND	141	VDD	183	ADDR8
16	DR1A	58	$\overline{WR}$	100	DATA12	142	NC	184	ADDR7
17	DR1B	59	$\overline{RD}$	101	DATA13	143	ID1	185	ADDR6
18	TFS1	60	GND	102	NC	144	ID0	186	GND
19	TCLK1	61	VDD	103	NC	145	$\overline{EMU}$	187	GND
20	VDD	62	GND	104	DATA14	146	TDO	188	ADDR5
21	VDD	63	REDY	105	VDD	147	$\overline{TRST}$	189	ADDR4
22	DT1A	64	$\overline{SW}$	106	GND	148	TDI	190	ADDR3
23	DT1B	65	$\overline{CPA}$	107	DATA15	149	TMS	191	VDD
24	PWM_EVENT1	66	VDD	108	DATA16	150	GND	192	VDD
25	GND	67	VDD	109	DATA17	151	TCK	193	ADDR2
26	PWM_EVENT0	68	GND	110	VDD	152	BSEL	194	ADDR1
27	$\overline{BR1}$	69	ACK	111	DATA18	153	$\overline{BMS}$	195	ADDR0
28	$\overline{BR2}$	70	$\overline{MS0}$	112	DATA19	154	GND	196	GND
29	VDD	71	$\overline{MS1}$	113	DATA20	155	GND	197	FLAG0
30	CLKIN	72	GND	114	GND	156	VDD	198	FLAG1
31	XTAL	73	GND	115	NC	157	$\overline{RESET}$	199	FLAG2
32	VDD	74	$\overline{MS2}$	116	DATA21	158	VDD	200	VDD
33	GND	75	$\overline{MS3}$	117	DATA22	159	GND	201	FLAG3
34	SDCLK1	76	FLAG11	118	DATA23	160	ADDR23	202	NC
35	GND	77	VDD	119	GND	161	ADDR22	203	NC
36	VDD	78	FLAG10	120	VDD	162	ADDR21	204	GND
37	SDCLK0	79	FLAG9	121	DATA24	163	VDD	205	$\overline{IRQ0}$
38	$\overline{DMAR1}$	80	FLAG8	122	DATA25	164	ADDR20	206	$\overline{IRQ1}$
39	$\overline{DMAR2}$	81	GND	123	DATA26	165	ADDR19	207	$\overline{IRQ2}$
40	$\overline{HBR}$	82	DATA0	124	VDD	166	ADDR18	208	NC
41	GND	83	DATA1	125	GND	167	GND		
42	$\overline{RAS}$	84	DATA2	126	DATA27	168	GND		

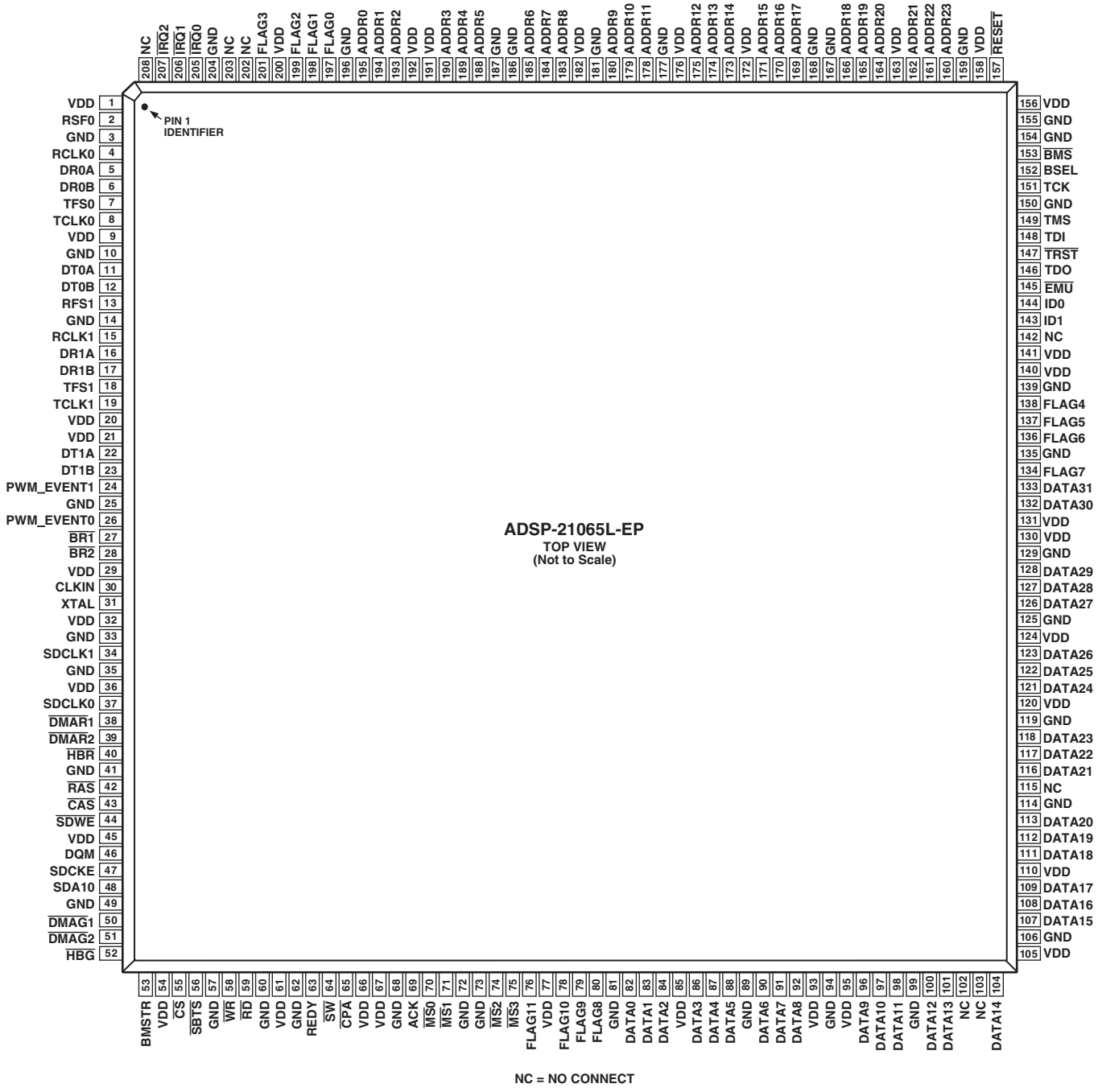
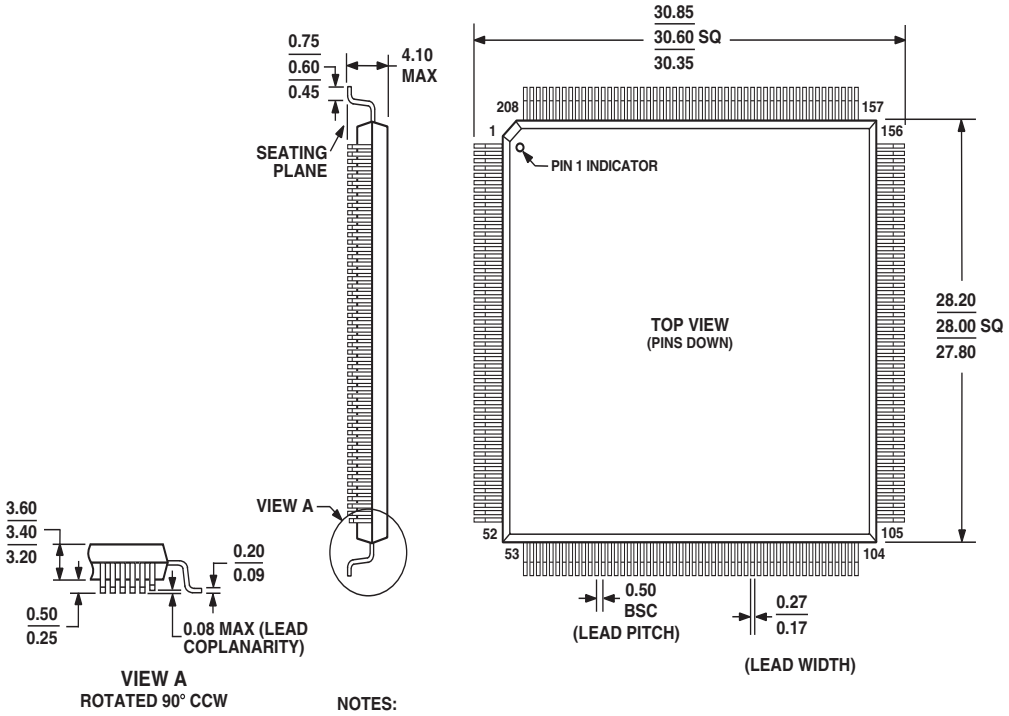


Figure 3. 208-Lead MQFP Pin Configuration

OUTLINE DIMENSIONS



NOTES:
1. THE ACTUAL POSITION OF EACH LEAD IS WITHIN 0.08 FROM ITS IDEAL POSITION WHEN MEASURED IN THE LATERAL DIRECTION.
2. CENTER DIMENSIONS ARE NOMINAL.
3. DIMENSIONS ARE IN MILLIMETERS AND COMPLY WITH JEDEC STANDARD MS-029, FA-1.

Figure 4. 208-Lead Metric Quad Flat Package [MQFP]
(S-208-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Notes	Temperature Range	Instruction Rate	On-Chip SRAM	Operating Voltage	Package Description	Package Option
ADSP21065LSS240-EP	[1]	–55°C to +110°C	60 MHz	544K Bit	3.3 V	208-Lead Metric Quad Flat Package	S-208-2

[1] Matte tin terminal finish.

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