FEATURES
- Precision Supply Voltage Monitor
  - 4.65 V ADM690A/ADM692A/ADM802L/M/ADM805L/M
  - 4.40 V ADM690A/ADM692A/ADM802M/ADM805M
- Reset Assertion Down to 1 V VCC
- Reset Timeout—200 ms
- Watchdog Timer—1.6 s
- 100 µA Quiescent Supply Current
- Automatic Battery Backup Power Switching
- Voltage Monitor for Power Fail
- ±2% Power Fail Accuracy on ADM802L/M
- Space-Saving MicroSOIC Package (ADM690A)

APPLICATIONS
- Microprocessor Systems
- Computers
- Controllers
- Intelligent Instruments

GENERAL DESCRIPTION
The ADM690A/ADM692A/ADM802L/M/ADM805L/M family of supervisory circuits offers complete single chip solutions for power supply monitoring and battery control functions in microprocessor systems. These functions include µP reset, backup battery switchover, watchdog timer, and power failure warning.

The ADM690A/ADM692A/ADM802L/M/ADM805L/M are available in 8-pin packages and provide:
1. Power-on reset output during power-up, power-down and brownout conditions. The RESET output remains operational with VCC as low as 1 V.
2. Battery backup switching for CMOS RAM, CMOS microprocessor or other low power devices.
3. A reset pulse if the optional watchdog timer has not been toggled within 1.6 seconds.
4. A 1.25 V threshold detector for power fail warning, low battery detection, or to monitor a power supply other than +5 V.

On the ADM690A/ADM802L/ADM805L the reset voltage threshold is 4.65 V. On the ADM692A/ADM802M/ADM805M, the reset voltage threshold is 4.40 V.

The ADM802L/ADM802M guarantee power fail accuracies to ±2%.

The ADM805L/M provides an active high reset output, RESET instead of RESET.

The family of products is fabricated using an advanced epilaxial CMOS process combining low power consumption and high reliability. RESET assertion is guaranteed with VCC as low as 1 V.

They provide a pin-compatible upgrade for the MAX690A/MAX692A/MAX802L/MAX802M/MAX805L.

All parts are available in 8-pin DIP and SOIC packages. The ADM690A is also available in a new space-saving microSOIC package.
## ADM690A/ADM692A/ADM802L/M/ADM805L/M–SPECIFICATIONS

(VCC = 4.75 V to 5.5 V (ADM690A/ADM802L/ADM805L), VCC = 4.5 V to 5.5 V, (ADM692A/ADM802M/ADM805M), Vbatt = +2.8 V, TA = Tmin to Tmax unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>VCC/Vbatt operation</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCC Operating Voltage Range</td>
<td>1.0</td>
<td>5.5</td>
<td>V</td>
<td></td>
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<tr>
<td>Supply Current (Excludes IOUT)</td>
<td>70</td>
<td>100</td>
<td>µA</td>
<td></td>
<td></td>
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<tr>
<td>Supply Current in Battery Backup</td>
<td>0.05</td>
<td>1.0</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Battery Standby Current (+ = Discharge, – = Charge)</td>
<td></td>
<td></td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VOUT Output Voltage</td>
<td>VCC – 0.02</td>
<td>VCC – 0.01</td>
<td>V</td>
<td></td>
<td>IOUT = 5 mA</td>
</tr>
<tr>
<td></td>
<td>VCC – 0.5</td>
<td>VCC – 0.05</td>
<td>V</td>
<td></td>
<td>IOUT = 50 mA</td>
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<tr>
<td></td>
<td>VCC – 0.02</td>
<td></td>
<td>V</td>
<td>VOUT = 250 mA</td>
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<tr>
<td>VOUT in Battery Backup Mode</td>
<td>Vbatt – 0.05</td>
<td>Vbatt – 0.002</td>
<td>V</td>
<td>VOUT = 250 µA, VCC &lt; Vbatt – 0.2 V</td>
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<tr>
<td>Battery Switchover Threshold</td>
<td>20</td>
<td>20</td>
<td>mV</td>
<td>Power Up</td>
<td></td>
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<tr>
<td>Battery Switchover Hysteresis</td>
<td>40</td>
<td>40</td>
<td>mV</td>
<td>Power Down</td>
<td></td>
</tr>
<tr>
<td><strong>Reset Threshold</strong></td>
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<td></td>
<td></td>
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</tr>
<tr>
<td>Reset Voltage Threshold</td>
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<td></td>
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<tr>
<td>ADM690A, ADM802L, ADM805L</td>
<td>4.5</td>
<td>4.65</td>
<td>4.75</td>
<td>V</td>
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<td>ADM692A, ADM802M, ADM805M</td>
<td>4.25</td>
<td>4.4</td>
<td>4.5</td>
<td>V</td>
<td>T_A = 25°C, VCC Falling</td>
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<tr>
<td>ADM802L</td>
<td>4.55</td>
<td>4.7</td>
<td>V</td>
<td>T_A = 25°C, VCC Falling</td>
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<tr>
<td>ADM802M</td>
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<td>4.45</td>
<td>V</td>
<td>T_A = 25°C, VCC Falling</td>
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<tr>
<td>Reset Threshold Hysteresis</td>
<td>40</td>
<td>40</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reset Timeout Delay</td>
<td>140</td>
<td>200</td>
<td>280</td>
<td>ms</td>
<td></td>
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<tr>
<td><strong>Watchdog Timer</strong></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Watchdog Timeout Period</td>
<td>1.0</td>
<td>1.6</td>
<td>2.25</td>
<td>s</td>
<td>VIL = 0.4, VIH = 0.8 (VCC)</td>
</tr>
<tr>
<td>WDI Input Pulse Width</td>
<td>50</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>WDI Input Threshold</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logic Low</td>
<td>3.5</td>
<td>0.8</td>
<td>V</td>
<td></td>
<td>WDI = VCC</td>
</tr>
<tr>
<td>Logic High</td>
<td>3.5</td>
<td>0.8</td>
<td>V</td>
<td></td>
<td>WDI = 0 V</td>
</tr>
<tr>
<td>WDI Input Current</td>
<td>–10</td>
<td>10</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Power Fail Detector</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PFI Input Threshold</td>
<td>1.20</td>
<td>1.25</td>
<td>1.30</td>
<td>V</td>
<td>ADM690A, ADM692A, ADM805L/M</td>
</tr>
<tr>
<td></td>
<td>1.225</td>
<td>1.25</td>
<td>1.275</td>
<td>V</td>
<td>ADM802L/M</td>
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<tr>
<td>PFI Input Current</td>
<td>–25</td>
<td>0.01</td>
<td>+25</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>PFO Output Voltage</td>
<td>VCC – 1.5</td>
<td>0.4</td>
<td>V</td>
<td>IOUT = 800 µA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>IOUT = 3.2 mA</td>
<td></td>
</tr>
</tbody>
</table>

**Notes**

1Either VCC or Vbatt can be 0 V if the other > 2.0 V.

Specifications subject to change without notice.
ABSOLUTE MAXIMUM RATINGS*  
(Ta = +25°C unless otherwise noted)

### VCC
- Power Supply Input: +5 V Nominal.
- Backup Battery Input. As VCC falls below the reset threshold and below VBATT by 20 mV, VBATT will be switched to VOUT. On power-up as VCC rises to 20 mV above VBATT, VOUT will be switched back to VCC.

### VBATT
- Output Voltage. When VCC is above the reset threshold, the higher of VCC or VBATT is connected to VOUT.

### GND
- 0 V. Ground reference for all signals.

### PFI
- Power Fail Comparator Input. If PFI is less than 1.25 V, the power fail output PFO goes low. If unused, PFI should be connected to VCC or GND.

### PFO
- Power Fail Comparator Output. If PFI is less than 1.25 V, the power fail output PFO goes low.

### RESET
- Logic Output. RESET goes low if
  1. VCC falls below the Reset Threshold
  2. The watchdog timer is not serviced within its timeout period (1.6 seconds)
- The reset threshold is typically 4.65 V for the ADM690A/ADM802L/ADM805L and 4.4 V for the ADM692A/ADM802M/ADM805M. RESET remains low for 200 ms after VCC returns above the threshold. RESET also goes low for 200 ms if the watchdog timer is enabled but not serviced within its timeout period.

### WDI
- Watchdog Input. WDI is a three level input. If WDI remains either high or low for longer than 1.6 s, (RESET) (RESET) is activated. The timer resets with each transition on the WDI line. The watchdog timer may be disabled if WDI is left floating or is connected to a high impedance three state logic output.

**Ordering Guide**

<table>
<thead>
<tr>
<th>Model</th>
<th>Temperature Range</th>
<th>Package Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADM690AAN</td>
<td>40°C to +85°C</td>
<td>N-8</td>
</tr>
<tr>
<td>ADM690AARN</td>
<td>40°C to +85°C</td>
<td>SO-8</td>
</tr>
<tr>
<td>ADM690AARM</td>
<td>40°C to +85°C</td>
<td>RM-8</td>
</tr>
<tr>
<td>ADM692AAN</td>
<td>40°C to +85°C</td>
<td>N-8</td>
</tr>
<tr>
<td>ADM692AARN</td>
<td>40°C to +85°C</td>
<td>SO-8</td>
</tr>
<tr>
<td>ADM802LAN</td>
<td>40°C to +85°C</td>
<td>N-8</td>
</tr>
<tr>
<td>ADM802LARN</td>
<td>40°C to +85°C</td>
<td>SO-8</td>
</tr>
<tr>
<td>ADM802MAN</td>
<td>40°C to +85°C</td>
<td>N-8</td>
</tr>
<tr>
<td>ADM802MARN</td>
<td>40°C to +85°C</td>
<td>SO-8</td>
</tr>
<tr>
<td>ADM805LAN</td>
<td>40°C to +85°C</td>
<td>N-8</td>
</tr>
<tr>
<td>ADM805LARN</td>
<td>40°C to +85°C</td>
<td>SO-8</td>
</tr>
<tr>
<td>ADM805MAN</td>
<td>40°C to +85°C</td>
<td>N-8</td>
</tr>
<tr>
<td>ADM805MARN</td>
<td>40°C to +85°C</td>
<td>SO-8</td>
</tr>
</tbody>
</table>

*Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.
Typical Performance Curves

Figure 1. Output Voltage vs. Load Current in Battery Backup

Figure 2. Power Fail Comparator Response Time L $\rightarrow$ H

Figure 3. ADM690A RESET Response Time

Figure 4. Output Voltage vs. Load Current in Normal Operation

Figure 5. Power Fail Comparator Response Time H $\rightarrow$ L

Figure 6. RESET Output Voltage vs. $V_{CC}$
POWER FAIL RESET, RESET

RESET is an active low output which provides a RESET signal to the microprocessor whenever V CC is at an invalid level. When V CC falls below the reset threshold, the RESET output is forced low. The nominal reset voltage threshold is 4.65 V (ADM690A/ADM802L/ADM805L or 4.4 V ADM692A/ADM802M/ADM805M).

On power-up RESET will remain low for 200 ms after V CC rises above the reset threshold. This allows time for the power supply and microprocessor to stabilize. On power-down, the RESET output remains low with V CC as low as 1 V. This ensures that the microprocessor is held in a stable shutdown condition.

The guaranteed minimum and maximum thresholds are as follows:
- ADM690A/ADM802L/ADM805L: 4.5 V and 4.75 V
- ADM692A: 4.25 V and 4.5 V
- ADM802L: 4.55 V and 4.7 V
- ADM802M: 4.3 V and 4.45 V

The ADM805L and ADM805M contain an active high reset output. This is the complement of RESET and is intended for processors requiring an active high RESET signal.

The guaranteed minimum and maximum thresholds for the ADM805 are:
- ADM805L: 4.5 V and 4.75 V
- ADM805M: 4.25 V and 4.5 V

Watchdog Timer RESET, RESET

The watchdog timer circuit monitors the activity of the microprocessor in order to check that it is not stalled in an indefinite loop. An output line on the processor is used to toggle the Watchdog Input (WDI) line. If this line is not toggled within 1.6 seconds, a RESET pulse is generated. The watchdog timeout period restarts with each transition on the WDI pin. To ensure that the watchdog timer does not time out, either a high-to-low or low-to-high transition on the WDI pin must occur at or less than the minimum timeout period. If WDI remains permanently either high or low, reset pulses will be issued after each timeout period (1.6 s). The watchdog monitor can be deactivated by floating the Watchdog Input (WDI) or by connecting it to midsupply.

BATTERY SWITCHOVER SECTION

During normal operation with V CC higher than the reset threshold, V CC is internally switched to V OUT via an internal PMOS transistor switch. This switch has a typical on-resistance of less than 1 Ω and can supply up to 100 mA at the V OUT terminal. Once V CC falls below the reset threshold, the higher of V CC or V BATT is switched to V OUT. This means that V BATT connects to V OUT only when V CC is below the reset threshold and V BATT is greater than V CC.

V OUT is normally used to drive a RAM memory bank which may require instantaneous currents of greater than 100 mA. If this is the case, then a bypass capacitor should be connected to V OUT. The capacitor will provide the peak current transients to the RAM. A capacitance value of 0.1 μF or greater may be used.

A 9 Ω MOSFET switch connects the V BATT input to V OUT during battery backup. This MOSFET has very low input-to-output differential (dropout voltage) at the low current levels required for battery backup of CMOS RAM or other low power CMOS circuitry. The supply current in battery backup is typically 0.05 μA.

Typically 3 V batteries are used as the backup supply. High value capacitors, either standard electrolytic or the farad size double layer capacitors, can also be used for short-term memory back up. A small charging current of typically 10 nA (0.1 μA max) flows out of the V BATT terminal. This current is useful for maintaining rechargeable batteries in a fully charged condition. This extends the life of the back up battery by compensating for its self discharge current. Also note that this current poses no problem when lithium batteries are used for back up since the maximum charging current (0.1 μA) is safe for even the smallest lithium cells.

If the battery-switchover section is not used, V BATT should be connected to GND and V OUT should be connected to V CC.
### Table I. Input and Output Status in Battery Backup Mode

<table>
<thead>
<tr>
<th>Signal</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>V$_{OUT}$</td>
<td>V$<em>{OUT}$ is connected to V$</em>{BATT}$ via an internal PMOS switch.</td>
</tr>
<tr>
<td>RESET</td>
<td>Logic low.</td>
</tr>
<tr>
<td>RESET (ADM805L, ADM805M)</td>
<td>Logic high. The open circuit output voltage is equal to V$_{OUT}$.</td>
</tr>
<tr>
<td>PFI</td>
<td>The power fail comparator is disabled</td>
</tr>
<tr>
<td>PFO</td>
<td>Logic low.</td>
</tr>
<tr>
<td>WDI</td>
<td>The watchdog timer is disabled</td>
</tr>
</tbody>
</table>

#### Power Fail Comparator

The power fail comparator is an independent comparator that may be used to monitor the input power supply. The comparator’s inverting input is internally connected to a 1.25 V reference voltage. The noninverting input is available at the PFI input. This input may be used to monitor the input power supply via a resistive divider network. When the voltage on the PFI input drops below 1.25 V, the comparator output (PFO) goes low indicating a power failure. For early warning of power failure the comparator may be used to monitor the preregulator input simply by choosing an appropriate resistive divider network. The PFO output can be used to interrupt the processor so that a shutdown procedure is implemented before the power is lost.

#### Adding Hysteresis to the Power Fail Comparator

For increased noise immunity, hysteresis may be added to the power fail comparator. Since the comparator circuit is non-inverting, hysteresis can be added simply by connecting a resistor between the PFO output and the PFI input as shown in Figure 10. When PFO is low, resistor R3 sinks current from the summing junction at the PFI pin. When PFO is high, resistor R3 sources current into the PFI summing junction. This results in differing trip levels for the comparator. Further noise immunity may be achieved by connecting a capacitor between PFI and GND.

#### Figure 9. Power Fail Comparator

#### TYPICAL APPLICATIONS

Figure 11 shows a typical power monitoring, battery backup application. V$_{OUT}$ powers the CMOS RAM. Under normal operating conditions with V$_{CC}$ present, V$_{OUT}$ is internally connected to V$_{CC}$. If a power failure occurs, V$_{CC}$ will decay and V$_{OUT}$ will be switched to V$_{BATT}$ thereby maintaining power for the CMOS RAM. A RESET pulse is also generated when V$_{CC}$ falls below the reset threshold.

#### Figure 10. Adding Hysteresis to the Power Fail Comparator

#### Figure 11. Typical Application Circuit

The watchdog timer input (WDI) monitors an I/O line from the µP system. This line must be toggled once every 1.6 seconds to verify correct software execution. Failure to toggle the line indicates that the µP system is not correctly executing its program and may be tied up in an endless loop. If this happens, a reset pulse is generated to initialize the processor.
If the watchdog timer is not needed, the WDI input should be left floating.

The Power Fail Input, PFI, monitors the input power supply via a resistive divider network. The voltage on the PFI input is compared with a precision 1.25 V internal reference. If the input voltage drops below 1.25 V, a power fail output (PFO) signal is generated. This warns of an impending power failure and may be used to interrupt the processor so that the system may be shut down in an orderly fashion. The resistors in the sensing network are ratioed to give the desired power fail threshold voltage $V_T$.

$$V_T = (1.25 \frac{R1}{R2}) + 1.25 \text{ V}$$

$$R1/R2 = \left(\frac{V_T}{1.25}\right) - 1$$

**Alternate Watchdog Input Drive Circuits**

The watchdog feature can be enabled and disabled under program control by driving WDI with a 3-state buffer. When three-stated, the WDI input will float thereby disabling the watchdog timer.

**High Capacity Backup Capacitors**

High capacity (0.1 µF or greater) capacitors may be used as a backup power source. A typical application is shown in Figure 12.

**Operation Without a Backup Supply**

If a backup power source is not used, $V_{BATT}$ should be connected to GND and $V_{OUT}$ should be connected to $V_{CC}$.

**Replacing the Backup Battery**

The backup battery may be replaced without any danger of spurious resetting when $V_{CC}$ is present. Since $V_{CC}$ is above the reset threshold, a reset will not occur even if $V_{BATT}$ is floating while a replacement battery is being inserted. This differs from older generation products where leakage currents flowing out $V_{BATT}$ could cause spurious resetting during battery replacement.

**µPs With Bidirectional RESET**

In order to prevent contention for microprocessors with a bidirectional reset line, a current limiting resistor should be inserted between the ADM69xA/ADM80xx RESET output pin and the µP reset pin. This will limit the current to a safe level if there are conflicting output reset levels. A suitable resistor value is 4.7 kΩ. If the reset output is required for other uses, then it should be buffered as shown in Figure 13.
OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).

8-Pin Plastic DIP
(N-8)

8-Lead SOIC
(SO-8)

8-Lead MicroSOIC
(RM-8)