

FEATURES

- Triaxial, digital gyroscope, $\pm 2000^\circ/\text{sec}$ dynamic range**
- 8°/hr in run bias stability**
- 0.008°/sec/ $\sqrt{\text{Hz}}$ rms rate noise density**
- Triaxial, digital accelerometer dynamic range: $\pm 40 g$**
- 13 μg in run bias stability**
- Triaxial, delta angle and delta velocity outputs**
- Factory calibrated sensitivity, bias, and axial alignment**
- Calibration temperature range: -10°C to $+75^\circ\text{C}$**
- SPI compatible data communications**
- Programmable operation and control**
- Automatic and manual bias correction controls**
- Data ready indicator for synchronous data acquisition**
- External sync modes: direct, pulse, scaled, and output**
- On demand self test of inertial sensors**
- On demand self test of flash memory**
- Single-supply operation (VDD): 3.0 V to 3.6 V**
- 2000 g mechanical shock survivability**
- Operating temperature range: -25°C to $+85^\circ\text{C}$**

APPLICATIONS

- Navigation, stabilization, and instrumentation**
- Unmanned and autonomous vehicles**
- Smart agriculture/construction machinery**
- Factory/industrial automation, robotics**
- Virtual/augmented reality**
- Internet of Moving Things**

GENERAL DESCRIPTION

The ADIS16470 is a miniature MEMS inertial measurement unit (IMU) that includes a triaxial gyroscope and a triaxial accelerometer. Each inertial sensor in the ADIS16470 combines with signal conditioning that optimizes dynamic performance. The factory calibration characterizes each sensor for sensitivity, bias, alignment, linear acceleration (gyroscope bias), and point of percussion (accelerometer location). As a result, each sensor has dynamic compensation formulas that provide accurate sensor measurements over a broad set of conditions.

The ADIS16470 provides a simple, cost effective method for integrating accurate, multi-axis inertial sensing into industrial systems, especially when compared with the complexity and investment associated with discrete designs. All necessary motion testing and calibration are part of the production process at the factory, greatly reducing system integration time. Tight orthogonal alignment simplifies inertial frame alignment in navigation systems. The serial peripheral interface (SPI) and register structure provide a simple interface for data collection and configuration control.

The ADIS16470 is in a 44-ball, ball grid array (BGA) package that is approximately 11 mm \times 15 mm \times 11 mm.

FUNCTIONAL BLOCK DIAGRAM

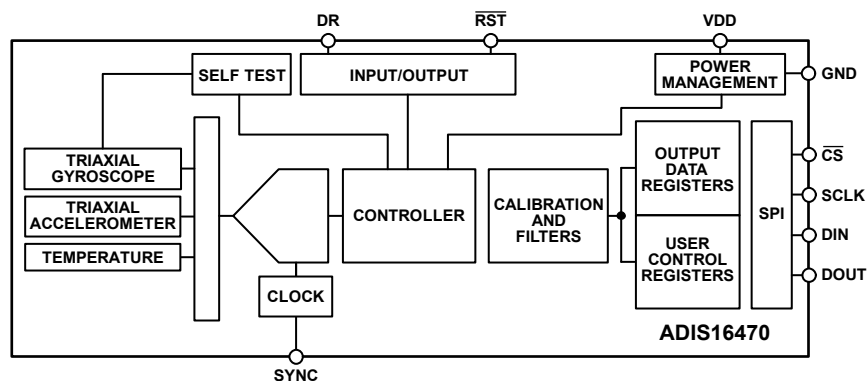


Figure 1.

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REVISION HISTORY

11/2017—Rev. 0 to Rev. A

| | |
|--------------------------|---|
| Changes to Table 1 | 3 |
|--------------------------|---|

10/2017—Rev. 0: Initial Version

SPECIFICATIONS

$T_C = 25^\circ\text{C}$, $V_{DD} = 3.3\text{ V}$, angular rate = $0^\circ/\text{sec}$, dynamic range = $\pm 2000^\circ/\text{sec} \pm 1\text{ g}$, unless otherwise noted.

Table 1.

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|--|---|------------|------------|-----|--|
| GYROSCOPES | | | | | |
| Dynamic Range | | ± 2000 | | | $^\circ/\text{sec}$ |
| Sensitivity | 16-bit format | | 10 | | LSB/ $^\circ/\text{sec}$ |
| | 32-bit format | | 655,360 | | LSB/ $^\circ/\text{sec}$ |
| Error over Temperature | $-10^\circ\text{C} \leq T_C \leq +75^\circ\text{C}$ | | ± 0.25 | | % |
| Misalignment | Axis to axis | | ± 0.1 | | Degrees |
| Nonlinearity ¹ | Full scale (FS) = $2000^\circ/\text{sec}$ | | ± 0.25 | | %FS |
| Bias | | | | | |
| In Run Stability | 1σ | | 8 | | $^\circ/\text{hr}$ |
| Angular Random Walk | 1σ | | 0.34 | | $^\circ/\sqrt{\text{hr}}$ |
| Error over Temperature | $-10^\circ\text{C} \leq T_C \leq +75^\circ\text{C}$, 1σ | | 0.2 | | $^\circ/\text{sec}$ |
| Linear Acceleration Effect | Any direction, 1σ | | 0.015 | | $^\circ/\text{sec}/\text{g}$ |
| Vibration Rectification Error | | | 0.0005 | | $^\circ/\text{sec}/\text{g}^2$ |
| Output Noise | 1σ , no filtering | | 0.17 | | $^\circ/\text{sec rms}$ |
| Rate Noise Density | 1σ , $f = 10\text{ Hz to }40\text{ Hz}$ | | 0.008 | | $^\circ/\text{sec}/\sqrt{\text{Hz rms}}$ |
| 3 dB Bandwidth | | | 550 | | Hz |
| Sensor Resonant Frequency | | | 66 | | kHz |
| ACCELEROMETERS² | | | | | |
| | Each axis | ± 40 | | | g |
| Dynamic Range | | | | | g |
| Sensitivity | 16-bit format | | 800 | | LSB/ g |
| | 32-bit format | | 52,428,800 | | LSB/ g |
| Error over temperature | $-10^\circ\text{C} \leq T_C \leq +75^\circ\text{C}$ | | ± 0.1 | | % |
| Misalignment | Axis to axis | | ± 0.1 | | Degrees |
| Nonlinearity | Best fit straight line, FS = $\pm 10\text{ g}$ | | 0.02 | | % FS |
| | Best fit straight line, FS = $\pm 20\text{ g}$ | | 0.4 | | % FS |
| | Best fit straight line, FS = $\pm 40\text{ g}$ | | 1.5 | | % FS |
| Bias | | | | | |
| In Run Stability | 1σ | | 13 | | μg |
| Velocity Random Walk | 1σ | | 0.037 | | $\text{m}/\text{sec}/\sqrt{\text{Hr}}$ |
| Error over Temperature | $-10^\circ\text{C} \leq T_C \leq +75^\circ\text{C}$, 1σ | | ± 4 | | mg |
| Output Noise | No filtering | | 2.3 | | mg rms |
| Noise Density | $f = 10\text{ Hz to }40\text{ Hz}$, no filtering | | 100 | | $\mu\text{g}/\sqrt{\text{Hz rms}}$ |
| 3 dB Bandwidth | | | 600 | | Hz |
| Sensor Resonant Frequency | Y-axis, z-axis | | 5.65 | | kHz |
| | X-axis | | 5.25 | | kHz |
| TEMPERATURE SENSOR | | | | | |
| Scale Factor | | | 0.1 | | $^\circ\text{C}/\text{LSB}$ |
| LOGIC INPUTS³ | | | | | |
| Input Voltage | | | | | |
| High, V_{IH} | | 2.0 | | | V |
| Low, V_{IL} | | | | 0.8 | V |
| $\overline{\text{RST}}$ Pulse Width | | 1 | | | μs |
| $\overline{\text{CS}}$ Wake-Up Pulse Width | | 20 | | | μs |
| Input Current | | | | | |
| Logic 1, I_{IH} | $V_{IH} = 3.3\text{ V}$ | | | 10 | μA |
| Logic 0, I_{IL} | $V_{IL} = 0\text{ V}$ | | | | |
| All Pins Except $\overline{\text{RST}}$ | | | | 10 | μA |
| $\overline{\text{RST}}$ Pin | | | 0.33 | | mA |
| Input Capacitance, C_{IN} | | | 10 | | pF |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|--|-------------|------|-----|-----------------|
| DIGITAL OUTPUTS | | | | | |
| Output Voltage | | | | | |
| High, V_{OH} | $I_{SOURCE} = 0.5 \text{ mA}$ | 2.4 | | | V |
| Low, V_{OL} | $I_{SINK} = 2.0 \text{ mA}$ | | | 0.4 | V |
| FLASH MEMORY | | | | | |
| Data Retention ⁵ | Endurance ⁴ $T_J = 85^\circ\text{C}$ | 10000 20 | | | Cycles Years |
| FUNCTIONAL TIMES ⁶ | Time until data is available | | | | |
| Power-On Start-Up Time | $V_{DD} > 3.0 \text{ V}$ to DR pulsing (see Figure 23) | | 252 | | ms |
| Hardware Reset Recovery Time ⁷ | $RST > V_{OH}$ to DR pulsing (see Figure 25) | | 193 | | ms |
| Software Reset Recovery Time | Register GLOB_CMD, Bit 7 = 1 (see Table 109) | | 193 | | ms |
| Flash Memory Update Time | Register GLOB_CMD, Bit 3 = 1 (see Table 109) | | 72 | | ms |
| Flash Memory Test Time | Register GLOB_CMD, Bit 4 = 1 (see Table 109) | | 32 | | ms |
| Factory Calibration Restore Time | Register GLOB_CMD, Bit 1 = 1 (see Table 109) | | 142 | | ms |
| Sensor Self Test Time ⁸ | Register GLOB_CMD, Bit 2 = 1 (see Table 109) | | 14 | | ms |
| CONVERSION RATE | | | 2000 | | SPS |
| Initial Clock Accuracy | | | 3 | | % |
| Sync Input Clock | | 1.9 | | 2.1 | kHz |
| POWER SUPPLY, VDD | | | | | |
| Power Supply Current ⁹ | Operating voltage range Normal mode, $V_{DD} = 3.3 \text{ V}$ | 3.0 | | 3.6 | V |
| | | | 42 | 50 | mA |

¹ Linearity is based on the deviation from a best fit linear model.

² All specifications associated with the accelerometers relate to the full-scale range of $\pm 40 \text{ g}$, unless otherwise noted.

³ The digital input/output signals use a 3.3 V system.

⁴ Endurance is qualified as per JEDEC Standard 22, Method A117, measured at -40°C , $+25^\circ\text{C}$, $+85^\circ\text{C}$, and $+125^\circ\text{C}$.

⁵ The data retention specification assumes a junction temperature (T_J) of 85°C per JEDEC Standard 22, Method A117. Data retention lifetime decreases with T_J .

⁶ These times do not include thermal settling and internal filter response times, which may affect overall accuracy.

⁷ The RST line must be in a low state for at least $10 \mu\text{s}$ to ensure a proper reset initiation and recovery.

⁸ Sensor self test time can extend when using external clock rates that are lower than 2000 Hz.

⁹ Supply current transients can reach 250 mA during initial startup or reset recovery.

TIMING SPECIFICATIONS

T_A = 25°C, VDD = 3.3 V, unless otherwise noted.

Table 2.

| Parameter | Description | Normal Mode | | | Burst Read | | | Unit |
|---|--|------------------|-----|------|--------------------|-----|------|------|
| | | Min ¹ | Typ | Max | Min ^{1,2} | Typ | Max | |
| f _{SCLK} | Serial clock | 0.1 | | 2.0 | 0.1 | | 1.0 | MHz |
| t _{STALL} | Stall period ³ between data | 16 | | | N/A | | | μs |
| t _{READRATE} | Read rate | 24 | | | | | | μs |
| t _{CS} | Chip select to SCLK edge | 200 | | | 200 | | | ns |
| t _{DAV} | DOUT valid after SCLK edge | | | 25 | | | 25 | ns |
| t _{DSU} | DIN setup time before SCLK rising edge | 25 | | | 25 | | | ns |
| t _{DHD} | DIN hold time after SCLK rising edge | 50 | | | 50 | | | ns |
| t _{SCLKR} , t _{SCLKF} | SCLK rise/fall times | | 5 | 12.5 | | 5 | 12.5 | ns |
| t _{DR} , t _{DF} | DOUT rise/fall times | | 5 | 12.5 | | 5 | 12.5 | ns |
| t _{SFS} | CS high after SCLK edge | 0 | | | 0 | | | ns |
| t ₁ | Input sync positive pulse width | | | | | | | |
| | Pulse sync mode, MSC_CTRL = 101 (binary, see Table 101) | 5 | | | 5 | | | μs |
| t _{STDR} | Input sync to data ready valid transition | | | | | | | |
| | Direct sync mode, MSC_CTRL = 001 (binary, see Table 101) | | 507 | | | 507 | | μs |
| | Pulse sync mode, MSC_CTRL = 101 (binary, see Table 101) | | 256 | | | 256 | | μs |
| t _{NV} | Data invalid time | | 20 | | | 20 | | μs |
| t ₂ | Input sync period | 500 | | | 500 | | | μs |

¹ Guaranteed by design and characterization, but not tested in production.

² N/A means not applicable.

³ When using the burst read mode, the stall period is not applicable.

Timing Diagrams

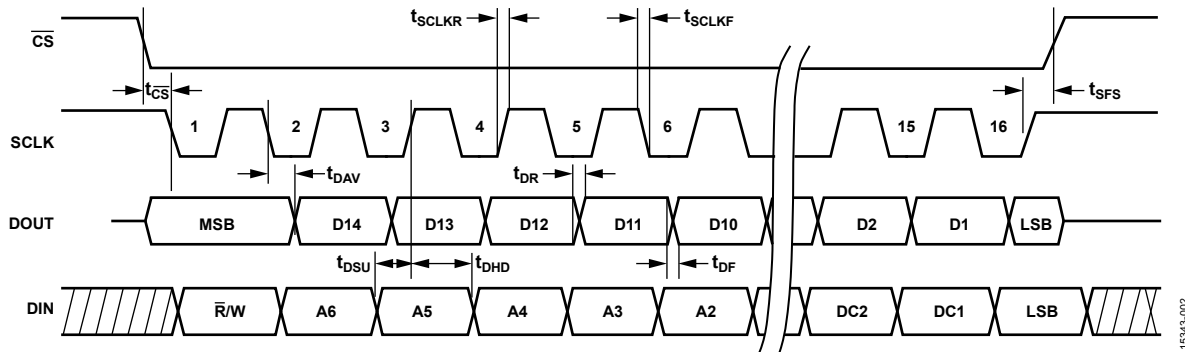


Figure 2. SPI Timing and Sequence

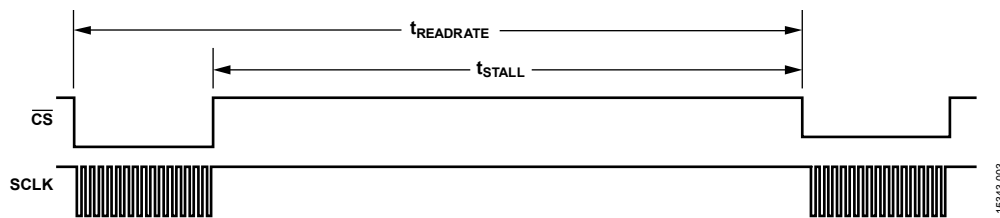


Figure 3. Stall Time and Data Rate

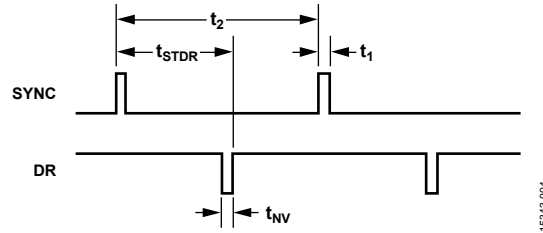


Figure 4. Input Clock Timing Diagram, Pulse Sync Mode, Register MSC_CTRL, Bits[4:2] = 101 (Binary)

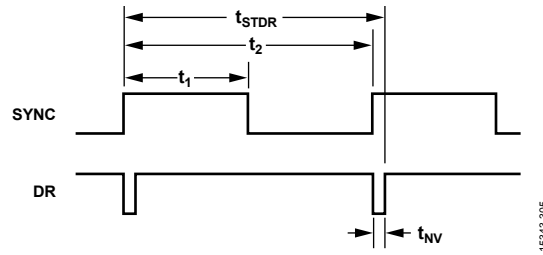


Figure 5. Input Clock Timing Diagram, Direct Sync Mode, Register MSC_CTRL, Bits[4:2] = 001 (Binary)

ABSOLUTE MAXIMUM RATINGS

Table 3.

| Parameter | Rating |
|--|-----------------------|
| Mechanical Shock Survivability | |
| Any Axis, Unpowered | 2000 g |
| Any Axis, Powered | 2000 g |
| VDD to GND | −0.3 V to +3.6 V |
| Digital Input Voltage to GND | −0.3 V to VDD + 0.2 V |
| Digital Output Voltage to GND | −0.3 V to VDD + 0.2 V |
| Operating Temperature Range | −25°C to +85°C |
| Storage Temperature Range ¹ | −65°C to +150°C |
| Barometric Pressure | 2 bar |

¹ Extended exposure to temperatures that are lower than −20°C or higher than +85°C can adversely affect the accuracy of the factory calibration.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

The ADIS16470 is a multichip module that includes many active components. The values in Table 4 identify the thermal response of the hottest component inside of the ADIS16470, with respect to the overall power dissipation of the module. This approach enables a simple method for predicting the temperature of the hottest junction, based on either ambient or case temperature.

For example, when the ambient temperature is 70°C, the hottest junction temperature (T_J) inside of the ADIS16470 is 93°C.

$$T_J = \theta_{JA} \times VDD \times I_{DD} + 70^\circ\text{C}$$

$$T_J = 158.2^\circ\text{C/W} \times 3.3 \text{ V} \times 0.044 \text{ A} + 70^\circ\text{C}$$

$$T_J = 93^\circ\text{C}$$

Table 4. Package Characteristics

| Package Type | θ_{JA} ¹ | θ_{JC} ² | Device Weight |
|----------------------|----------------------------|----------------------------|---------------|
| ML-44-1 ³ | 158.2°C/W | 106.1°C/W | 1.3 grams |

¹ θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

² θ_{JC} is the junction to case thermal resistance.

³ Thermal impedance values come from direct observation of the hottest temperature inside of the ADIS16470, when it is attached to a FR4-08 PCB that has two metal layers and has a thickness of 0.063".

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

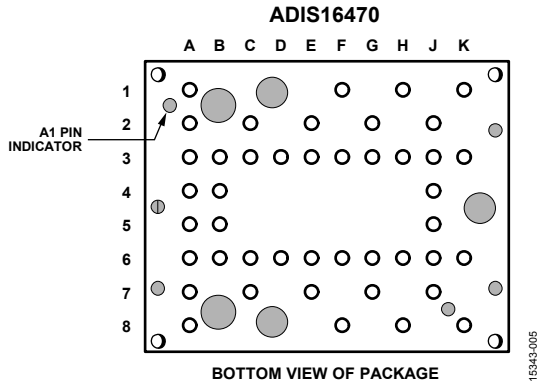


Figure 6. Pin Assignments, Bottom View

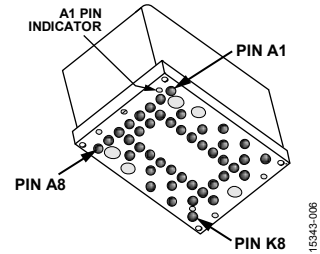


Figure 7. Pin Assignments, Package Level View

Table 5. Pin Function Descriptions

| Pin No. | Mnemonic | Type | Description |
|---------|----------|----------------|-------------------|
| A1 | GND | Supply | Power Ground |
| A2 | GND | Supply | Power Ground |
| A3 | GND | Supply | Power Ground |
| A4 | GND | Supply | Power Ground |
| A5 | GND | Supply | Power Ground |
| A6 | GND | Supply | Power Ground |
| A7 | GND | Supply | Power Ground |
| A8 | GND | Supply | Power Ground |
| B3 | GND | Supply | Power Ground |
| B4 | GND | Supply | Power Ground |
| B5 | GND | Supply | Power Ground |
| B6 | GND | Supply | Power Ground |
| C2 | GND | Supply | Power Ground |
| C3 | DNC | Not applicable | Do Not Connect |
| C6 | GND | Supply | Power Ground |
| C7 | VDD | Supply | Power Supply |
| D3 | GND | Supply | Power Ground |
| D6 | VDD | Supply | Power Supply |
| E2 | GND | Supply | Power Ground |
| E3 | VDD | Supply | Power Supply |
| E6 | GND | Supply | Power Ground |
| E7 | GND | Supply | Power Ground |
| F1 | GND | Supply | Power Ground |
| F3 | RST | Input | Reset |
| F6 | GND | Supply | Power Ground |
| F8 | GND | Supply | Power Ground |
| G2 | GND | Supply | Power Ground |
| G3 | CS | Input | SPI, Chip Select |
| G6 | DIN | Input | SPI, Data Input |
| G7 | GND | Supply | Power Supply |
| H1 | VDD | Supply | Power Supply |
| H3 | DOUT | Output | SPI, Data Output |
| H6 | SCLK | Input | SPI, Serial Clock |
| H8 | GND | Supply | Power Ground |

| Pin No. | Mnemonic | Type | Description |
|---------|----------|--------|-----------------------|
| J2 | GND | Supply | Power Ground |
| J3 | SYNC | Input | Sync (External Clock) |
| J4 | VDD | Supply | Power Supply |
| J5 | VDD | Supply | Power Supply |
| J6 | DR | Output | Data Ready |
| J7 | GND | Supply | Power Ground |
| K1 | GND | Supply | Power Ground |
| K3 | GND | Supply | Power Ground |
| K6 | VDD | Supply | Power Supply |
| K8 | GND | Supply | Power Ground |

TYPICAL PERFORMANCE CHARACTERISTICS

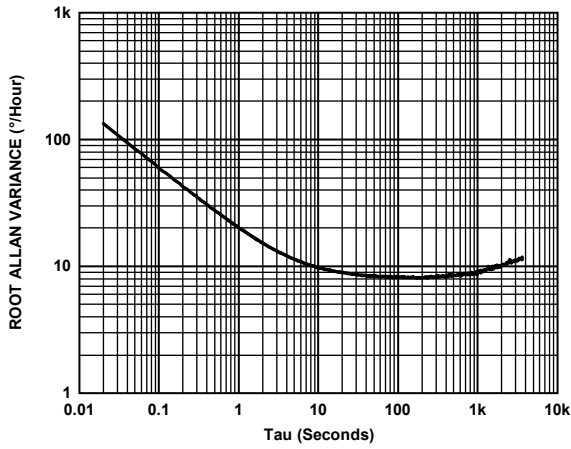


Figure 8. Gyroscope Root Allan Variance, $T_C = 25^\circ\text{C}$

15343-007

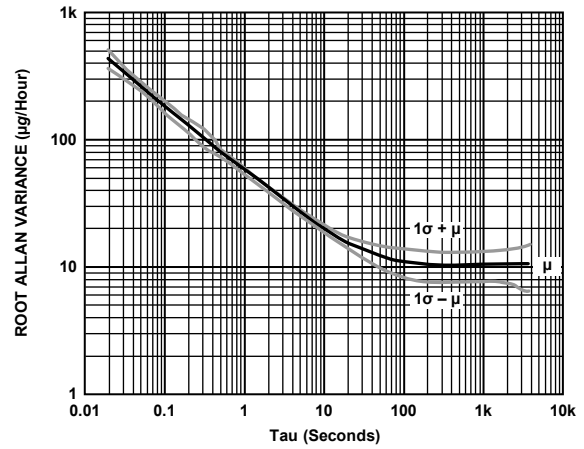


Figure 11. Accelerometer Root Allan Variance, $T_C = 25^\circ\text{C}$

15343-311

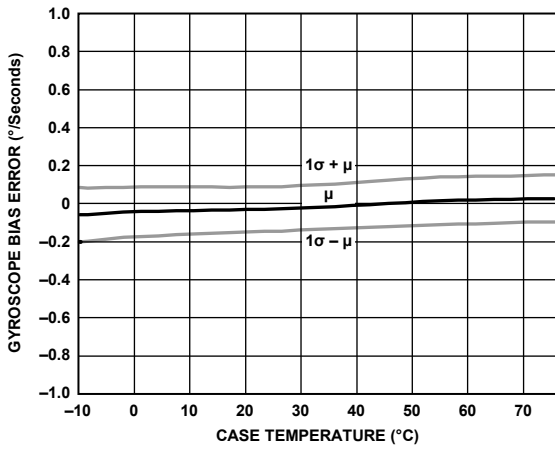


Figure 9. Gyroscope Bias Error vs. Case Temperature

15343-008

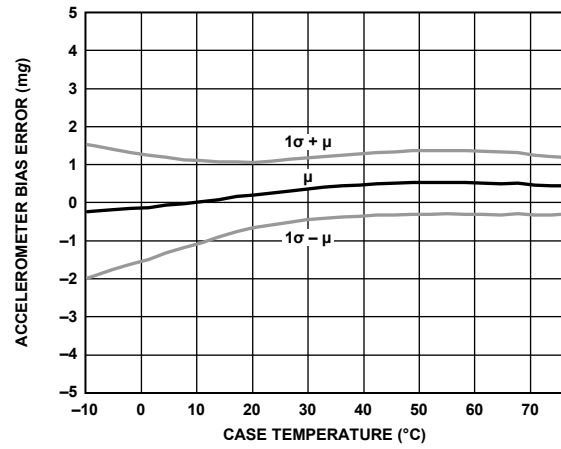


Figure 12. Accelerometer Bias Error vs. Case Temperature

15343-011

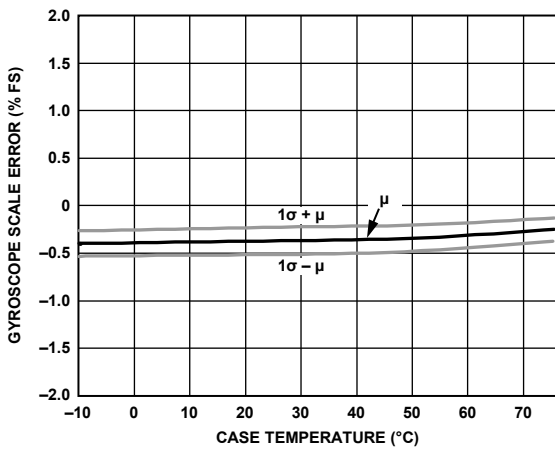


Figure 10. Gyroscope Scale (Sensitivity) Error vs. Case Temperature

15343-009

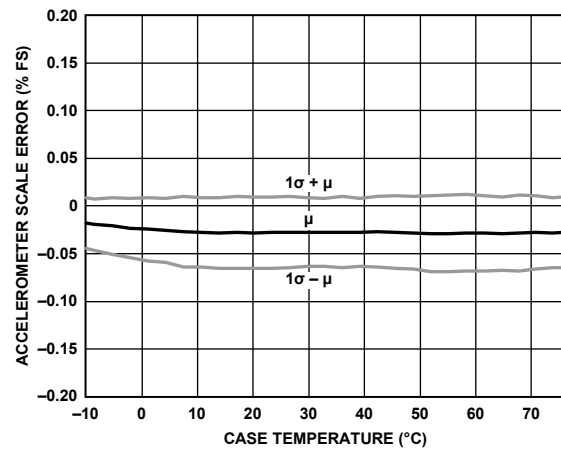


Figure 13. Accelerometer Scale (Sensitivity) Error vs. Case Temperature

15343-012

THEORY OF OPERATION

INTRODUCTION

When using the factory default configuration for all user configurable control registers, the ADIS16470 initializes itself and automatically starts a continuous process of sampling, processing, and loading calibrated sensor data into its output registers at a rate of 2000 SPS.

INERTIAL SENSOR SIGNAL CHAIN

Figure 14 provides the basic signal chain for the inertial sensors in the ADIS16470. This signal chain produces an update rate of 2000 SPS in the output data registers when it operates in internal clock mode (default, see Register MSC_CTRL, Bits [4:2] in Table 101).



Figure 14. Signal Processing Diagram, Inertial Sensors

Gyroscope Data Sampling

The three gyroscopes produce angular rate measurements around three orthogonal axes (x, y, and z). Figure 15 shows the sampling plan for each gyroscope when the ADIS16470 operates in the internal clock mode (default, see Register MSC_CTRL, Bits [4:2] in Table 101). Each gyroscope has an analog-to-digital converter (ADC) and sample clock (f_{SG}) that drives data sampling at a rate of 4100 Hz ($\pm 5\%$). The internal processor reads and processes this data from each gyroscope at a rate of 2000 Hz (f_{SM}).

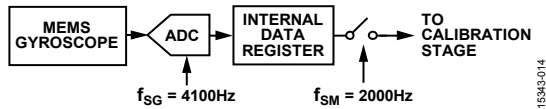


Figure 15. Gyroscope Data Sampling

Accelerometer Data Sampling

The three accelerometers produce linear acceleration measurements along the same orthogonal axes (x, y, and z) as the gyroscopes. Figure 16 provides the sampling plan for each accelerometer when the ADIS16470 operates in the internal clock mode (default, see Register MSC_CTRL, Bits [4:2] in Table 101).

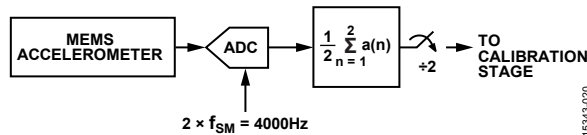


Figure 16. Accelerometer Data Sampling

External Clock Options

The ADIS16470 provides three different modes of operation that support the device using an external clock to control the internal processing rate (f_{SM} in Figure 15 and Figure 16) through the SYNC pin. The MSC_CTRL register (see Table 101) provides the configuration options for these external clock modes in Bits [4:2].

Inertial Sensor Calibration

The inertial sensor calibration function for the gyroscopes and the accelerometers has two components: factory calibration and user calibration (see Figure 17).



Figure 17. Inertial Sensor Calibration Processing

The factory calibration of the gyroscope applies the following correction formulas to the data of each gyroscope:

$$\begin{bmatrix} \omega_{XC} \\ \omega_{YC} \\ \omega_{ZC} \end{bmatrix} = \begin{bmatrix} m_{11} & m_{12} & m_{13} \\ m_{21} & m_{22} & m_{23} \\ m_{31} & m_{32} & m_{33} \end{bmatrix} \times \begin{bmatrix} \omega_X \\ \omega_Y \\ \omega_Z \end{bmatrix} + \begin{bmatrix} b_X \\ b_Y \\ b_Z \end{bmatrix}$$

$$\begin{bmatrix} l_{11} & l_{12} & l_{13} \\ l_{21} & l_{22} & l_{23} \\ l_{31} & l_{32} & l_{33} \end{bmatrix} \times \begin{bmatrix} a_{XC} \\ a_{YC} \\ a_{ZC} \end{bmatrix}$$

where:

ω_{XC} , ω_{YC} , and ω_{ZC} are the gyroscope outputs (post calibration). m_{11} , m_{12} , m_{13} , m_{21} , m_{22} , m_{23} , m_{31} , m_{32} , and m_{33} provide scale and alignment correction.

ω_X , ω_Y , and ω_Z are the gyroscope outputs (precalibration). b_X , b_Y , and b_Z provide bias correction.

l_{11} , l_{12} , l_{13} , l_{21} , l_{22} , l_{23} , l_{31} , l_{32} , and l_{33} provide linear g correction. a_{XC} , a_{YC} , and a_{ZC} are the accelerometer outputs (post calibration).

All of the correction factors in this relationship come from direct observation of the response of each gyroscope at multiple temperatures over the calibration temperature range ($-10^\circ\text{C} \leq T_C \leq +75^\circ\text{C}$). These correction factors are stored in the flash memory bank, but they are not available for observation or configuration. Register MSC_CTRL, Bit 7 (see Table 101) provides the only user configuration option for the factory calibration of the gyroscopes: an on/off control for the linear g compensation. See Figure 40 for more details on the user calibration options that are available for the gyroscopes.

The factory calibration of the accelerometer applies the following correction formulas to the data of each accelerometer:

$$\begin{bmatrix} a_{XC} \\ a_{YC} \\ a_{ZC} \end{bmatrix} = \begin{bmatrix} m_{11} & m_{12} & m_{13} \\ m_{21} & m_{22} & m_{23} \\ m_{31} & m_{32} & m_{33} \end{bmatrix} \times \begin{bmatrix} a_X \\ a_Y \\ a_Z \end{bmatrix} + \begin{bmatrix} b_X \\ b_Y \\ b_Z \end{bmatrix} + \begin{bmatrix} 0 & p_{12} & p_{13} \\ p_{21} & 0 & p_{23} \\ p_{31} & p_{32} & 0 \end{bmatrix} \times \begin{bmatrix} \omega_{XC}^2 \\ \omega_{YC}^2 \\ \omega_{ZC}^2 \end{bmatrix}$$

where:

a_{XC} , a_{YC} , and a_{ZC} are the accelerometer outputs (post calibration).

m_{11} , m_{12} , m_{13} , m_{21} , m_{22} , m_{23} , m_{31} , m_{32} , and m_{33} provide scale and alignment correction.

a_X , a_Y , and a_Z are the accelerometer outputs (precalibration).

b_X , b_Y , and b_Z provide bias correction.

p_{12} , p_{13} , p_{21} , p_{23} , p_{31} and p_{32} provide point of percussion alignment correction to (see Figure 43).

ω_{XC}^2 , ω_{YC}^2 , and ω_{ZC}^2 are the square of the gyroscope outputs (post calibration).

All of the correction factors in this relationship come from direct observation of the response of each accelerometer at multiple temperatures, over the calibration temperature range ($-10^{\circ}\text{C} \leq \text{TC} \leq +75^{\circ}\text{C}$). These correction factors are stored in the flash memory bank; but they are not available for observation or configuration. MSC_CTRL, Bit 6 (see Table 101) provides the only user configuration option for the factory calibration of the accelerometers: an on/off control for the point of percussion, alignment function. See Figure 41 for more details on the user calibration options that are available for the accelerometers.

Bartlett Window FIR Filter

The Bartlett window finite impulse response (FIR) filter (see Figure 18) contains two averaging filter stages, in a cascade configuration. The FILT_CTRL register (see Table 99) provides the configuration controls for this filter.

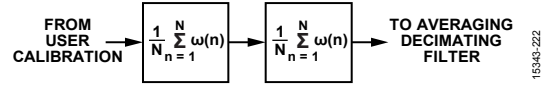


Figure 18. Bartlett Window FIR Filter Signal Path

Averaging/Decimating Filter

The second digital filter averages multiple samples together to produce each register update. In this type of filter structure, the number of samples in the average is equal to the reduction in the update rate for the output data registers. The DEC_RATE register (see Table 105) provides the configuration controls for this filter.

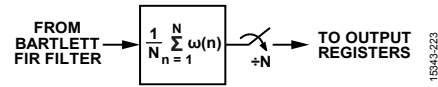


Figure 19. Averaging/Decimating Filter Diagram

REGISTER STRUCTURE

All communication between the ADIS16470 and an external processor involves either reading the contents of an output register or writing configuration/command information to a control register. The output data registers include the latest sensor data, error flags, and identification information. The control registers include sample rate, filtering, calibration, and diagnostic options. Each user accessible register has two bytes (upper and lower), each of which have their own unique address. See Table 8 for a detailed list of all user registers, along with their addresses.

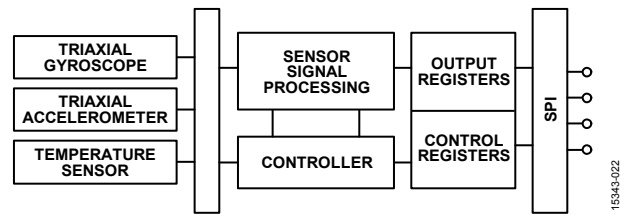


Figure 20. Basic Operation of the ADIS16470

SERIAL PERIPHERAL INTERFACE (SPI)

The SPI provides access to the user registers (see Table 8). Figure 21 provides the most common connections between the ADIS16470 and a SPI master, which is often an embedded processor that has a SPI-compatible interface. In this example, the SPI master uses an interrupt service routine to collect data every time the data ready (DR) signal pulses.

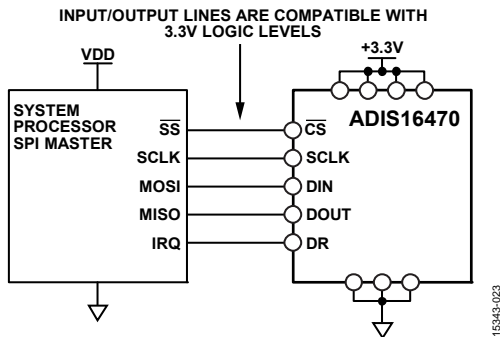


Figure 21. Electrical Connection Diagram

Table 6. Generic SPI Master Pin Names and Functions

| Mnemonic | Function |
|----------|----------------------------|
| SS | Slave select |
| SCLK | Serial clock |
| MOSI | Master output, slave input |
| MISO | Master input, slave output |
| IRQ | Interrupt request |

Embedded processors typically use control registers to configure their serial ports for communicating with SPI slave devices such as the ADIS16470. Table 7 provides a list of settings that describe the SPI protocol of the ADIS16470. The initialization routine of the master processor typically establishes these settings using firmware commands to write them into its control registers.

Table 7. Generic Master Processor SPI Settings

| Processor Setting | Description |
|-----------------------------|--|
| Master | ADIS16470 operates as slave |
| $SCLK \leq 2 \text{ MHz}^1$ | Maximum serial clock rate |
| SPI Mode 3 | CPOL = 1 (polarity), CPHA = 1 (phase) |
| MSB First Mode | Bit sequence, see Figure 26 for coding |
| 16-Bit Mode | Shift register and data length |

¹ Burst mode read requires this to be $\leq 1 \text{ MHz}$ (see Table 2 for more information).

DATA READY (DR)

The factory default configuration provides users with a DR signal on the DR pin (see Table 5), which pulses when the output data registers are updating. Connect this with a pin on the embedded processor, which triggers data collection, on the second edge of this pulse. The MSC_CTRL register, Bit 0 (see Table 101), controls the polarity of this signal. In Figure 22, Register MSC_CTRL, Bit 0 = 1, which means that data collection must start on the rising edges of the DR pulses.

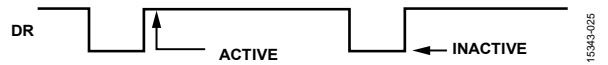


Figure 22. Data Ready When Register MSC_CTRL, Bit 0 = 1 (Default)

During the startup and reset recovery processes, the DR signal may exhibit some transient behavior before data production begins. Figure 23 provides an example of the DR behavior during startup, and Figure 24 and Figure 25 provide examples of the DR behavior during recovery from reset commands.

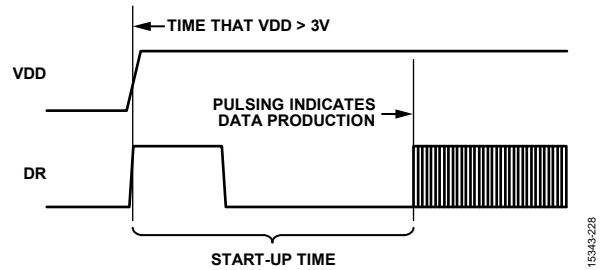


Figure 23. Data Ready Response During Startup

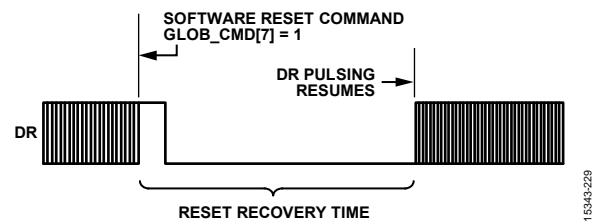


Figure 24. Data Ready Response During Reset (Register GLOB_CMD, Bit 7 = 1) Recovery

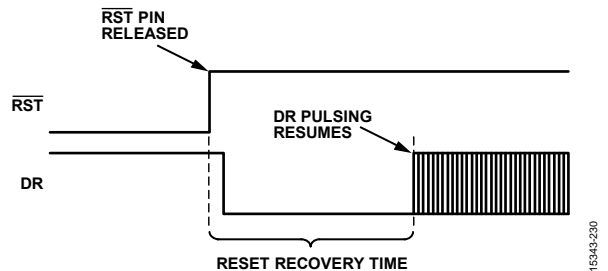
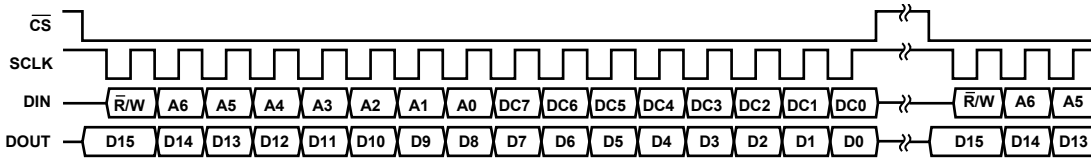


Figure 25. Data Ready Response During Reset ($\overline{RST} = 0$) Recovery



- NOTES
1. DOUT BITS ARE PRODUCED ONLY WHEN THE PREVIOUS 16-BIT DIN SEQUENCE STARTS WITH $\bar{R}/W = 0$.
 2. WHEN \bar{CS} IS HIGH, DOUT IS IN A THREE-STATE, HIGH IMPEDANCE MODE, WHICH ALLOWS MULTIFUNCTIONAL USE OF THE LINE FOR OTHER DEVICES.

Figure 26. SPI Communication Bit Sequence

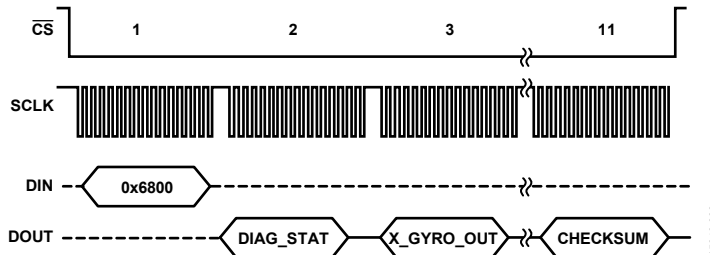


Figure 27. Burst Read Sequence

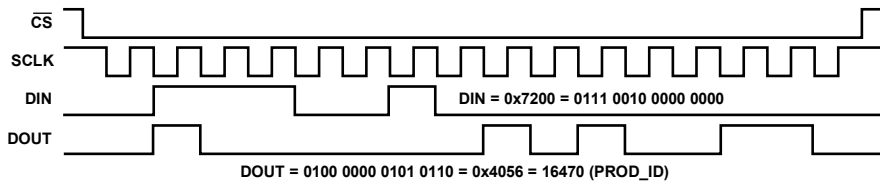


Figure 28. SPI Signal Patter, Repeating Read of the PROD_ID Register

READING SENSOR DATA

Reading a single register requires two 16-bit cycles on the SPI: one to request the contents of a register and another to receive those contents. The 16-bit command code (see Figure 26) for a read request on the SPI has three parts: the read bit ($\bar{R}/W = 0$), either address of the register, [A6:A0], and eight don't care bits, [DC7:DC0]. Figure 29 provides an example that includes two register reads in succession. This example starts with $DIN = 0x0C00$, to request the contents of the Z_GYRO_LOW register, and follows with $0x0E00$, to request the contents of the Z_GYRO_OUT register. The sequence in Figure 29 also illustrates full duplex mode of operation, which means that the ADIS16470 can receive requests on DIN while also transmitting data out on DOUT within the same 16-bit SPI cycle.



Figure 29. SPI Read Example

Figure 28 provides an example of the four SPI signals when reading the PROD_ID register (see Table 117) in a repeating pattern. This pattern can be helpful when troubleshooting the SPI interface setup and communications because the signals are the same for each 16-bit sequence, except during the first cycle.

Burst Read Function

The burst read function provides a way to read a batch of output data registers, using a continuous stream of bits, at a rate of up to 1 MHz (SCLK). This method does not require a stall time between each 16-bit segment (see Figure 3). As shown in Figure 27, start this mode by setting $DIN = 0x6800$, and then read each of the registers in the sequence out of DOUT while keeping \bar{CS} low for the entire 176-bit sequence.

The sequence of registers (and checksum value) in the burst read response depends on which sample clock mode that the ADIS16470 is operating in (Register MSC_CTRL, Bits[4:2], see Table 101). In all clock modes, except when operating in scaled sync mode (Register MSC_CTRL, Bits[4:2] = 010), the burst read response includes the following registers and checksum value: DIAG_STAT, X_GYRO_OUT, Y_GYRO_OUT, Z_GYRO_OUT, X_ACCL_OUT, Y_ACCL_OUT, Z_ACCL_OUT, TEMP_OUT, DATA_CNTR, and checksum. In these cases, use the following formula to verify the checksum value, treating each byte in the formula as an independent, unsigned, 8-bit number:

$$Checksum = DIAG_STAT, Bits[15:8] + DIAG_STAT, Bits[7:0] + X_GYRO_OUT, Bits[15:8] + X_GYRO_OUT, Bits[7:0] + Y_GYRO_OUT, Bits[15:8] + Y_GYRO_OUT, Bits[7:0] + Z_GYRO_OUT, Bits[15:8] + Z_GYRO_OUT, Bits[7:0] + X_ACCL_OUT, Bits[15:8] + X_ACCL_OUT, Bits[7:0] + Y_ACCL_OUT, Bits[15:8] + Y_ACCL_OUT, Bits[7:0] + Z_ACCL_OUT, Bits[15:8] + Z_ACCL_OUT, Bits[7:0] + TEMP_OUT, Bits[15:8] + TEMP_OUT, Bits[7:0] + DATA_CNTR, Bits[15:8] + DATA_CNTR, Bits[7:0]$$

When operating in scaled sync mode (Register MSC_CTRL, Bits[4:2] = 010), the burst read response includes the following registers and value: DIAG_STAT, X_GYRO_OUT, Y_GYRO_OUT, Z_GYRO_OUT, X_ACCL_OUT, Y_ACCL_OUT, Z_ACCL_OUT, TEMP_OUT, TIME_STMP, and the checksum value. In this case, use the following formula to verify the checksum value, treating each byte in the formula as an independent, unsigned, 8-bit number.

$$\begin{aligned} \text{Checksum} = & \text{DIAG_STAT, Bits}[15:8] + \text{DIAG_STAT, Bits}[7:0] + \\ & \text{X_GYRO_OUT, Bits}[15:8] + \text{X_GYRO_OUT, Bits}[7:0] + \\ & \text{Y_GYRO_OUT, Bits}[15:8] + \text{Y_GYRO_OUT, Bits}[7:0] + \\ & \text{Z_GYRO_OUT, Bits}[15:8] + \text{Z_GYRO_OUT, Bits}[7:0] + \\ & \text{X_ACCL_OUT, Bits}[15:8] + \text{X_ACCL_OUT, Bits}[7:0] + \\ & \text{Y_ACCL_OUT, Bits}[15:8] + \text{Y_ACCL_OUT, Bits}[7:0] + \\ & \text{Z_ACCL_OUT, Bits}[15:8] + \text{Z_ACCL_OUT, Bits}[7:0] + \\ & \text{TEMP_OUT, Bits}[15:8] + \text{TEMP_OUT, Bits}[7:0] + \\ & \text{TIME_STMP, Bits}[15:8] + \text{TIME_STMP, Bits}[7:0] \end{aligned}$$

DEVICE CONFIGURATION

Each configuration register contains 16 bits (two bytes). Bits[7:0] contain the low byte, and Bits[15:8] contain the high byte of each register. Each byte has its own unique address in the user register map (see Table 8). Updating the contents of a register requires writing to both of its bytes in the following sequence: low byte first, high byte second. There are three parts to coding a SPI command (see Figure 26) that write a new byte of data to a register: the write bit (R/W = 1), the address of the byte, [A6:A0], and the new data for that location, [DC7:DC0]. Figure 30 provides a coding example for writing 0x0004 to the FILT_CTRL register (see Table 99). In Figure 30, the 0xDC04 command writes 0x04 to Address 0x5C (lower byte) and the 0xDD00 command writes 0x00 to Address 0x5D (upper byte).

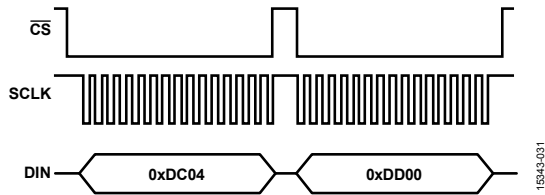


Figure 30. SPI Sequence for Writing 0x0004 to FILT_CTRL

Memory Structure

Figure 31 provides a functional diagram for the memory structure of the ADIS16470. The flash memory bank contains the operational code, unit specific calibration coefficients and user configuration settings. During initialization (power application or reset recover), this information loads from the flash memory into the SRAM, which supports all normal operation, including register access through the SPI port. Writing to a configuration register (using the SPI) updates its SRAM location but does not automatically update its settings in the flash memory bank. The manual flash memory update command (Register GLOB_CMD, Bit 3, see Table 109) provides a convenient method for saving all of these settings to the flash memory bank at one time. A Yes in the flash back-up column of Table 8 identifies the registers that have storage support in the flash memory bank.

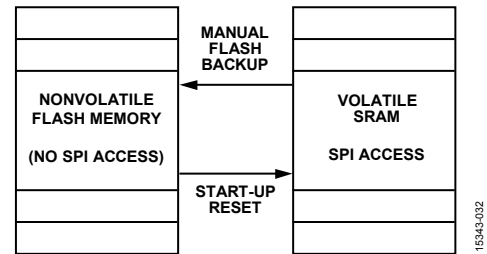


Figure 31. SRAM and Flash Memory Diagram

USER REGISTER MEMORY MAP

Table 8. User Register Memory Map (N/A Means Not Applicable)

| Name | R/W | Flash Backup | Address | Default | Register Description |
|---------------|-----|--------------|--------------|---------|--|
| Reserved | N/A | N/A | 0x00, 0x01 | N/A | Reserved |
| DIAG_STAT | R | No | 0x02, 0x03 | 0x0000 | Output, system error flags |
| X_GYRO_LOW | R | No | 0x04, 0x05 | N/A | Output, x-axis gyroscope, low word |
| X_GYRO_OUT | R | No | 0x06, 0x07 | N/A | Output, x-axis gyroscope, high word |
| Y_GYRO_LOW | R | No | 0x08, 0x09 | N/A | Output, y-axis gyroscope, low word |
| Y_GYRO_OUT | R | No | 0x0A, 0x0B | N/A | Output, y-axis gyroscope, high word |
| Z_GYRO_LOW | R | No | 0x0C, 0x0D | N/A | Output, z-axis gyroscope, low word |
| Z_GYRO_OUT | R | No | 0x0E, 0x0F | N/A | Output, z-axis gyroscope, high word |
| X_ACCL_LOW | R | No | 0x10, 0x11 | N/A | Output, x-axis accelerometer, low word |
| X_ACCL_OUT | R | No | 0x12, 0x13 | N/A | Output, x-axis accelerometer, high word |
| Y_ACCL_LOW | R | No | 0x14, 0x15 | N/A | Output, y-axis accelerometer, low word |
| Y_ACCL_OUT | R | No | 0x16, 0x17 | N/A | Output, y-axis accelerometer, high word |
| Z_ACCL_LOW | R | No | 0x18, 0x19 | N/A | Output, z-axis accelerometer, low word |
| Z_ACCL_OUT | R | No | 0x1A, 0x1B | N/A | Output, z-axis accelerometer, high word |
| TEMP_OUT | R | No | 0x1C, 0x1D | N/A | Output, temperature |
| TIME_STAMP | R | No | 0x1E, 0x1F | N/A | Output, time stamp |
| Reserved | N/A | N/A | 0x20, 0x21 | N/A | Reserved |
| DATA_CNTR | R | No | 0x22, 0x23 | N/A | New data counter |
| X_DELTANG_LOW | R | No | 0x24, 0x25 | N/A | Output, x-axis delta angle, low word |
| X_DELTANG_OUT | R | No | 0x26, 0x27 | N/A | Output, x-axis delta angle, high word |
| Y_DELTANG_LOW | R | No | 0x28, 0x29 | N/A | Output, y-axis delta angle, low word |
| Y_DELTANG_OUT | R | No | 0x2A, 0x2B | N/A | Output, y-axis delta angle, high word |
| Z_DELTANG_LOW | R | No | 0x2C, 0x2D | N/A | Output, z-axis delta angle, low word |
| Z_DELTANG_OUT | R | No | 0x2E, 0x2F | N/A | Output, z-axis delta angle, high word |
| X_DELTVEL_LOW | R | No | 0x30, 0x31 | N/A | Output, x-axis delta velocity, low word |
| X_DELTVEL_OUT | R | No | 0x32, 0x33 | N/A | Output, x-axis delta velocity, high word |
| Y_DELTVEL_LOW | R | No | 0x34, 0x35 | N/A | Output, y-axis delta velocity, low word |
| Y_DELTVEL_OUT | R | No | 0x36, 0x37 | N/A | Output, y-axis delta velocity, high word |
| Z_DELTVEL_LOW | R | No | 0x38, 0x39 | N/A | Output, z-axis delta velocity, low word |
| Z_DELTVEL_OUT | R | No | 0x3A, 0x3B | N/A | Output, z-axis delta velocity, high word |
| Reserved | N/A | N/A | 0x3C to 0x3F | N/A | Reserved |
| XG_BIAS_LOW | R/W | Yes | 0x40, 0x41 | 0x0000 | Calibration, offset, gyroscope, x-axis, low word |
| XG_BIAS_HIGH | R/W | Yes | 0x42, 0x43 | 0x0000 | Calibration, offset, gyroscope, x-axis, high word |
| YG_BIAS_LOW | R/W | Yes | 0x44, 0x45 | 0x0000 | Calibration, offset, gyroscope, y-axis, low word |
| YG_BIAS_HIGH | R/W | Yes | 0x46, 0x47 | 0x0000 | Calibration, offset, gyroscope, y-axis, high word |
| ZG_BIAS_LOW | R/W | Yes | 0x48, 0x49 | 0x0000 | Calibration, offset, gyroscope, z-axis, low word |
| ZG_BIAS_HIGH | R/W | Yes | 0x4A, 0x4B | 0x0000 | Calibration, offset, gyroscope, z-axis, high word |
| XA_BIAS_LOW | R/W | Yes | 0x4C, 0x4D | 0x0000 | Calibration, offset, accelerometer, x-axis, low word |
| XA_BIAS_HIGH | R/W | Yes | 0x4E, 0x4F | 0x0000 | Calibration, offset, accelerometer, x-axis, high word |
| YA_BIAS_LOW | R/W | Yes | 0x50, 0x51 | 0x0000 | Calibration, offset, accelerometer, y-axis, low word |
| YA_BIAS_HIGH | R/W | Yes | 0x52, 0x53 | 0x0000 | Calibration, offset, accelerometer, y-axis, high word |
| ZA_BIAS_LOW | R/W | Yes | 0x54, 0x55 | 0x0000 | Calibration, offset, accelerometer, z-axis, low word |
| ZA_BIAS_HIGH | R/W | Yes | 0x56, 0x57 | 0x0000 | Calibration, offset, accelerometer, z-axis, high word |
| Reserved | N/A | N/A | 0x58 to 0x5B | N/A | Reserved |
| FILT_CTRL | R/W | Yes | 0x5C, 0x5D | 0x0000 | Control, Bartlett window FIR filter |
| Reserved | N/A | N/A | 0x5E, 0x5F | N/A | Reserved |
| MSC_CTRL | R/W | Yes | 0x60, 0x61 | 0x00C1 | Control, input/output and other miscellaneous options |
| UP_SCALE | R/W | Yes | 0x62, 0x63 | 0x07D0 | Control, scale factor for input clock, pulse per second (PPS) mode |
| DEC_RATE | R/W | Yes | 0x64, 0x65 | 0x0000 | Control, decimation filter (output data rate) |

| Name | R/W | Flash Backup | Address | Default | Register Description |
|--------------|-----|--------------|--------------|---------|--|
| NULL_CNFG | R/W | Yes | 0x66, 0x67 | 0x070A | Control, bias estimation period |
| GLOB_CMD | W | No | 0x68, 0x69 | N/A | Control, global commands |
| Reserved | N/A | N/A | 0x6A to 0x6B | N/A | Reserved |
| FIRM_REV | R | N/A | 0x6C, 0x6D | N/A | Identification, firmware revision |
| FIRM_DM | R | N/A | 0x6E, 0x6F | N/A | Identification, date code, day and month |
| FIRM_Y | R | N/A | 0x70, 0x71 | N/A | Identification, date code, year |
| PROD_ID | R | N/A | 0x72, 0x73 | 0x4056 | Identification, part number |
| SERIAL_NUM | R | N/A | 0x74, 0x75 | N/A | Identification, serial number |
| USER_SCR1 | R/W | N/A | 0x76, 0x77 | N/A | User Scratch Register 1 |
| USER_SCR2 | R/W | N/A | 0x78, 0x79 | N/A | User Scratch Register 2 |
| USER_SCR3 | R/W | N/A | 0x7A, 0x7B | N/A | User Scratch Register 3 |
| FLSHCNT_LOW | R | N/A | 0x7C, 0x7D | N/A | Output, flash memory write cycle counter, lower word |
| FLSHCNT_HIGH | R | N/A | 0x7E, 0x7E | N/A | Output, flash memory write cycle counter, upper word |

USER REGISTER DEFINITIONS

Status/Error Flag Indicators (DIAG_STAT)

Table 9. DIAG_STAT Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|---------|--------|--------------|
| 0x02, 0x03 | 0x0000 | R | No |

Table 10. DIAG_STAT Bit Assignments

| Bits | Description |
|--------|--|
| [15:8] | Reserved. |
| 7 | Clock error. A 1 indicates that the internal data sampling clock (f_{SM} , see Figure 15 and Figure 16) does not synchronize with the external clock, which only applies when using scale sync mode (Register MSC_CTRL, Bits[4:2] = 010, see Table 101). When this occurs, adjust the frequency of the clock signal on the SYNC pin to operate within the appropriate range. |
| 6 | Memory failure. A 1 indicates a failure in the flash memory test (Register GLOB_CMD, Bit 4, see Table 109), which involves a comparison between a cyclic redundancy check (CRC) computation of the present flash memory and a CRC computation from the same memory locations at the time of initial programming (during production process). If this occurs, repeat the same test. If this error persists, replace the ADIS16470 device. |
| 5 | Sensor failure. A 1 indicates failure of at least one sensor, at the conclusion of the self test (Register GLOB_CMD, Bit 2, see Table 109). If this occurs, repeat the same test. If this error persists, replace the ADIS16470. Motion, during the execution of this test, can cause a false failure. |
| 4 | Standby mode. A 1 indicates that the voltage across VDD and GND is <2.8 V, which causes data processing to stop. When VDD \geq 2.8 V for 250 ms, the ADIS16470 reinitializes itself and starts producing data again. |
| 3 | SPI communication error. A 1 indicates that the total number of SCLK cycles is not equal to an integer multiple of 16. When this occurs, repeat the previous communication sequence. Persistence in this error may indicate a weakness in the SPI service that the ADIS16470 is receiving from the system it is supporting. |
| 2 | Flash memory update failure. A 1 indicates that the most recent flash memory update (Register GLOB_CMD, Bit 3, see Table 109) failed. If this occurs, ensure that VDD \geq 3 V and repeat the update attempt. If this error persists, replace the ADIS16470. |
| 1 | Data path overrun. A 1 indicates that one of the data paths have experienced an overrun condition. If this occurs, initiate a reset, using the RST pin (see Table 5, Pin F3) or Register GLOB_CMD, Bit 7 (see Table 109). |
| 0 | Reserved |

The DIAG_STAT register (see Table 9 and Table 10) provides error flags for monitoring the integrity and operation of the ADIS16470. Reading this register causes all of its bits to return to 0. The error flags in DIAG_STAT are sticky, meaning that when they raise to a 1 value that they remain there until a read request clears them. If an error condition persists, its flag (bit) automatically returns to an alarm value of 1.

GYROSCOPE DATA

The gyroscopes in the ADIS16470 measure the angular rate of rotation around three orthogonal axes (x, y, and z). Figure 32 illustrates the orientation of each gyroscope axis, along with the direction of rotation that produces a positive response in each of their measurements.

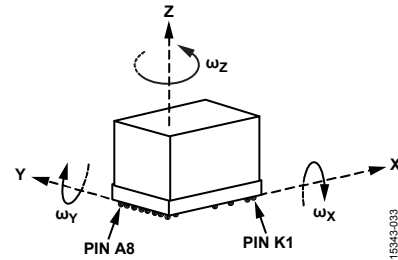


Figure 32. Gyroscope Axis and Polarity Assignments

Each gyroscope has two output data registers. Figure 33 illustrates how these two registers combine to support a 32-bit, twos complement data format for the x-axis gyroscope measurements. This format also applies to the y- and z-axes.

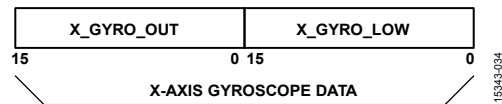


Figure 33. Gyroscope Output Data Structure

Gyroscope Data Formatting

Table 11 and Table 12 offer various numerical examples that demonstrate the format of the rotation rate data in both 16-bit and 32-bit formats.

Table 11. 16-Bit Gyroscope Data Format Examples

| Rotation Rate | Decimal | Hex | Binary |
|---------------|---------|--------|---------------------|
| +2000°/sec | +20,000 | 0x4E20 | 0100 1110 0010 0000 |
| +0.2°/sec | +2 | 0x0002 | 0000 0000 0000 0010 |
| +0.1°/sec | +1 | 0x0001 | 0000 0000 0000 0001 |
| 0°/sec | 0 | 0x0000 | 0000 0000 0000 0000 |
| -0.1°/sec | -1 | 0xFFFF | 1111 1111 1111 1111 |
| -0.2°/sec | -2 | 0xFFFE | 1111 1111 1111 1110 |
| -2000°/sec | -20,000 | 0xB1E0 | 1011 0001 1110 0000 |

Table 12. 32-Bit Gyroscope Data Format Examples

| Rotation Rate | Decimal | Hex |
|---------------------------|----------------|------------|
| +2000°/sec | +1,310,720,000 | 0x4E200000 |
| +0.1°/sec/2 ¹⁵ | +2 | 0x00000002 |
| +0.1°/sec/2 ¹⁶ | +1 | 0x00000001 |
| 0°/sec | 0 | 0x00000000 |
| -0.1°/sec/2 ¹⁶ | -1 | 0xFFFFFFFF |
| -0.1°/sec/2 ¹⁵ | -2 | 0xFFFFFFFF |
| -2000°/sec | -1,310,720,000 | 0xB1E00000 |

X-Axis Gyroscope (X_GYRO_LOW and X_GYRO_OUT)

Table 13. X_GYRO_LOW Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x04, 0x05 | Not applicable | R | No |

Table 14. X_GYRO_LOW Bit Definitions

| Bits | Description |
|--------|---|
| [15:0] | X-axis gyroscope data; additional resolution bits |

Table 15. X_GYRO_OUT Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x06, 0x07 | Not applicable | R | No |

Table 16. X_GYRO_OUT Bit Definitions

| Bits | Description |
|--------|--|
| [15:0] | X-axis gyroscope data; high word; twos complement, 0°/sec = 0x0000, 1 LSB = 0.1°/sec |

The X_GYRO_LOW (see Table 13 and Table 14) and X_GYRO_OUT (see Table 15 and Table 16) registers contain the gyroscope data for the x-axis.

Y-Axis Gyroscope (Y_GYRO_LOW and Y_GYRO_OUT)

Table 17. Y_GYRO_LOW Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x08, 0x09 | Not applicable | R | No |

Table 18. Y_GYRO_LOW Bit Definitions

| Bits | Description |
|--------|---|
| [15:0] | Y-axis gyroscope data; additional resolution bits |

Table 19. Y_GYRO_OUT Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x0A, 0x0B | Not applicable | R | No |

Table 20. Y_GYRO_OUT Bit Definitions

| Bits | Description |
|--------|--|
| [15:0] | Y-axis gyroscope data; high word; twos complement, 0°/sec = 0x0000, 1 LSB = 0.1°/sec |

The Y_GYRO_LOW (see Table 17 and Table 18) and Y_GYRO_OUT (see Table 19 and Table 20) registers contain the gyroscope data for the y-axis.

Z-Axis Gyroscope (Z_GYRO_LOW and Z_GYRO_OUT)

Table 21. Z_GYRO_LOW Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x0C, 0x0D | Not applicable | R | No |

Table 22. Z_GYRO_LOW Bit Definitions

| Bits | Description |
|--------|---|
| [15:0] | Z-axis gyroscope data; additional resolution bits |

Table 23. Z_GYRO_OUT Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x0E, 0x0F | Not applicable | R | No |

Table 24. Z_GYRO_OUT Bit Definitions

| Bits | Description |
|--------|--|
| [15:0] | Z-axis gyroscope data; high word; twos complement, 0°/sec = 0x0000, 1 LSB = 0.1°/sec |

The Z_GYRO_LOW (see Table 21 and Table 22) and Z_GYRO_OUT (see Table 23 and Table 24) registers contain the gyroscope data for the z-axis.

Acceleration Data

The accelerometers in the ADIS16470 measure both dynamic and static (response to gravity) acceleration along the same three orthogonal axes that define the axes of rotation for the gyroscopes (x, y, and z). Figure 34 illustrates the orientation of each accelerometer axis, along with the direction of acceleration that produces a positive response in each of their measurements.

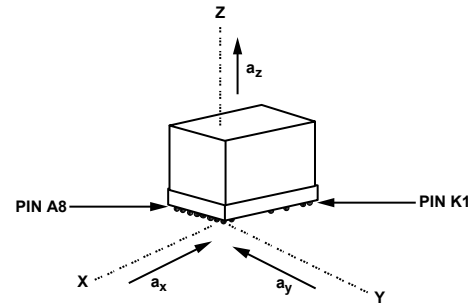


Figure 34. Accelerometer Axis and Polarity Assignments

Each accelerometer has two output data registers. Figure 35 shows how these two registers combine to support a 32-bit, twos complement data format for the x-axis accelerometer measurements. This format also applies to the y- and z-axes.

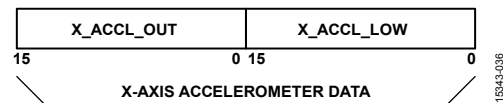


Figure 35. Accelerometer Output Data Structure

Accelerometer Resolution

Table 25 and Table 26 offer various numerical examples that demonstrate the format of the linear acceleration data in both 16-bit and 32-bit formats.

Table 25. 16-Bit Accelerometer Data Format Examples

| Acceleration | Decimal | Hex | Binary |
|--------------|---------|--------|---------------------|
| +40 g | +32,000 | 0x7D00 | 0111 1101 0000 0000 |
| +2.5 mg | +2 | 0x0002 | 0000 0000 0000 0010 |
| +1.25 mg | +1 | 0x0001 | 0000 0000 0000 0001 |
| 0 mg | 0 | 0x0000 | 0000 0000 0000 0000 |
| -1.25 mg | -1 | 0xFFFF | 1111 1111 1111 1111 |
| -2.5 mg | -2 | 0xFFFE | 1111 1111 1111 1110 |
| -40 g | -32,000 | 0x8300 | 1000 0011 0000 0000 |

Table 26. 32-Bit Accelerometer Data Format Examples

| Acceleration (g) | Decimal | Hex |
|--------------------------|----------------|-------------|
| +40 g | +2,097,152,000 | 0x7D000000 |
| +1.25/2 ¹⁵ mg | +2 | 0x00000002 |
| +1.25/2 ¹⁶ mg | +1 | 0x00000001 |
| 0 | 0 | 0x00000000 |
| -1.25/2 ¹⁶ mg | -1 | 0xFFFFFFFF |
| -1.25/2 ¹⁵ mg | -2 | 0xFFFFFFFFE |
| -40 g | -2,097,152,000 | 0x83000000 |

X-Axis Accelerometer (X_ACCL_LOW and X_ACCL_OUT)

Table 27. X_ACCL_LOW Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x10, 0x11 | Not applicable | R | No |

Table 28. X_ACCL_LOW Bit Definitions

| Bits | Description |
|--------|---|
| [15:0] | X-axis accelerometer data; additional resolution bits |

Table 29. X_ACCL_OUT Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x12, 0x13 | Not applicable | R | No |

Table 30. X_ACCL_OUT Bit Definitions

| Bits | Description |
|--------|--|
| [15:0] | X-axis accelerometer data, high word; twos complement, ±40g range; 0 g = 0x0000, 1 LSB = 1.25 mg |

The X_ACCL_LOW (see Table 27 and Table 28) and X_ACCL_OUT (see Table 29 and Table 30) registers contain the accelerometer data for the x-axis.

Y-Axis Accelerometer (Y_ACCL_LOW and Y_ACCL_OUT)

Table 31. Y_ACCL_LOW Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x14, 0x15 | Not applicable | R | No |

Table 32. Y_ACCL_LOW Bit Definitions

| Bits | Description |
|--------|---|
| [15:0] | Y-axis accelerometer data; additional resolution bits |

Table 33. Y_ACCL_OUT Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x16, 0x17 | Not applicable | R | No |

Table 34. Y_ACCL_OUT Bit Definitions

| Bits | Description |
|--------|--|
| [15:0] | Y-axis accelerometer data, high word; twos complement, ±40g range; 0 g = 0x0000, 1 LSB = 1.25 mg |

The Y_ACCL_LOW (see Table 31 and Table 32) and Y_ACCL_OUT (see Table 33 and Table 34) registers contain the accelerometer data for the y-axis.

Z-Axis Accelerometer (Z_ACCL_LOW and Z_ACCL_OUT)

Table 35. Z_ACCL_LOW Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x18, 0x19 | Not applicable | R | No |

Table 36. Z_ACCL_LOW Bit Definitions

| Bits | Description |
|--------|---|
| [15:0] | Z-axis accelerometer data; additional resolution bits |

Table 37. Z_ACCL_OUT Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x1A, 0x1B | Not applicable | R | No |

Table 38. Z_ACCL_OUT Bit Definitions

| Bits | Description |
|--------|--|
| [15:0] | Z-axis accelerometer data, high word; twos complement, ±40g range; 0 g = 0x0000, 1 LSB = 1.25 mg |

The Z_ACCL_LOW (see Table 35 and Table 36) and Z_ACCL_OUT (see Table 37 and Table 38) registers contain the accelerometer data for the z-axis.

Internal Temperature (TEMP_OUT)

Table 39. TEMP_OUT Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x1C, 0x1D | Not applicable | R | No |

Table 40. TEMP_OUT Bit Definitions

| Bits | Description |
|--------|--|
| [15:0] | Temperature data; twos complement, 1 LSB = 0.1°C, 0°C = 0x0000 |

The TEMP_OUT register (see Table 39 and Table 40) provides a coarse measurement of the temperature inside of the ADIS16470. This data is most useful for monitoring relative changes in the thermal environment.

Table 41. TEMP_OUT Data Format Examples

| Temperature (°C) | Decimal | Hex | Binary |
|------------------|---------|---------|---------------------|
| +85 | +850 | 0x0352 | 0000 0011 0101 0010 |
| +70 | +700 | 0x02BC | 0000 0010 1011 1100 |
| +25 | +250 | 0x00FA | 0000 0000 1111 1010 |
| +0.2 | +2 | 0x0002 | 0000 0000 0000 0010 |
| +0.1 | +1 | 0x0001 | 0000 0000 0000 0001 |
| +0 | 0 | 0x0000 | 0000 0000 0000 0000 |
| +0.1 | -1 | 0xFFFF | 1111 1111 1111 1111 |
| +0.2 | -2 | 0xFFFFE | 1111 1111 1111 1110 |
| -25 | -250 | 0xFF06 | 1111 1111 0000 0110 |

Time Stamp (TIME_STAMP)

Table 42. TIME_STAMP Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x1E, 0x1F | Not applicable | R | No |

Table 43. TIME_STAMP Bit Definitions

| Bits | Description |
|--------|--|
| [15:0] | Time from the last pulse on the SYNC pin; offset binary format, 1 LSB = 49.02 μs |

The TIME_STAMP (see Table 42 and Table 43) register works in conjunction with scaled sync mode (Register MSC_CTRL, Bits[4:2] = 010, see Table 101). The 16-bit number in TIME_STAMP contains the time associated with the last sample in each data update relative to the most recent edge of the clock signal in the SYNC pin. For example, when the value in the UP_SCALE register (see Table 103) represents a scale factor of 20, DEC_RATE = 0, and the external SYNC rate of 100 Hz results in the following time stamp sequence: 0 LSB, 10 LSB, 21 LSB, 31 LSB, 41 LSB, 51 LSB, 61 LSB, 72 LSB, ..., 194 LSB for the 20th sample, which translates to 0 μs, 490 μs, ..., 9510 μs which is the time from the first SYNC edge.

Data Update Counter (DATA_CNTR)

Table 44. DATA_CNTR Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x22, 0x23 | Not applicable | R | No |

Table 45. DATA_CNTR Bit Definitions

| Bits | Description |
|--------|---|
| [15:0] | Data update counter, offset binary format |

When the ADIS16470 goes through its power-on sequence or when it recovers from a reset command, DATA_CNTR (see Table 44 and Table 45) starts with a value of 0x0000 and increments every time new data loads into the output registers. When it reaches 0xFFFF, the next data update causes it to wrap back around to 0x0000, where it continues to increment every time new data loads into the output registers.

DELTA ANGLES

In addition to the angular rate of rotation (gyroscope) measurements around each axis (x, y, and z), the ADIS16470 also provides delta angle measurements that represent a computation of angular displacement between each sample update.

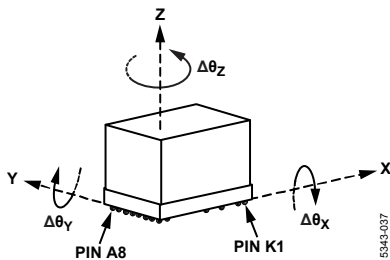


Figure 36. Delta Angle Axis and Polarity Assignments

The delta angle outputs represent an integration of the gyroscope measurements and use the following formula for all three axes (x-axis displayed):

$$\Delta\theta_{x,nD} = \frac{1}{2 \times f_s} \times \sum_{d=0}^{D-1} (\omega_{x,nD+d} + \omega_{x,nD+d-1})$$

where:

x is the x-axis.

n is the sample time, prior to the decimation filter.

D is the decimation rate = DEC_RATE + 1 (see Table 105).

f_s is the sample rate.

d is the incremental variable in the summation formula.

ω_x is the x-axis rate of rotation (gyroscope).

When using the internal sample clock, f_s is equal to a nominal rate of 2000 SPS. For better precision in this measurement, measure the internal sample rate (f_s) using the data ready signal on the DR pin (DEC_RATE = 0x0000, see Table 104), divide each delta angle result (from the delta angle output registers) by the data ready frequency and multiply it by 2000. Each axis of the delta angle measurements has two output data registers. Figure 37 illustrates how these two registers combine to support a 32-bit, twos complement data format for the x-axis delta angle measurements. This format also applies to the y- and z-axes.

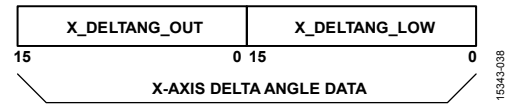


Figure 37. Delta Angle Output Data Structure

X-Axis Delta Angle (X_DELTANG_LOW and X_DELTANG_OUT)

Table 46. X_DELTANG_LOW Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x24, 0x25 | Not applicable | R | No |

Table 47. X_DELTANG_LOW Bit Definitions

| Bits | Description |
|--------|---|
| [15:0] | X-axis delta angle data; additional resolution bits |

Table 48. X_DELTANG_OUT Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x26, 0x27 | Not applicable | R | No |

Table 49. X_DELTANG_OUT Bit Definitions

| Bits | Description |
|--------|--|
| [15:0] | X-axis delta angle data; twos complement, 0° = 0x0000, 1 LSB = 2160°/2 ¹⁵ |

The X_DELTANG_LOW (see Table 46 and Table 47) and X_DELTANG_OUT (see Table 48 and Table 49) registers contain the delta angle data for the x-axis.

Y-Axis Delta Angle (Y_DELTANG_LOW and Y_DELTANG_OUT)

Table 50. Y_DELTANG_LOW Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x28, 0x29 | Not applicable | R | No |

Table 51. Y_DELTANG_LOW Bit Definitions

| Bits | Description |
|--------|---|
| [15:0] | Y-axis delta angle data; additional resolution bits |

Table 52. Y_DELTANG_OUT Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x2A, 0x2B | Not applicable | R | No |

Table 53. Y_DELTANG_OUT Bit Definitions

| Bits | Description |
|--------|--|
| [15:0] | Y-axis delta angle data; twos complement, 0° = 0x0000, 1 LSB = 2160°/2 ¹⁵ |

The Y_DELTANG_LOW (see Table 50 and Table 51) and Y_DELTANG_OUT (see Table 52 and Table 53) registers contain the delta angle data for the y-axis.

Z-Axis Delta Angle (Z_DELTANG_LOW and Z_DELTANG_OUT)

Table 54. Z_DELTANG_LOW Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x2C, 0x2D | Not applicable | R | No |

Table 55. Z_DELTANG_LOW Bit Definitions

| Bits | Description |
|--------|---|
| [15:0] | Z-axis delta angle data; additional resolution bits |

Table 56. Z_DELTANG_OUT Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x2E, 0x2F | Not applicable | R | No |

Table 57. Z_DELTANG_OUT Bit Definitions

| Bits | Description |
|--------|--|
| [15:0] | Z-axis delta angle data; twos complement, 0° = 0x0000, 1 LSB = 2160°/2 ¹⁵ |

The Z_DELTANG_LOW (see Table 54 and Table 55) and Z_DELTANG_OUT (see Table 56 and Table 57) registers contain the delta angle data for the z-axis.

Delta Angle Resolution

Table 58 and Table 59 offers various numerical examples that demonstrate the format of the delta angle data in both 16-bit and 32-bit formats.

Table 58. 16-Bit Delta Angle Data Format Examples

| Delta Angle (°) | Decimal | Hex | Binary |
|---|---------|--------|---------------------|
| 2160° × (2 ¹⁵ - 1) / 2 ¹⁵ | +32,767 | 0x7FFF | 0111 1111 1111 1111 |
| +2160°/2 ¹⁴ | +2 | 0x0002 | 0000 0000 0000 0010 |
| +2160°/2 ¹⁵ | +1 | 0x0001 | 0000 0000 0000 0001 |
| 0 | 0 | 0x0000 | 0000 0000 0000 0000 |
| -2160°/2 ¹⁵ | -1 | 0xFFFF | 1111 1111 1111 1111 |
| -2160°/2 ¹⁴ | -2 | 0xFFFE | 1111 1111 1111 1110 |
| -2160° | -32,768 | 0x8000 | 1000 0000 0000 0000 |

Table 59. 32-Bit Delta Angle Data Format Examples

| Delta Angle (°) | Decimal | Hex |
|--|----------------|-------------|
| +2160° × (2 ³¹ - 1) / 2 ³¹ | +2,147,483,647 | 0x7FFFFFFF |
| +2160°/2 ³⁰ | +2 | 0x00000002 |
| +2160°/2 ³¹ | +1 | 0x00000001 |
| 0 | 0 | 0x00000000 |
| -2160°/2 ³¹ | -1 | 0xFFFFFFFF |
| -2160°/2 ³⁰ | -2 | 0xFFFFFFFFE |
| -2160° | -2,147,483,648 | 0x80000000 |

DELTA VELOCITY

In addition to the linear acceleration measurements along each axis (x, y, and z), the ADIS16470 also provides delta velocity measurements that represent a computation of linear velocity change between each sample update.

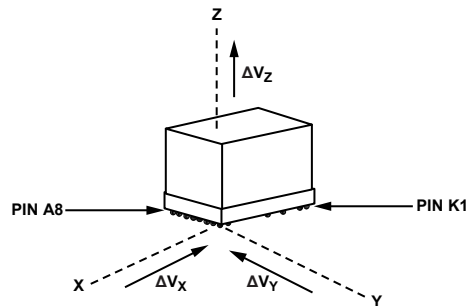


Figure 38. Delta Velocity Axis and Polarity Assignments

The delta velocity outputs represent an integration of the acceleration measurements and use the following formula for all three axes (x-axis displayed):

$$\Delta V_{x,nD} = \frac{1}{2 \times f_s} \times \sum_{d=0}^{D-1} (a_{x,nD+d} + a_{x,nD+d-1})$$

where:

x is the x-axis.

n is the sample time, prior to the decimation filter.

D is the decimation rate = DEC_RATE + 1 (see Table 105).

f_s is the sample rate.

d is the incremental variable in the summation formula.

a_x is the x-axis acceleration.

When using the internal sample clock, f_s is equal to a nominal rate of 2000 SPS. For better precision in this measurement, measure the internal sample rate (f_s) using the data ready signal on the DR pin (DEC_RATE = 0x0000, see Table 104), divide each delta angle result (from the delta angle output registers) by the data ready frequency and multiply it by 2000. Each axis of the delta velocity measurements has two output data registers. Figure 39 illustrates how these two registers combine to support 32-bit, twos complement data format for the delta velocity measurements along the x-axis. This format also applies to the y-axis and z-axis.

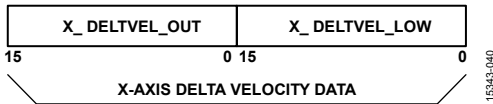


Figure 39. Delta Angle Output Data Structure

X-Axis Delta Velocity (X_DELTVEL_LOW and X_DELTVEL_OUT)

Table 60. X_DELTVEL_LOW Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x30, 0x31 | Not applicable | R | No |

Table 61. X_DELTVEL_LOW Bit Definitions

| Bits | Description |
|--------|--|
| [15:0] | X-axis delta velocity data; additional resolution bits |

Table 62. X_DELTVEL_OUT Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x32, 0x33 | Not applicable | R | No |

Table 63. X_DELTVEL_OUT Bit Definitions

| Bits | Description |
|--------|--|
| [15:0] | X-axis delta velocity data; twos complement, ± 400 m/sec range, 0 m/sec = 0x0000; 1 LSB = $400 \text{ m/sec} \div 2^{15} = \sim 0.01221 \text{ m/sec}$ |

The X_DELTVEL_LOW (see Table 60 and Table 61) and X_DELTVEL_OUT (see Table 62 and Table 63) registers contain the delta velocity data for the x-axis.

Y-Axis Delta Velocity (Y_DELTVEL_LOW and Y_DELTVEL_OUT)

Table 64. Y_DELTVEL_LOW Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x34, 0x35 | Not applicable | R | No |

Table 65. Y_DELTVEL_LOW Bit Definitions

| Bits | Description |
|--------|--|
| [15:0] | Y-axis delta velocity data; additional resolution bits |

Table 66. Y_DELTVEL_OUT Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x36, 0x37 | Not applicable | R | No |

Table 67. Y_DELTVEL_OUT Bit Definitions

| Bits | Description |
|--------|--|
| [15:0] | Y-axis delta velocity data; twos complement, ± 400 m/sec range, 0 m/sec = 0x0000; 1 LSB = $400 \text{ m/sec} \div 2^{15} = \sim 0.01221 \text{ m/sec}$ |

The Y_DELTVEL_LOW (see Table 64 and Table 65) and Y_DELTVEL_OUT (see Table 66 and Table 67) registers contain the delta velocity data for the y-axis.

Z-Axis Delta Velocity (Z_DELTVEL_LOW and Z_DELTVEL_OUT)

Table 68. Z_DELTVEL_LOW Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x38, 0x39 | Not applicable | R | No |

Table 69. Z_DELTVEL_LOW Bit Definitions

| Bits | Description |
|--------|--|
| [15:0] | Z-axis delta velocity data; additional resolution bits |

Table 70. Z_DELTVEL_OUT Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x3A, 0x3B | Not applicable | R | No |

Table 71. Z_DELTVEL_OUT Bit Definitions

| Bits | Description |
|--------|--|
| [15:0] | Z-axis delta velocity data; twos complement, ± 400 m/sec range, 0 m/sec = 0x0000; 1 LSB = $400 \text{ m/sec} \div 2^{15} = \sim 0.01221 \text{ m/sec}$ |

The Z_DELTVEL_LOW (see Table 68 and Table 69) and Z_DELTVEL_OUT (see Table 70 and Table 71) registers contain the delta velocity data for the z-axis.

Delta Velocity Resolution

Table 72 and Table 73 offer various numerical examples that demonstrate the format of the delta velocity data in both 16-bit and 32-bit formats.

Table 72. 16-Bit Delta Velocity Data Format Examples

| Velocity (m/sec) | Decimal | Hex | Binary |
|-----------------------------------|---------|--------|---------------------|
| $+400 \times (2^{15} - 1)/2^{15}$ | +32,767 | 0x7FFF | 0111 1111 1111 1111 |
| $+400/2^{14}$ | +2 | 0x0002 | 0000 0000 0000 0010 |
| $+400/2^{15}$ | +1 | 0x0001 | 0000 0000 0000 0001 |
| 0 | 0 | 0x0000 | 0000 0000 0000 0000 |
| $-400/2^{15}$ | -1 | 0xFFFF | 1111 1111 1111 1111 |
| $-400/2^{14}$ | -2 | 0xFFFE | 1111 1111 1111 1110 |
| -400 | -32,768 | 0x8000 | 1000 0000 0000 0000 |

Table 73. 32-Bit Delta Velocity Data Format Examples

| Velocity (m/sec) | Decimal | Hex |
|-----------------------------------|----------------|-------------|
| $+400 \times (2^{31} - 1)/2^{31}$ | +2,147,483,647 | 0x7FFFFFFF |
| $+400/2^{30}$ | +2 | 0x00000002 |
| $+400/2^{31}$ | +1 | 0x00000001 |
| 0 | 0 | 0x00000000 |
| $-400/2^{31}$ | -1 | 0xFFFFFFFF |
| $-400/2^{30}$ | -2 | 0xFFFFFFFFE |
| -400 | +2,147,483,648 | 0x80000000 |

CALIBRATION

The signal chain of each inertial sensor (accelerometers and gyroscopes) includes application of unique correction formulas, which come from extensive characterization of bias, sensitivity, alignment, response to linear acceleration (gyroscopes), and point of percussion (accelerometer location) over a temperature range of -10°C to +75°C, for every ADIS16470. These correction formulas are not accessible, but users do have the opportunity to adjust the bias for each sensor (individually) through user accessible registers. These correction factors follow immediately after the factory derived correction formulas in the signal chain, which processes at a rate of 2000 Hz when using the internal sample clock.

Calibration, Gyroscope Bias (XG_BIAS_LOW and XG_BIAS_HIGH)

Table 74. XG_BIAS_LOW Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|---------|--------|--------------|
| 0x40, 0x41 | 0x0000 | R/W | Yes |

Table 75. XG_BIAS_LOW Bit Definitions

| Bits | Description |
|--------|--|
| [15:0] | X-axis gyroscope offset correction; lower word |

Table 76. XG_BIAS_HIGH Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|---------|--------|--------------|
| 0x42, 0x43 | 0x0000 | R/W | Yes |

Table 77. XG_BIAS_HIGH Bit Definitions

| Bits | Description |
|--------|---|
| [15:0] | X-axis gyroscope offset correction factor, upper word |

The XG_BIAS_LOW (see Table 74 and Table 75) and XG_BIAS_HIGH (see Table 76 and Table 77) registers combine to allow users to adjust the bias of the x-axis gyroscopes. The digital format examples in Table 11 also apply to the XG_BIAS_HIGH register and the digital format examples in Table 12 apply to the 32-bit combination of the XG_BIAS_LOW and XG_BIAS_HIGH registers. See Figure 40 for an illustration of how these two registers combine and influence the x-axis gyroscope measurements.

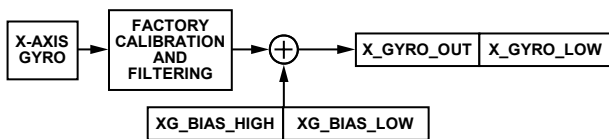


Figure 40. User Calibration Signal Path, Gyroscopes

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Calibration, Gyroscope Bias (YG_BIAS_LOW and YG_BIAS_HIGH)

Table 78. YG_BIAS_LOW Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|---------|--------|--------------|
| 0x44, 0x45 | 0x0000 | R/W | Yes |

Table 79. YG_BIAS_LOW Bit Definitions

| Bits | Description |
|--------|--|
| [15:0] | Y-axis gyroscope offset correction; lower word |

Table 80. YG_BIAS_HIGH Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|---------|--------|--------------|
| 0x46, 0x47 | 0x0000 | R/W | Yes |

Table 81. YG_BIAS_HIGH Bit Definitions

| Bits | Description |
|--------|---|
| [15:0] | Y-axis gyroscope offset correction factor, upper word |

The YG_BIAS_LOW (see Table 78 and Table 79) and YG_BIAS_HIGH (see Table 80 and Table 81) registers combine to allow users to adjust the bias of the y-axis gyroscopes. The digital format examples in Table 11 also apply to the YG_BIAS_HIGH register and the digital format examples in Table 12 apply to the 32-bit combination of the YG_BIAS_LOW and YG_BIAS_HIGH registers. These registers influence the y-axis gyroscope measurements in the same manner that the XG_BIAS_LOW and XG_BIAS_HIGH registers influence the x-axis gyroscope measurements (see Figure 40).

Calibration, Gyroscope Bias (ZG_BIAS_LOW and ZG_BIAS_HIGH)

Table 82. ZG_BIAS_LOW Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|---------|--------|--------------|
| 0x48, 0x49 | 0x0000 | R/W | Yes |

Table 83. ZG_BIAS_LOW Bit Definitions

| Bits | Description |
|--------|--|
| [15:0] | Z-axis gyroscope offset correction; lower word |

Table 84. ZG_BIAS_HIGH Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|---------|--------|--------------|
| 0x4A, 0x4B | 0x0000 | R/W | Yes |

Table 85. ZG_BIAS_HIGH Bit Definitions

| Bits | Description |
|--------|---|
| [15:0] | Z-axis gyroscope offset correction factor, upper word |

The ZG_BIAS_LOW (see Table 82 and Table 83) and ZG_BIAS_HIGH (see Table 84 and Table 85) registers combine to allow users to adjust the bias of the z-axis gyroscopes. The digital format examples in Table 11 also apply to the ZG_BIAS_HIGH register and the digital format examples in Table 12 apply to the 32-bit combination of the ZG_BIAS_LOW and ZG_BIAS_HIGH registers. These registers influence the z-axis gyroscope measurements in the same manner that the XG_BIAS_LOW and XG_BIAS_HIGH registers influence the x-axis gyroscope measurements (see Figure 40).

Calibration, Accelerometer Bias (XA_BIAS_LOW and XA_BIAS_HIGH)

Table 86. XA_BIAS_LOW Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|---------|--------|--------------|
| 0x4C, 0x4D | 0x0000 | R/W | Yes |

Table 87. XA_BIAS_LOW Bit Definitions

| Bits | Description |
|--------|--|
| [15:0] | X-axis accelerometer offset correction; lower word |

Table 88. XA_BIAS_HIGH Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|---------|--------|--------------|
| 0x4E, 0x4F | 0x0000 | R/W | Yes |

Table 89. XA_BIAS_HIGH Bit Definitions

| Bits | Description |
|--------|--|
| [15:0] | X-axis accelerometer offset correction, upper word |

The XA_BIAS_LOW (see Table 86 and Table 87) and XA_BIAS_HIGH (see Table 88 and Table 89) registers combine to allow users to adjust the bias of the x-axis accelerometers. The digital format examples in Table 25 also apply to the XA_BIAS_HIGH register and the digital format examples in Table 26 apply to the 32-bit combination of the XA_BIAS_LOW and XA_BIAS_HIGH registers. See Figure 41 for an illustration of how these two registers combine and influence the x-axis gyroscope measurements.

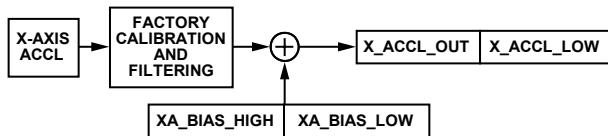


Figure 41. User Calibration Signal Path, Accelerometers

Calibration, Accelerometer Bias (YA_BIAS_LOW and YA_BIAS_HIGH)

Table 90. YA_BIAS_LOW Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|---------|--------|--------------|
| 0x50, 0x51 | 0x0000 | R/W | Yes |

Table 91. YA_BIAS_LOW Bit Definitions

| Bits | Description |
|--------|--|
| [15:0] | Y-axis accelerometer offset correction; lower word |

Table 92. YA_BIAS_HIGH Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|---------|--------|--------------|
| 0x52, 0x53 | 0x0000 | R/W | Yes |

Table 93. YA_BIAS_HIGH Bit Definitions

| Bits | Description |
|--------|--|
| [15:0] | Y-axis accelerometer offset correction, upper word |

The YA_BIAS_LOW (see Table 90 and Table 91) and YA_BIAS_HIGH (see Table 92 and Table 93) registers combine to allow users to adjust the bias of the y-axis accelerometers. The digital format examples in Table 25 also apply to the YA_BIAS_HIGH register, and the digital format examples in Table 26 apply to the 32-bit combination of the YA_BIAS_LOW and YA_BIAS_HIGH registers. These registers influence the y-axis accelerometer measurements in the same manner that the XA_BIAS_LOW and XA_BIAS_HIGH registers influence the x-axis accelerometer measurements (see Figure 41).

Calibration, Accelerometer Bias (ZA_BIAS_LOW and ZA_BIAS_HIGH)

Table 94. ZA_BIAS_LOW Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|---------|--------|--------------|
| 0x54, 0x55 | 0x0000 | R/W | Yes |

Table 95. ZA_BIAS_LOW Bit Definitions

| Bits | Description |
|--------|--|
| [15:0] | Z-axis accelerometer offset correction; lower word |

Table 96. ZA_BIAS_HIGH Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|---------|--------|--------------|
| 0x56, 0x57 | 0x0000 | R/W | Yes |

Table 97. ZA_BIAS_HIGH Bit Definitions

| Bits | Description |
|--------|--|
| [15:0] | Z-axis accelerometer offset correction, upper word |

The ZA_BIAS_LOW (see Table 94 and Table 95) and ZA_BIAS_HIGH (see Table 96 and Table 97) registers combine to allow users to adjust the bias of the z-axis accelerometers. The digital format examples in Table 25 also apply to the ZA_BIAS_HIGH register and the digital format examples in Table 26 apply to the 32-bit combination of the ZA_BIAS_LOW and ZA_BIAS_HIGH registers. These registers influence the z-axis accelerometer measurements in the same manner that the XA_BIAS_LOW and XA_BIAS_HIGH registers influence the x-axis accelerometer measurements (see Figure 41).

Filter Control Register (FILT_CTRL)

Table 98. FILT_CTRL Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|---------|--------|--------------|
| 0x5C, 0x5D | 0x0000 | R/W | Yes |

Table 99. FILT_CTRL Bit Definitions

| Bits | Description |
|--------|---|
| [15:3] | Not used |
| [2:0] | Filter Size Variable B Number of taps in each stage; $N_B = 2^B$ |

The FILT_CTRL register (see Table 98 and Table 99) provides user controls for the Bartlett window FIR filter (see Figure 18), which contains two cascaded averaging filters. For example, use the following sequence to set Register FILT_CTRL, Bits[2:0] = 0100, which sets each stage to have 16 taps: 0xCC04, 0xCD00. Figure 42 provides the frequency response for several settings in the FILT_CTRL register.

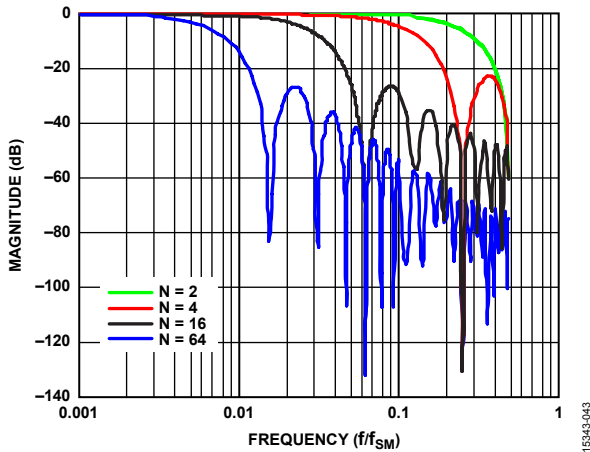


Figure 42. Bartlett Window, FIR Filter Frequency Response (Phase Delay = N Samples)

Miscellaneous Control Register (MSC_CTRL)

Table 100. MSC_CTRL Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|---------|--------|--------------|
| 0x60, 0x61 | 0x00C1 | R/W | Yes |

Table 101. MSC_CTRL Bit Definitions

| Bits | Description |
|--------|--|
| [15:8] | Not used |
| 7 | Linear <i>g</i> compensation for gyroscopes (1 = enabled) |
| 6 | Point of percussion alignment (1 = enabled) |
| 5 | Not used, always set to zero |
| [4:2] | SYNC function setting 111 = reserved (do not use) 110 = reserved (do not use) 101 = pulse sync mode 100 = reserved (do not use) 011 = output sync mode 010 = scaled sync mode 001 = direct sync mode 000 = internal clock mode (default) |
| 1 | SYNC polarity (input or output) 1 = rising edge triggers sampling 0 = falling edge triggers sampling |
| 0 | DR polarity 1 = active high when data is valid 0 = active low when data is valid |

Point of Percussion

Register MSC_CTRL, Bit 6 (see Table 101) offers an on/off control for the point of percussion alignment function, which maps the accelerometer sensors to the corner of the package that is closest to Pin A1 (see Figure 43). The factory default setting in the MSC_CTRL register activates this function. To turn this function off while retaining the rest of the factory default settings in the MSC_CTRL register, set Register MSC_CTRL, Bit 6 = 0, using the following command sequence on the DIN pin: 0xE081, 0xE100.

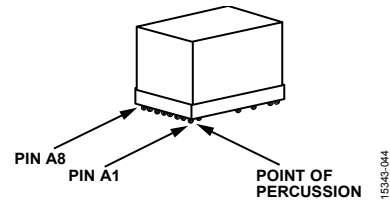


Figure 43. Point of Percussion Reference Point

Linear Acceleration Effect on Gyroscope Bias

Register MSC_CTRL, Bit 7 (see Table 101) provides an on/off control for the linear *g* compensation in the signal calibration routines of the gyroscope. The factory default contents in the MSC_CTRL register enable this compensation. To turn it off, set Register MSC_CTRL, Bit 7 = 0, using the following sequence on the DIN pin: 0xE041, 0xEF00.

Internal Clock Mode

Register MSC_CTRL, Bits[4:2] (see Table 101), provide five different configuration options for controlling the clock (f_{SM} ; see Figure 15 and Figure 16), which controls data acquisition and processing for the inertial sensors. The default setting for Register MSC_CTRL, Bits[4:2] is 000 (binary), which places the ADIS16470 in the internal clock mode. In this mode, an internal clock controls inertial sensor data acquisition and processing at a nominal rate of 2000 Hz. In this mode, each accelerometer data update comes from an average of two data samples (sample rate = 4000 Hz).

Output Sync Mode

When Register MSC_CTRL, Bits[4:2] = 011, the ADIS16470 operates in output sync mode, which is the same as internal clock mode with one exception, the SYNC pin pulses when the internal processor collects data from the inertial sensors. Figure 44 provides an example of this signal.

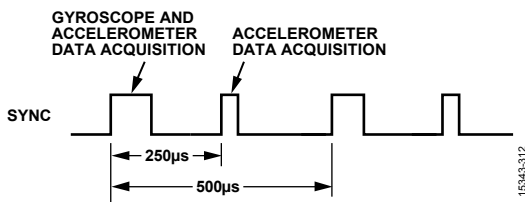


Figure 44. Sync Output Signal, Register MSC_CTRL, Bits[4:2] = 011

Direct Sync Mode

When Register MSC_CTRL, Bits[4:2] = 001, the ADIS16470 operates in direct sync mode; the signal on the SYNC pin directly controls the sample clock. In this mode, the internal processor collects accelerometer data samples on the rising and falling edge of the clock signal and then averages them together to produce each data update. When using this mode, the input clock signal requires a 50% duty cycle.

Pulse Sync Mode

When operating in pulse sync mode (Register MSC_CTRL, Bits[4:2] = 101), the internal processor only collects accelerometers samples on the leading edge of the clock signal, which enables use of a narrow pulse width (see Table 2) in the clock signal on the SYNC pin. Using pulse sync mode also lowers the bandwidth on the inertial sensors to 370 Hz.

Scaled Sync Mode

When Register MSC_CTRL, Bits[4:2] = 010, the ADIS16470 operates in scaled sync mode that supports a frequency range of 1 Hz to 128 Hz for the clock signal on the SYNC pin. This mode of operation is particularly useful when synchronizing the data processing with a PPS signal from a global positioning system (GPS) receiver or with a synchronization signal from a video processing system. When operating in scaled sync mode, the frequency of the sample clock is equal to the product of the external clock scale factor, K_{ESCF} , (from the UP_SCALE register, see Table 102 and Table 103) and the frequency of the clock signal on the SYNC pin.

For example, when using a 1 Hz input signal, set UP_SCALE = 0x07D0 ($K_{ESCF} = 2000$ (decimal)) to establish a sample rate of 2000 SPS for the inertial sensors and their signal processing. Use the following sequence on the DIN pin to configure UP_SCALE for this scenario: 0xE2D0, 0xE307.

Table 102. UP_SCALE Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|---------|--------|--------------|
| 0x62, 0x63 | 0x07D0 | R/W | Yes |

Table 103. UP_SCALE Bit Definitions

| Bits | Description |
|--------|----------------------------|
| [15:0] | K_{ESCF} ; binary format |

Decimation Filter (DEC_RATE)

Table 104. DEC_RATE Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|---------|--------|--------------|
| 0x64, 0x65 | 0x0000 | R/W | Yes |

Table 105. DEC_RATE Bit Definitions

| Bits | Description |
|---------|--|
| [15:11] | Don't care |
| [10:0] | Decimation rate, binary format, maximum = 1999 |

The DEC_RATE register (see Table 104 and Table 105) provides user control for the averaging decimating filter, which averages and decimates the gyroscope and accelerometer data; it also extends the time that the delta angle and the delta velocity track between each update. When the ADIS16470 operates in internal clock mode (see Register MSC_CTRL, Bits [4:2], in Table 101), the nominal output data rate is equal to $2000 / (\text{DEC_RATE} + 1)$. For example, set DEC_RATE = 0x0013 to reduce the output sample rate to 100 SPS ($2000 \div 20$), using the following the DIN pin sequence: 0xE413, 0xE500.

Data Update Rate in External Sync Modes

When using the input sync option, in scaled sync mode (Register MSC_CTRL, Bits[4:2] = 010, see Table 101), the output data rate is equal to $(f_{\text{SYNC}} \times K_{\text{ESCF}}) / (\text{DEC_RATE} + 1)$, where f_{SYNC} represents the frequency of the clock signal on the SYNC pin, and K_{ESCF} represents the value from the UP_SCALE register (see Table 103). When using direct sync mode and pulse sync mode, K_{ESCF} equals 1.

Continuous Bias Estimation (NULL_CNFG)**Table 106. NULL_CNFG Register Definition**

| Addresses | Default | Access | Flash Backup |
|------------|---------|--------|--------------|
| 0x66, 0x67 | 0x070A | R/W | Yes |

Table 107. NULL_CNFG Bit Definitions

| Bits | Description |
|---------|--|
| [15:14] | Not used |
| 13 | Z-axis accelerometer bias correction enable (1 = enabled) |
| 12 | Y-axis accelerometer bias correction enable (1 = enabled) |
| 11 | X-axis accelerometer bias correction enable (1 = enabled) |
| 10 | Z-axis gyroscope bias correction enable (1 = enabled) |
| 9 | Y-axis gyroscope bias correction enable (1 = enabled) |
| 8 | X-axis gyroscope bias correction enable (1 = enabled) |
| [7:4] | Not used |
| [3:0] | Time base control (TBC), range: 0 to 12 (default = 10); $t_B = 2^{TBC}/2000$, time base; $t_A = 64 \times t_B$, average time |

The NULL_CNFG register (see Table 106 and Table 107) provides the configuration controls for the continuous bias estimator (CBE), which associates with the bias correction update command in Register GLOB_CMD, Bit 0 (see Table 109). Register NULL_CNFG, Bits[3:0] establishes the total average time (t_A) for the bias estimates and Register NULL_CNFG, Bits[13:8] provide on/off controls for each sensor. The factory default configuration for the NULL_CNFG register enables the bias null command for the gyroscopes, disables the bias null command for the accelerometers, and sets the average time to ~32 sec.

Global Commands (GLOB_CMD)**Table 108. GLOB_CMD Register Definition**

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x68, 0x69 | Not applicable | W | No |

Table 109. GLOB_CMD Bit Definitions

| Bits | Description |
|--------|-----------------------------|
| [15:8] | Not used |
| 7 | Software reset |
| [6:5] | Not used |
| 4 | Flash memory test |
| 3 | Flash memory update |
| 2 | Sensor self test |
| 1 | Factory calibration restore |
| 0 | Bias correction update |

The GLOB_CMD register (see Table 108 and Table 109) provides trigger bits for several operations. Write a 1 to the appropriate bit in GLOB_CMD to start a particular function. During the execution of these commands, data production stops, pulsing stops on the DR pin, and the SPI interface does not respond to requests. Table 1 provides the execution time for each GLOB_CMD command.

Software Reset

Use the following DIN sequence to set Register GLOB_CMD, Bit 7 = 1, which triggers a reset: 0xE880, 0xE900. This reset clears all data, and then restarts data sampling and processing. This function provides a firmware alternative to toggling the RST pin (see Table 5, Pin F3).

Flash Memory Test

Use the following DIN sequence to set Register GLOB_CMD, Bit 4 = 1, which tests the flash memory: 0xE810, 0xE900. The command performs a CRC computation on the flash memory (excluding user register locations) and compares it with the original CRC value, which comes from the factory configuration process. If the current CRC value does not match the original CRC value, Register DIAG_STAT, Bit 6 (see Table 10) rises to 1, indicating a failing result.

Flash Memory Update

Use the following DIN sequence to set Register GLOB_CMD, Bit 3 = 1, which triggers a back up of all user configurable registers in the flash memory: 0xE808, 0xE900. Register DIAG_STAT, Bit 2 (see Table 10) identifies success (0) or failure (1) in completing this process.

Self Test

Use the following DIN sequence to set Register GLOB_CMD, Bit 2 = 1, which triggers the self test routine for the inertial sensors: 0xE804, 0xE900. The self test routine uses the following steps to validate the integrity of each inertial sensor:

1. Measure the output on each sensor.
2. Activate an internal stimulus on the mechanical elements of each sensor to move them in a predictable manner and create an observable response in the sensors.
3. Measure the output response on each sensor.
4. Deactivate the internal stimulus on each sensor.
5. Calculate the difference between the sensor measurements from Step 1 (stimulus is off) and from Step 4 (stimulus is on).
6. Compare the difference with internal pass and fail criteria.
7. Report the pass and fail result to Register DIAG_STAT, Bit 5 (see Table 10).

Motion, during the execution of this test, can indicate a false failure.

Factory Calibration Restore

Use the following DIN sequence to set Register GLOB_CMD, Bit 1 = 1 to restore the factory default settings for the MSC_CTRL, DEC_RATE, and FILT_CTRL registers and to clear all user configurable bias correction settings: 0xE802, 0xE900. Executing this command results in writing 0x0000 to the following registers: XG_BIAS_LOW, XG_BIAS_HIGH, YG_BIAS_LOW, YG_BIAS_HIGH, ZG_BIAS_LOW, ZG_BIAS_HIGH, XA_BIAS_LOW, XA_BIAS_HIGH, YA_BIAS_LOW, YA_BIAS_HIGH, ZA_BIAS_LOW, and ZA_BIAS_HIGH.

Bias Correction Update

Use the following DIN pin sequence to set Register GLOB_CMD, Bit 0 = 1 to trigger a bias correction, using the correction factors from the CBE (see Table 107): 0xE801, 0xE900.

Firmware Revision (FIRM_REV)**Table 110. FIRM_REV Register Definition**

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x6C, 0x6D | Not applicable | R | Yes |

Table 111. FIRM_REV Bit Definitions

| Bits | Description |
|--------|--|
| [15:0] | Firmware revision, binary coded decimal (BCD) format |

The FIRM_REV register (see Table 110 and Table 111) provides the firmware revision for the internal firmware. This register uses a BCD format, where each nibble represents a digit. For example, if FIRM_REV = 0x0104, the firmware revision is 1.04.

Firmware Revision Day and Month (FIRM_DM)**Table 112. FIRM_DM Register Definition**

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x6E, 0x6F | Not applicable | R | Yes |

Table 113. FIRM_DM Bit Definitions

| Bits | Description |
|--------|---|
| [15:8] | Factory configuration month, BCD format |
| [7:0] | Factory configuration day, BCD format |

The FIRM_DM register (see Table 112 and Table 113) contains the month and day of the factory configuration date. Register FIRM_DM, Bits[15:8] contains digits that represent the month of the factory configuration. For example, November is the 11th month in a year and is represented by Register FIRM_DM, Bits[15:8] = 0x11. Register FIRM_DM, Bits[7:0] contains the day of factory configuration. For example, the 27th day of the month is represented by Register FIRM_DM, Bits[7:0] = 0x27.

Firmware Revision Year (FIRM_Y)**Table 114. FIRM_Y Register Definition**

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x70, 0x71 | Not applicable | R | Yes |

Table 115. FIRM_Y Bit Definitions

| Bits | Description |
|--------|--|
| [15:0] | Factory configuration year, BCD format |

The FIRM_Y register (see Table 114 and Table 115) contains the year of the factory configuration date. For example, the year, 2017, is represented by FIRM_Y = 0x2017.

Product Identification (PROD_ID)**Table 116. PROD_ID Register Definition**

| Addresses | Default | Access | Flash Backup |
|------------|---------|--------|--------------|
| 0x72, 0x73 | 0x4056 | R | No |

Table 117. PROD_ID Bit Definitions

| Bits | Description |
|--------|---------------------------------|
| [15:0] | Product identification = 0x4056 |

The PROD_ID register (see Table 116 and Table 117) contains the numerical portion of the device number (16,470). See Figure 28 for an example of how to use a looping read of this register to validate the integrity of the communication.

Serial Number (SERIAL_NUM)**Table 118. SERIAL_NUM Register Definition**

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x74, 0x75 | Not applicable | R | Yes |

Table 119. SERIAL_NUM Bit Definitions

| Bits | Description |
|--------|----------------------------|
| [15:0] | Lot specific serial number |

Scratch Registers (USER_SCR_1 to USER_SCR_3)**Table 120. USER_SCR_1 Register Definition**

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x76, 0x77 | Not applicable | R/W | Yes |

Table 121. USER_SCR_1 Bit Definitions

| Bits | Description |
|--------|--------------|
| [15:0] | User defined |

Table 122. USER_SCR_2 Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x78, 0x79 | Not applicable | R/W | Yes |

Table 123. USER_SCR_2 Bit Definitions

| Bits | Description |
|--------|--------------|
| [15:0] | User defined |

Table 124. USER_SCR_3 Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x7A, 0x7B | Not applicable | R/W | Yes |

Table 125. USER_SCR_3 Bit Definitions

| Bits | Description |
|--------|--------------|
| [15:0] | User defined |

The USER_SCR_1 (see Table 120 and Table 121), USER_SCR_2 (see Table 122 and Table 123), and USER_SCR_3 (see Table 124 and Table 125) registers provide three locations for users to store information. For nonvolatile storage, use the manual flash memory update command (Register GLOB_CMD, Bit 3, see Table 109), after writing information to these registers.

Flash Memory Endurance Counter (FLSHCNT_LOW and FLSHCNT_HIGH)

Table 126. FLSHCNT_LOW Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x7C, 0x7D | Not applicable | R | Yes |

Table 127. FLSHCNT_LOW Bit Definitions

| Bits | Description |
|--------|--------------------------------------|
| [15:0] | Flash memory write counter, low word |

Table 128. FLSHCNT_HIGH Register Definition

| Addresses | Default | Access | Flash Backup |
|------------|----------------|--------|--------------|
| 0x7E, 0x7F | Not applicable | R | Yes |

Table 129. FLSHCNT_HIGH Bit Definitions

| Bits | Description |
|--------|---------------------------------------|
| [15:0] | Flash memory write counter, high word |

The FLSHCNT_LOW (see Table 126 and Table 127) and FLSHCNT_HIGH (see Table 128 and Table 129) registers combine to provide a 32-bit, binary counter that tracks the number of flash memory write cycles. In addition to the number of write cycles, the flash memory has a finite service lifetime, which depends on the junction temperature. Figure 45 provides guidance for estimating the retention life for the flash memory at specific junction temperatures. The junction temperature is approximately 7°C above the case temperature.

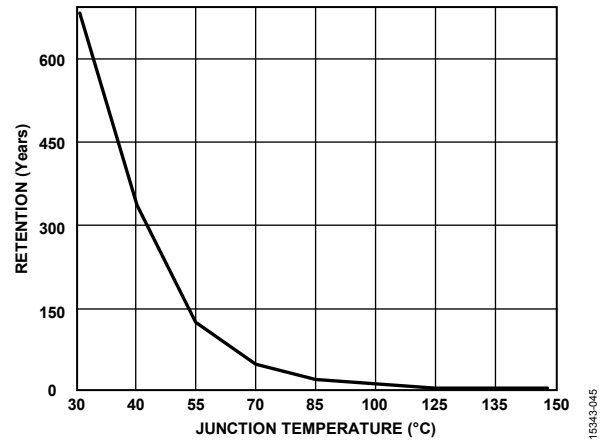


Figure 45. Flash Memory Retention

APPLICATIONS INFORMATION

ASSEMBLY AND HANDLING TIPS

Package Attributes

The ADIS16470 is a multichip module package that has a 44-ball BGA interface. This package has three basic attributes that influence its handling and assembly to the PCB of the system: the lid, the substrate, and the BGA pattern. The material of the lid is a liquid crystal polymer (LCP), and its nominal thickness is 0.5 mm. The substrate is a laminate composition that has a nominal thickness of 1.57 mm. The solder ball material is SAC305, and each ball has a nominal diameter of 0.75 mm (± 0.15 mm). The BGA pattern follows an 8×10 array, with 36 unpopulated positions, which simplifies the escape pattern for the power, ground, and signal traces on the system PCB.

Assembly Tips

When developing a process to attach the ADIS16470 to a PCB, consider the following tips and insights:

- The ADIS16470 packaging has passed numerous qualification tests that have exposed it to solder reflow profiles and are compliant with J-STD-020E, having a peak temperature of 260°C.
- Limit device exposure to one pass through the solder reflow process (no rework).
- The hole in the top of the lid (see Figure 46) provides venting and pressure relief during the assembly process of the ADIS16470. Keep this hole clear of obstruction while attaching the ADIS16470 to a PCB.

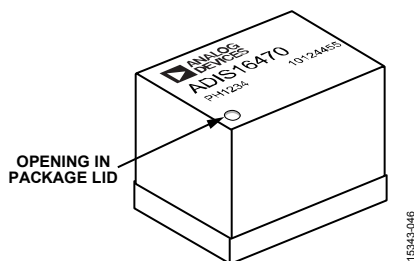


Figure 46. Pressure Relief Hole

- Use no clean flux to avoid exposing the device to cleaning solvents, which can penetrate the inside of the ADIS16470 through the hole in the lid and be difficult to remove. When the assembly process requires the use of liquids that can reach the hole in the lid, use a temporary seal to prevent entrapment of those liquids inside of the cavity.
- Manage moisture exposure prior to the solder reflow processing, in accordance with J-STD-033, MSL5.
- Avoid exposing the ADIS16470 to mechanical shock survivability that exceeds the maximum rating of 2000 g (see Table 3). In standard PCB processing, high speed handling equipment and panel separation processes often present the most risk of introducing harmful levels of mechanical shock survivability.

PCB Layout Suggestions

Figure 47 provides an example of the pad design and layout for the ADIS16470 on a PCB. This example uses a solder mask opening, with a diameter of 0.73 mm, around a metal pad that has a diameter of 0.56 mm. When using a material for the system PCB, which has similar thermal expansion properties as the substrate material of the ADIS16470, the system PCB can also use the solder mask to define the pads that support attachment to the balls of the ADIS16470. The coefficient of thermal expansion (CTE) in the substrate of the ADIS16470 is approximately 14 ppm/°C.

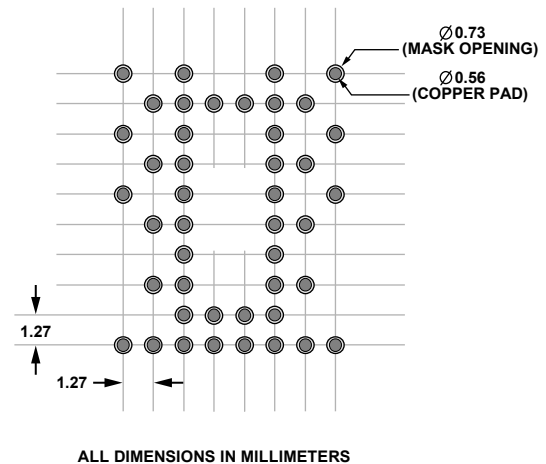


Figure 47. Recommend PCB Pattern, Solder Mask Defined Pads

Underfill

Underfill can be a useful technique in managing certain threats to the integrity of the solder joints of the ADIS16470, including peeling stress and extended exposure to vibration. When selecting underfill material and developing an application and curing process, ensure that the material fills the gap between each surface (ADIS16470 substrate and system PCB) and adheres to both surfaces. The ADIS16470 does not require the use of underfill materials in applications that do not anticipate exposure to these types of mechanical stresses and when the CTE of the system PCB is close to the same value as the CTE of the substrate of the ADIS16470 (~ 14 ppm/°C).

Process Validation and Control

These tips and guidelines provide a starting point for developing a process for attaching the ADIS16470 to a system PCB. Because each system and situation may present unique requirements for this attachment process, ensure that the process supports optimal solder joint integrity, verify that the final system meets all environmental test requirements, and establish observation and control strategies for all key process attributes (peak temperatures, dwell times, ramp rates, and so on).

POWER SUPPLY CONSIDERATIONS

The ADIS16470 contains 6 μF of decoupling capacitance across its VDD and GND pins. When the VDD voltage raises from 0 V to 3.3 V, the charging current for this capacitor bank imposes the following current profile (in amperes):

$$I_{DD}(t) = C \frac{dVDD}{dt} = 6 \times 10^{-6} \times \frac{dVDD(t)}{dt}$$

where:

$I_{DD}(t)$ is the current demand on the VDD pin during the initial power supply ramp, with respect to time.
 C is the internal capacitance across the VDD and GND pins (6 μF).
 $VDD(t)$ is the voltage on the VDD pin, with respect to time.

For example, if VDD follows a linear ramp from 0 V to 3.3 V, in 66 μs, the charging current is 300 mA for that timeframe. The ADIS16470 also contains embedded processing functions that present transient current demands during initialization or reset recovery operations. During these processes, the peak current demand reaches 250 mA and occurs at a time that is approximately 40 ms after VDD reaches 3.0 V (or ~40 ms after initiating a reset sequence).

EVALUATION TOOLS

Breakout Board

The ADIS16470/PCBZ is a breakout board that provides a simple way to develop a prototype connection between the ADIS16470 and an existing embedded processor platform. This breakout board already contains an ADIS16470AMLZ and a dual row, 2 mm pitch, 16-pin header (J1). Table 130 provides the J1 pin assignments, which support direction connection

with an embedded processor board, using standard ribbon cables. As a general guideline, the ADIS16470/PCBZ supports reliable communications over ribbon cables that are up to 20 cm in length. Local electromagnetic interference (EMI) conditions can influence signal integrity, which may require some signal level observation with an oscilloscope, to assure reliable communications.

Table 130. J1 Pin Assignments, Breakout Board

| J1 Pin Number | Signal | Function |
|---------------|--------|--------------|
| 1 | RST | Reset |
| 2 | SCLK | SPI |
| 3 | CS | SPI |
| 4 | DOUT | SPI |
| 5 | NC | Not connect |
| 6 | DIN | SPI |
| 7 | GND | Ground |
| 8 | GND | Ground |
| 9 | GND | Ground |
| 10 | VDD | Power, 3.3 V |
| 11 | VDD | Power, 3.3 V |
| 12 | VDD | Power, 3.3 V |
| 13 | DR | Data ready |
| 14 | SYNC | Input clock |
| 15 | NC | Not connect |
| 16 | NC | Not connect |

Figure 48 provides a top level view of the breakout board, including dimensional locations for all the key mechanical features, such as the mounting holes and the 16-pin header. Figure 49 provides an electrical schematic for this breakout board.

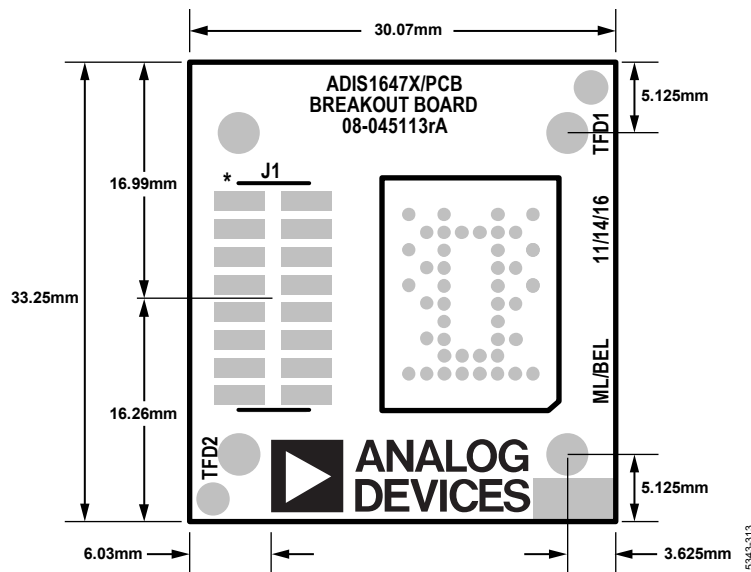


Figure 48. Top Level View of the Breakout Board

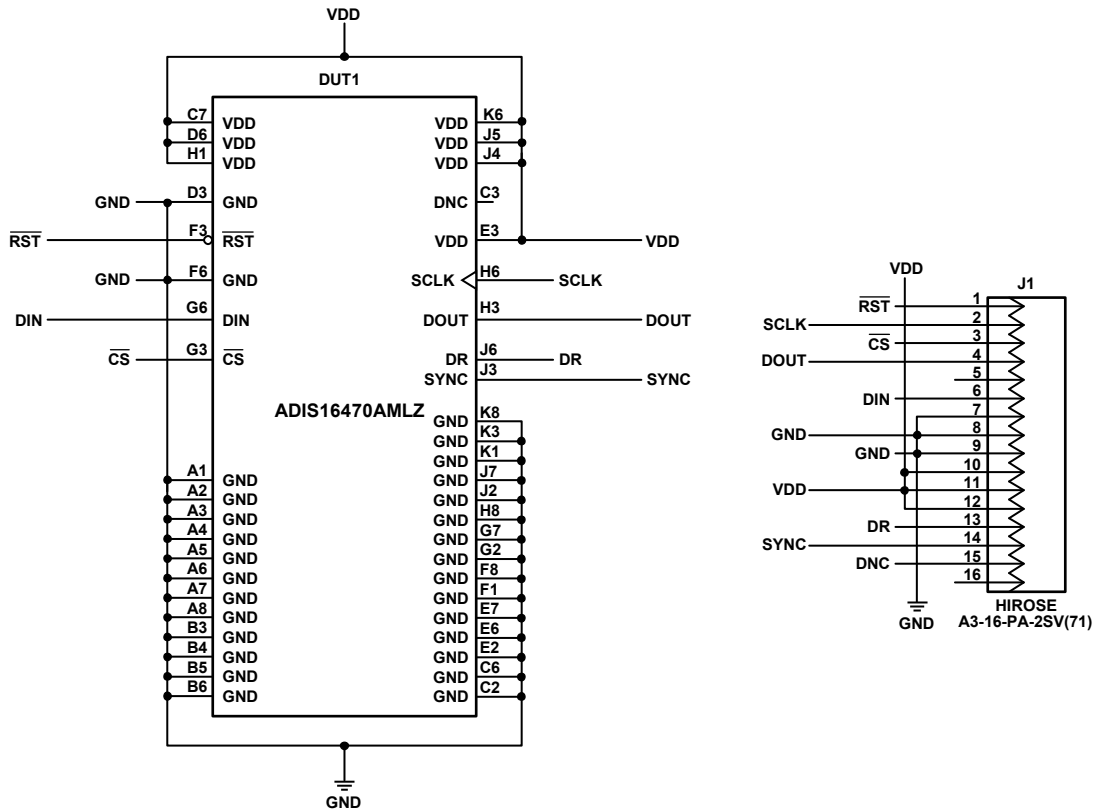


Figure 49. Breakout Board Schematic

PC-Based Evaluation, EVAL-ADIS2

In addition to supporting quick prototype connections between the ADIS16470 and an embedded processing system, J1 on the ADIS16470/PCBZ also connects directly to J1 on the EVAL-

ADIS2 evaluation system. When used in conjunction with the IMU Evaluation Software for the EVAL-ADISX Platforms, the EVAL-ADIS2 provides a simple, functional test platform that provides users with configuration control and the ability to collect data from the output data registers of the ADIS16470.

PACKAGING AND ORDERING INFORMATION
OUTLINE DIMENSIONS

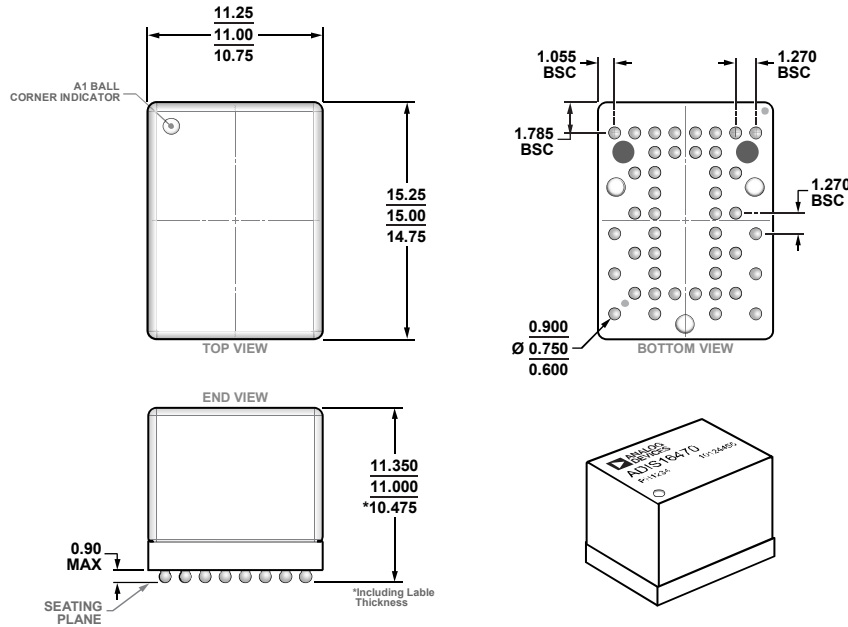


Figure 50. 44-Ball Ball Grid Array Module [BGA]
 (ML-44-1)
 Dimensions shown in millimeters

ORDERING GUIDE

| Model ¹ | Temperature Range | Description | Package Option |
|--------------------|-------------------|--------------------------------------|----------------|
| ADIS16470AMLZ | -25°C to +85°C | 44-Ball Ball Grid Array Module [BGA] | ML-44-1 |
| ADIS16470/PCBZ | | Breakout Board (Evaluation Board) | |

¹ Z = RoHS Compliant Part.