2.1 Ω on resistance, ±15 V/+12 V/±5 V

**iCMOS SPDT Switch ADG1419**

**FEATURES**
- 2.1 Ω on resistance
- 0.5 Ω maximum on resistance flatness at 25°C
- Up to 390 mA continuous current
- Fully specified at +12 V, ±15 V, ±5 V
- No V<sub>L</sub> supply required
- 3 V logic-compatible inputs
- Rail-to-rail operation
- 8-lead MSOP and 8-lead 3 mm × 2 mm LFCSP packages

**APPLICATIONS**
- Automatic test equipment
- Data acquisition systems
- Battery-powered systems
- Relay replacements
- Sample-and-hold systems
- Audio signal routing
- Video signal routing
- Communication systems

**GENERAL DESCRIPTION**

The ADG1419 is a monolithic iCMOS<sup>®</sup> device containing a single-pole/double-throw (SPDT) switch. An EN input on the LFCSP package is used to enable or disable the device. When disabled, all channels are switched off.

The iCMOS (industrial CMOS) modular manufacturing process combines high voltage, complementary metal-oxide semiconductor (CMOS) and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no other generation of high voltage parts has achieved. Unlike analog ICs using conventional CMOS processes, iCMOS components can tolerate high supply voltages while providing increased performance, dramatically lower power consumption, and reduced package size.

The on resistance profile is very flat over the full analog input range ensuring excellent linearity and low distortion when switching audio signals. The iCMOS construction ensures ultralow power dissipation, making the part ideally suited for portable and battery-powered instruments.

Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked. The ADG1419 exhibits break-before-make switching action for use in multiplexer applications.

**PRODUCT HIGHLIGHTS**

1. 2.4 Ω maximum on resistance at 25°C.
2. Minimum distortion.
3. 3 V logic-compatible digital inputs: V<sub>INH</sub> = 2.0 V, V<sub>INL</sub> = 0.8 V.
4. No V<sub>L</sub> logic power supply required.
5. 8-lead MSOP and 8-lead, 3 mm × 2 mm LFCSP packages.
TABLE OF CONTENTS

Features .............................................................................................. 1
Applications ........................................................................................ 1
Functional Block Diagram .............................................................. 1
General Description .......................................................................... 1
Product Highlights ........................................................................... 1
Revision History ................................................................................ 2
Specifications .................................................................................... 3
  ±15 V Dual Supply ........................................................................ 3
  +12 V Single Supply ..................................................................... 4
  ±5 V Dual Supply ......................................................................... 5
  Continuous Current Per Channel, S or D ...................................... 6

Absolute Maximum Ratings ................................................................. 7
  Thermal Resistance ........................................................................ 7
  ESD Caution .................................................................................. 7
  Pin Configuration and Function Descriptions ............................... 8
  Typical Performance Characteristics .......................................... 9
  Test Circuits .................................................................................. 12
  Terminology .................................................................................. 14
  Outline Dimensions ....................................................................... 15
  Ordering Guide ............................................................................. 15

REVISION HISTORY

10/09—Revision 0: Initial Version
SPECIFICATIONS
±15 V DUAL SUPPLY

VDD = +15 V ± 10%, VSS = −15 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter 25°C</th>
<th>−40°C to +85°C</th>
<th>−40°C to +125°C</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANALOG SWITCH</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Analog Signal Range</td>
<td>VDD to VSS</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>On Resistance, RON</td>
<td>2.1</td>
<td>Ω typ</td>
<td>VSS = ±10 V, IS = −10 mA; see Figure 22</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2.4</td>
<td>2.8</td>
<td>3.2</td>
<td>Ω max</td>
<td>VDD = +13.5 V, VSS = −13.5 V</td>
</tr>
<tr>
<td>On Resistance Match Between Channels, ∆RON</td>
<td>0.05</td>
<td>Ω typ</td>
<td>V5 = ±10 V, IS = −10 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.2</td>
<td>0.25</td>
<td>0.3</td>
<td>Ω max</td>
<td></td>
</tr>
<tr>
<td>On Resistance Flatness, RFLAT (ON)</td>
<td>0.4</td>
<td>Ω typ</td>
<td>V5 = ±10 V, IS = −10 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.5</td>
<td>0.6</td>
<td>0.65</td>
<td>Ω max</td>
<td></td>
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<tr>
<td>LEAKAGE CURRENTS</td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Source Off Leakage, IS (Off)</td>
<td>±0.1</td>
<td>nA typ</td>
<td>VDD = +16.5 V, VSS = −16.5 V</td>
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<td></td>
</tr>
<tr>
<td></td>
<td>±0.5</td>
<td>±2</td>
<td>±75</td>
<td>nA max</td>
<td></td>
</tr>
<tr>
<td>Drain Off Leakage, ID (Off)</td>
<td>±0.2</td>
<td>nA typ</td>
<td>V5 = ±10 V, V5 = ±10 V; see Figure 23</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>±0.6</td>
<td>±3</td>
<td>±100</td>
<td>nA max</td>
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</tr>
<tr>
<td>Channel On Leakage, ID, IS (On)</td>
<td>±0.2</td>
<td>nA typ</td>
<td>V5 = VDD = ±10 V; see Figure 24</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>±1</td>
<td>±3</td>
<td>±100</td>
<td>nA max</td>
<td></td>
</tr>
<tr>
<td>DIGITAL INPUTS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input High Voltage, VINH</td>
<td>2.0</td>
<td>V min</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Low Voltage, VINL</td>
<td>0.8</td>
<td>V max</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>Input Current, IINL or IINH</td>
<td>0.005</td>
<td>μA typ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>±0.1</td>
<td>μA max</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Digital Input Capacitance, Cin</td>
<td>4</td>
<td>pF typ</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>DYNAMIC CHARACTERISTICS</td>
<td></td>
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<td></td>
<td></td>
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<tr>
<td>Transition Time, τTRANSITION</td>
<td>130</td>
<td>ns typ</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>155</td>
<td>190</td>
<td>220</td>
<td>ns max</td>
<td></td>
</tr>
<tr>
<td>tON (EN)</td>
<td>85</td>
<td>ns typ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>110</td>
<td>125</td>
<td>140</td>
<td>ns max</td>
<td></td>
</tr>
<tr>
<td>tOFF (EN)</td>
<td>115</td>
<td>ns typ</td>
<td></td>
<td></td>
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</tr>
<tr>
<td></td>
<td>140</td>
<td>160</td>
<td>180</td>
<td>ns max</td>
<td></td>
</tr>
<tr>
<td>Break-Before-Make Time Delay, td</td>
<td>15</td>
<td>ns typ</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Charge Injection</td>
<td>−16</td>
<td>pC typ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Off Isolation</td>
<td>−64</td>
<td>dB typ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Channel-to-Channel Crosstalk</td>
<td>−64</td>
<td>dB typ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total Harmonic Distortion + Noise</td>
<td>0.016</td>
<td>% typ</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>−3 dB Bandwidth</td>
<td>135</td>
<td>MHz typ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Insertion Loss</td>
<td>0.16</td>
<td>dB typ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C0 (Off)</td>
<td>19</td>
<td>pF typ</td>
<td>f = 1 MHz; V5 = 0 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C0 (Off)</td>
<td>44</td>
<td>pF typ</td>
<td>f = 1 MHz; V5 = 0 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C0, C0 (On)</td>
<td>114</td>
<td>pF typ</td>
<td>f = 1 MHz; V5 = 0 V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### POWER REQUIREMENTS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>25°C</th>
<th>−40°C to +85°C</th>
<th>−40°C to +125°C</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{DD} )</td>
<td>0.002</td>
<td>1.0</td>
<td></td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>( I_{DD} ), 8-Lead MSOP</td>
<td>58</td>
<td>95</td>
<td></td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>( I_{DD} ), 8-Lead LFCSP</td>
<td>120</td>
<td>190</td>
<td></td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>( I_{SS} )</td>
<td>0.002</td>
<td>1.0</td>
<td></td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>( V_{DD}/V_{SS} )</td>
<td>±4.5/±16.5</td>
<td>V min/max</td>
<td>Ground = 0 V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\(^1\) Guaranteed by design, not subject to production test.

### +12 V SINGLE SUPPLY

\( V_{DD} = 12 \, V \pm 10\% \), \( V_{SS} = 0 \, V \), GND = 0 V, unless otherwise noted.

### Table 2.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>25°C</th>
<th>−40°C to +85°C</th>
<th>−40°C to +125°C</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANALOG SWITCH</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Analog Signal Range</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>On Resistance, ( R_{ON} )</td>
<td>4</td>
<td>0 V to ( V_{DD} )</td>
<td></td>
<td>Ω</td>
<td>( V_{S} = 0 , V ) to 10 , V, ( I_{S} = -10 , mA ); see Figure 22</td>
</tr>
<tr>
<td>On Resistance Match Between Channels, ( \Delta R_{ON} )</td>
<td>0.08</td>
<td>0.25 0.3 0.35</td>
<td></td>
<td>Ω</td>
<td>( V_{S} = 0 , V ) to 10 , V, ( I_{S} = -10 , mA )</td>
</tr>
<tr>
<td>On Resistance Flatness, ( R_{FLAT (ON)} )</td>
<td>1.2</td>
<td>1.5 1.75 1.9</td>
<td></td>
<td>Ω</td>
<td>( V_{S} = 0 , V ) to 10 , V, ( I_{S} = -10 , mA )</td>
</tr>
<tr>
<td>LEAKAGE CURRENTS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Source Off Leakage, ( I_{S} ) (Off)</td>
<td>±0.1</td>
<td>±0.5 ±2 ±75</td>
<td></td>
<td>nA</td>
<td>( V_{DD} = +13.2 , V, V_{SS} = 0 , V )</td>
</tr>
<tr>
<td>Drain Off Leakage, ( I_{D} ) (Off)</td>
<td>±0.2</td>
<td>±0.6 ±3 ±100</td>
<td></td>
<td>nA</td>
<td>( V_{S} = 1 , V/10 , V, V_{D} = 10 , V/1 , V ); see Figure 23</td>
</tr>
<tr>
<td>Channel On Leakage, ( I_{on}, I_{off} ) (On)</td>
<td>±0.2</td>
<td>±1 ±3 ±100</td>
<td></td>
<td>nA</td>
<td>( V_{S} = V_{D} = 1 , V ) or 10 , V; see Figure 24</td>
</tr>
<tr>
<td>DIGITAL INPUTS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input High Voltage, ( V_{INH} )</td>
<td>2.0</td>
<td>0.8</td>
<td></td>
<td>V min</td>
<td>( V_{IN} = V_{GND} ) or ( V_{DD} )</td>
</tr>
<tr>
<td>Input Low Voltage, ( V_{INL} )</td>
<td></td>
<td></td>
<td></td>
<td>V max</td>
<td>( V_{IN} = V_{GND} ) or ( V_{DD} )</td>
</tr>
<tr>
<td>Input Current, ( I_{INL} ) or ( I_{INH} )</td>
<td>0.005</td>
<td>±0.1</td>
<td></td>
<td>µA max</td>
<td>( V_{IN} = V_{GND} ) or ( V_{DD} )</td>
</tr>
<tr>
<td>DYNAMIC CHARACTERISTICS(^1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Transition Time, ( t_{TRANSITION} )</td>
<td>200</td>
<td>255 265 370</td>
<td></td>
<td>ns</td>
<td>( R_{L} = 300 , \Omega, C_{L} = 35 , pF )</td>
</tr>
<tr>
<td>( t_{ON} ) (EN)</td>
<td>145</td>
<td>190 220 245</td>
<td></td>
<td>ns</td>
<td>( V_{S} = 8 , V ); see Figure 25</td>
</tr>
<tr>
<td>( t_{OFF} ) (EN)</td>
<td>130</td>
<td>170 205 220</td>
<td></td>
<td>ns</td>
<td>( V_{S} = 8 , V ); see Figure 27</td>
</tr>
<tr>
<td>Break-Before-Make Time Delay, ( t_{O} )</td>
<td>55</td>
<td>33</td>
<td></td>
<td>ns</td>
<td>( V_{S1} = V_{S2} = 8 , V ); see Figure 26</td>
</tr>
<tr>
<td>Charge Injection</td>
<td>13</td>
<td>13</td>
<td></td>
<td>pC</td>
<td>( V_{S} = 6 , V, R_{S} = 0 , \Omega, C_{L} = 1 , nF ); see Figure 28</td>
</tr>
<tr>
<td>Off Isolation</td>
<td>−60</td>
<td>−60</td>
<td></td>
<td>dB</td>
<td>( R_{L} = 50 , \Omega, C_{L} = 5 , pF, f = 1 , MHz ); see Figure 29</td>
</tr>
</tbody>
</table>

\(^1\) Guaranteed by design, not subject to production test.
### Channel-to-Channel Crosstalk

-25°C: 

-40°C to +85°C:  

-40°C to +125°C:  

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel-to-Channel Crosstalk</td>
<td>dB</td>
<td>RL = 50 Ω, C1 = 5 pF, f = 1 MHz; see Figure 30</td>
</tr>
</tbody>
</table>

### −3 dB Bandwidth

-25°C: 95 MHz typ  

-40°C to +85°C: 95 MHz typ  

-40°C to +125°C: 95 MHz typ  

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Insertion Loss</td>
<td>pF</td>
<td>RL = 50 Ω, C1 = 5 pF, f = 1 MHz; see Figure 31</td>
</tr>
</tbody>
</table>

### CS (Off)

-25°C: 32 pF typ  

-40°C to +85°C: 32 pF typ  

-40°C to +125°C: 32 pF typ  

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>CD (Off)</td>
<td>pF</td>
<td>RL = 50 Ω, C1 = 5 pF, f = 1 MHz; see Figure 31</td>
</tr>
</tbody>
</table>

### CD, CS (On)

-25°C: 123 pF typ  

-40°C to +85°C: 123 pF typ  

-40°C to +125°C: 123 pF typ  

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Requirements</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Digital Inputs

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Requirements</td>
<td></td>
<td>VDD = 13.2 V</td>
</tr>
</tbody>
</table>

### ±5 V Dual Supply

VDD = +5 V ± 10%, VSS = −5 V ± 10%, GND = 0 V, unless otherwise noted.

### Table 3.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog Signal Range</td>
<td>V</td>
<td>VDD to VSS V</td>
</tr>
</tbody>
</table>

### On Resistance, RON

-25°C: 4.5 Ω typ  

-40°C to +85°C: 5.2 Ω typ  

-40°C to +125°C: 6.2 Ω typ  

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>On Resistance Match Between Channels, ΔRON</td>
<td>Ω typ</td>
<td>V = ±4.5 V, IS = −10 mA; see Figure 22</td>
</tr>
</tbody>
</table>

### On Resistance Flatness, RFLAT (ON)

-25°C: 1.3 Ω typ  

-40°C to +85°C: 0.3 Ω typ  

-40°C to +125°C: 0.35 Ω typ  

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Leakage Currents</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Source Off Leakage, IS (Off)

-25°C: ±0.1 mA typ  

-40°C to +85°C: ±0.5 mA typ  

-40°C to +125°C: ±0.6 mA typ  

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
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</thead>
<tbody>
<tr>
<td>Drain Off Leakage, ID (Off)</td>
<td>mA max</td>
<td>V = ±4.5 V, VD = ±4.5 V; see Figure 23</td>
</tr>
</tbody>
</table>

### Channel On Leakage, IO (On)

-25°C: ±0.1 mA typ  

-40°C to +85°C: ±1 mA typ  

-40°C to +125°C: ±3 mA typ  

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital Inputs</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Input High Voltage, VINH

-25°C: 2.0 V min  

-40°C to +85°C: 0.8 V max  

-40°C to +125°C: 0.8 V max  

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital Input Capacitance, Cin</td>
<td>pF</td>
<td>V = VDD or VSS</td>
</tr>
</tbody>
</table>

1 Guaranteed by design, not subject to production test.
### Dynamic Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>25°C</th>
<th>−40°C to +85°C</th>
<th>−40°C to +125°C</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transition Time, t&lt;sub&gt;TRANSITION&lt;/sub&gt;</td>
<td>310</td>
<td>410 495 560</td>
<td>ns typ</td>
<td>R&lt;sub&gt;L&lt;/sub&gt; = 300 Ω, C&lt;sub&gt;L&lt;/sub&gt; = 35 pF</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;ON&lt;/sub&gt; (EN)</td>
<td>230</td>
<td>305 355 390</td>
<td>ns max</td>
<td>R&lt;sub&gt;L&lt;/sub&gt; = 300 Ω, C&lt;sub&gt;L&lt;/sub&gt; = 35 pF</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;OFF&lt;/sub&gt; (EN)</td>
<td>220</td>
<td>290 335 365</td>
<td>ns max</td>
<td>R&lt;sub&gt;L&lt;/sub&gt; = 300 Ω, C&lt;sub&gt;L&lt;/sub&gt; = 35 pF</td>
<td></td>
</tr>
<tr>
<td>Break-Before-Make Time Delay, t&lt;sub&gt;D&lt;/sub&gt;</td>
<td>65</td>
<td>31</td>
<td>ns min</td>
<td>V&lt;sub&gt;S1&lt;/sub&gt; = V&lt;sub&gt;S2&lt;/sub&gt; = 3 V; see Figure 26</td>
<td></td>
</tr>
<tr>
<td>Charge Injection</td>
<td>59</td>
<td>pC typ</td>
<td></td>
<td>VS = 0 V, R&lt;sub&gt;S&lt;/sub&gt; = 0 Ω, C&lt;sub&gt;L&lt;/sub&gt; = 1 nF; see Figure 28</td>
<td></td>
</tr>
<tr>
<td>Off Isolation</td>
<td>−60</td>
<td>dB typ</td>
<td></td>
<td>R&lt;sub&gt;L&lt;/sub&gt; = 50 Ω, C&lt;sub&gt;L&lt;/sub&gt; = 35 pF; see Figure 29</td>
<td></td>
</tr>
<tr>
<td>Channel-to-Channel Crosstalk</td>
<td>−60</td>
<td>dB typ</td>
<td></td>
<td>R&lt;sub&gt;L&lt;/sub&gt; = 50 Ω, C&lt;sub&gt;L&lt;/sub&gt; = 35 pF; see Figure 30</td>
<td></td>
</tr>
<tr>
<td>Total Harmonic Distortion + Noise</td>
<td>0.04</td>
<td>% typ</td>
<td></td>
<td>R&lt;sub&gt;L&lt;/sub&gt; = 10 kΩ, 5 V p-p, f = 20 Hz to 20 kHz; see Figure 31</td>
<td></td>
</tr>
<tr>
<td>−3 dB Bandwidth</td>
<td>105</td>
<td>MHz typ</td>
<td></td>
<td>R&lt;sub&gt;L&lt;/sub&gt; = 50 Ω, C&lt;sub&gt;L&lt;/sub&gt; = 35 pF; see Figure 31</td>
<td></td>
</tr>
<tr>
<td>Insertion Loss</td>
<td>0.28</td>
<td>dB typ</td>
<td></td>
<td>R&lt;sub&gt;L&lt;/sub&gt; = 50 Ω, C&lt;sub&gt;L&lt;/sub&gt; = 35 pF; see Figure 31</td>
<td></td>
</tr>
<tr>
<td>C&lt;sub&gt;S&lt;/sub&gt; (Off)</td>
<td>26</td>
<td>pF typ</td>
<td></td>
<td>V&lt;sub&gt;S&lt;/sub&gt; = 0 V, f = 1 MHz</td>
<td></td>
</tr>
<tr>
<td>C&lt;sub&gt;D&lt;/sub&gt; (Off)</td>
<td>62</td>
<td>pF typ</td>
<td></td>
<td>V&lt;sub&gt;S&lt;/sub&gt; = 0 V, f = 1 MHz</td>
<td></td>
</tr>
<tr>
<td>C&lt;sub&gt;D&lt;/sub&gt;, C&lt;sub&gt;S&lt;/sub&gt; (On)</td>
<td>128</td>
<td>pF typ</td>
<td></td>
<td>V&lt;sub&gt;S&lt;/sub&gt; = 0 V, f = 1 MHz</td>
<td></td>
</tr>
</tbody>
</table>

### Power Requirements

<table>
<thead>
<tr>
<th>Parameter</th>
<th>25°C</th>
<th>85°C</th>
<th>125°C</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>I&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>0.001</td>
<td></td>
<td></td>
<td>μA typ</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = +5.5 V, V&lt;sub&gt;SS&lt;/sub&gt; = −5.5 V</td>
</tr>
<tr>
<td>I&lt;sub&gt;SS&lt;/sub&gt;</td>
<td>0.001</td>
<td></td>
<td></td>
<td>μA typ</td>
<td>Digital inputs = 0 V or V&lt;sub&gt;DD&lt;/sub&gt;</td>
</tr>
<tr>
<td>V&lt;sub&gt;DD&lt;/sub&gt;/V&lt;sub&gt;SS&lt;/sub&gt;</td>
<td>±4.5/±16.5</td>
<td></td>
<td></td>
<td>μA typ</td>
<td>Digital inputs = 0 V or V&lt;sub&gt;DD&lt;/sub&gt;</td>
</tr>
</tbody>
</table>

1 Guaranteed by design, not subject to production test.

### Continuous Current Per Channel, S or D

#### Table 4.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>25°C</th>
<th>85°C</th>
<th>125°C</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>±15 V Dual Supply</td>
<td></td>
<td></td>
<td></td>
<td>mA maximum</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = +13.5 V, V&lt;sub&gt;SS&lt;/sub&gt; = −13.5 V</td>
</tr>
<tr>
<td>8-Lead MSOP (θ&lt;sub&gt;JA&lt;/sub&gt; = 206°C/W)</td>
<td>215</td>
<td>135</td>
<td>80</td>
<td>mA maximum</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = +10.8 V, V&lt;sub&gt;SS&lt;/sub&gt; = 0 V</td>
</tr>
<tr>
<td>8-Lead LFCSP (θ&lt;sub&gt;JA&lt;/sub&gt; = 50.8°C/W)</td>
<td>390</td>
<td>215</td>
<td>100</td>
<td>mA maximum</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = +4.5 V, V&lt;sub&gt;SS&lt;/sub&gt; = −4.5 V</td>
</tr>
<tr>
<td>±12 V Single Supply</td>
<td></td>
<td></td>
<td></td>
<td>mA maximum</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = +13.5 V, V&lt;sub&gt;SS&lt;/sub&gt; = −13.5 V</td>
</tr>
<tr>
<td>8-Lead MSOP (θ&lt;sub&gt;JA&lt;/sub&gt; = 206°C/W)</td>
<td>175</td>
<td>115</td>
<td>70</td>
<td>mA maximum</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = +10.8 V, V&lt;sub&gt;SS&lt;/sub&gt; = 0 V</td>
</tr>
<tr>
<td>8-Lead LFCSP (θ&lt;sub&gt;JA&lt;/sub&gt; = 50.8°C/W)</td>
<td>320</td>
<td>185</td>
<td>95</td>
<td>mA maximum</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = +4.5 V, V&lt;sub&gt;SS&lt;/sub&gt; = −4.5 V</td>
</tr>
<tr>
<td>±5 V Dual Supply</td>
<td></td>
<td></td>
<td></td>
<td>mA maximum</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = +13.5 V, V&lt;sub&gt;SS&lt;/sub&gt; = −13.5 V</td>
</tr>
<tr>
<td>8-Lead MSOP (θ&lt;sub&gt;JA&lt;/sub&gt; = 206°C/W)</td>
<td>165</td>
<td>110</td>
<td>70</td>
<td>mA maximum</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = +10.8 V, V&lt;sub&gt;SS&lt;/sub&gt; = 0 V</td>
</tr>
<tr>
<td>8-Lead LFCSP (θ&lt;sub&gt;JA&lt;/sub&gt; = 50.8°C/W)</td>
<td>310</td>
<td>180</td>
<td>95</td>
<td>mA maximum</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = +4.5 V, V&lt;sub&gt;SS&lt;/sub&gt; = −4.5 V</td>
</tr>
</tbody>
</table>

1 Guaranteed by design, not subject to production test.
ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$ to $V_{SS}$</td>
<td>35 V</td>
</tr>
<tr>
<td>$V_{DD}$ to GND</td>
<td>$-0.3 \text{ V to } +25 \text{ V}$</td>
</tr>
<tr>
<td>$V_{SS}$ to GND</td>
<td>$+0.3 \text{ V to } -25 \text{ V}$</td>
</tr>
<tr>
<td>Analog Inputs$^1$</td>
<td>$V_{SS} - 0.3 \text{ V to } V_{DD} + 0.3 \text{ V or } 30 \text{ mA, whichever occurs first}$</td>
</tr>
<tr>
<td>Digital Inputs$^1$</td>
<td>$GND - 0.3 \text{ V to } V_{DD} + 0.3 \text{ V or } 30 \text{ mA, whichever occurs first}$</td>
</tr>
<tr>
<td>Peak Current, S or D (Pulsed at 1 ms, 10% Duty-Cycle Maximum)</td>
<td>400 mA</td>
</tr>
<tr>
<td>8-Lead MSOP (4-Layer Board)</td>
<td>600 mA</td>
</tr>
<tr>
<td>8-Lead LFCSF</td>
<td></td>
</tr>
<tr>
<td>Continuous Current per Channel, S or D</td>
<td>Data in Table 4 + 15% mA</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td></td>
</tr>
<tr>
<td>Industrial</td>
<td>$-40^\circ\text{C to } +125^\circ\text{C}$</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>$-65^\circ\text{C to } +150^\circ\text{C}$</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>150$^\circ\text{C}$</td>
</tr>
<tr>
<td>Reflow Soldering Peak Temperature, Pb Free</td>
<td>260$^\circ\text{C}$</td>
</tr>
</tbody>
</table>

$^1$ Over voltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

<table>
<thead>
<tr>
<th>Package Type</th>
<th>$\theta JA$</th>
<th>$\theta JC$</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>8-Lead MSOP (4-Layer Board)</td>
<td>206</td>
<td>44</td>
<td>°C/W</td>
</tr>
<tr>
<td>8-Lead LFCSF</td>
<td>50.8</td>
<td></td>
<td>°C/W</td>
</tr>
</tbody>
</table>

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.
PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 7. 8-Lead LFCSP Pin Function Descriptions

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>D</td>
<td>Drain Terminal. This pin can be an input or output.</td>
</tr>
<tr>
<td>2</td>
<td>SA</td>
<td>Source Terminal. This pin can be an input or output.</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>Ground (0 V) Reference.</td>
</tr>
<tr>
<td>4</td>
<td>VDD</td>
<td>Most Positive Power Supply Potential.</td>
</tr>
<tr>
<td>5</td>
<td>EN</td>
<td>Active High Digital Input. When this pin is low, the device is disabled and all switches are turned off. When this pin is high, the IN logic input determines which switch is turned on.</td>
</tr>
<tr>
<td>6</td>
<td>IN</td>
<td>Logic Control Input.</td>
</tr>
<tr>
<td>7</td>
<td>VSS</td>
<td>Most Negative Power Supply Potential.</td>
</tr>
<tr>
<td>8</td>
<td>SB</td>
<td>Source Terminal. This pin can be an input or output.</td>
</tr>
<tr>
<td></td>
<td>EPAD</td>
<td>Exposed pad tied to substrate, VSS.</td>
</tr>
</tbody>
</table>

Table 8. 8-Lead LFCSP Truth Table

<table>
<thead>
<tr>
<th>EN</th>
<th>IN</th>
<th>Switch A</th>
<th>Switch B</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>On</td>
<td>Off</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Off</td>
<td>On</td>
</tr>
</tbody>
</table>

Table 9. 8-Lead MSOP Pin Function Descriptions

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>D</td>
<td>Drain Terminal. This pin can be an input or output.</td>
</tr>
<tr>
<td>2</td>
<td>SA</td>
<td>Source Terminal. This pin can be an input or output.</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>Ground (0 V) Reference.</td>
</tr>
<tr>
<td>4</td>
<td>VDD</td>
<td>Most Positive Power Supply Potential.</td>
</tr>
<tr>
<td>5</td>
<td>NC</td>
<td>No Connect.</td>
</tr>
<tr>
<td>6</td>
<td>IN</td>
<td>Logic Control Input.</td>
</tr>
<tr>
<td>7</td>
<td>VSS</td>
<td>Most Negative Power Supply Potential.</td>
</tr>
<tr>
<td>8</td>
<td>SB</td>
<td>Source Terminal. This pin can be an input or output.</td>
</tr>
</tbody>
</table>

Table 10. 8-Lead MSOP Truth Table

<table>
<thead>
<tr>
<th>IN</th>
<th>Switch A</th>
<th>Switch B</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>On</td>
<td>Off</td>
</tr>
<tr>
<td>1</td>
<td>Off</td>
<td>On</td>
</tr>
</tbody>
</table>
TYPICAL PERFORMANCE CHARACTERISTICS

Figure 5. On Resistance as a Function of $V_D$ ($V_S$) for Dual Supply

Figure 6. On Resistance as a Function of $V_D$ ($V_S$) for Single Supply

Figure 7. On Resistance as a Function of $V_D$ ($V_S$) for Dual Supply

Figure 8. On Resistance as a Function of $V_D$ ($V_S$) for Different Temperatures, ±15 V Dual Supply

Figure 9. On Resistance as a Function of $V_D$ ($V_S$) for Different Temperatures, ±12 V Single Supply

Figure 10. On Resistance as a Function of $V_D$ ($V_S$) for Different Temperatures, ±5 V Dual Supply
Figure 11. Leakage Currents as a Function of Temperature, ±15 V Dual Supply

Figure 12. Leakage Currents as a Function of Temperature, +12 V Single Supply

Figure 13. Leakage Currents as a Function of Temperature, ±5 V Dual Supply

Figure 14. IDD vs. Logic Level

Figure 15. Charge Injection vs. Source Voltage

Figure 16. ttrsp Times vs. Temperature
Figure 17. Off Isolation vs. Frequency

Figure 18. Crosstalk vs. Frequency

Figure 19. On Response vs. Frequency

Figure 20. THD + N vs. Frequency

Figure 21. ACPSRR vs. Frequency
TEST CIRCUITS

Figure 22. On Resistance

Figure 23. Off Leakage

Figure 25. Switching Times, $t_{\text{ON}}$ and $t_{\text{OFF}}$

Figure 26. Break-Before-Make Time Delay

Figure 27. Enable Delay, $t_{\text{ON (EN)}}$, $t_{\text{OFF (EN)}}$
VIN (NORMALLY CLOSED SWITCH)

VOUT

VIN (NORMALLY OPEN SWITCH)

OFF

Δ

VOUT

ON

QINJ = CL × ΔVOUT

Figure 28. Charge Injection

Figure 29. Off Isolation

Figure 30. Channel-to-Channel Crosstalk

Figure 31. Bandwidth

Figure 32. THD + N
TERMINOLOGY

**I\text{DD}**
The positive supply current.

**I\text{SS}**
The negative supply current.

**V_D (V_S)**
The analog voltage on Terminal D and Terminal S.

**RON**
The ohmic resistance between Terminal D and Terminal S.

**RFLAT (ON)**
Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

**I_S (Off)**
The source leakage current with the switch off.

**I_D (Off)**
The drain leakage current with the switch off.

**I_D, I_S (On)**
The channel leakage current with the switch on.

**V_{INL}**
The maximum input voltage for Logic 0.

**V_{INH}**
The minimum input voltage for Logic 1.

**I_{INL} (I_{INH})**
The input current of the digital input.

**C_S (Off)**
The off switch source capacitance, measured with reference to ground.

**C_D (Off)**
The off switch drain capacitance, measured with reference to ground.

**C_{ON}, C_S (On)**
The on switch capacitance, measured with reference to ground.

**C_{IN}**
The digital input capacitance.

**t_{ON} (EN)**
Delay time between the 50% and 90% points of the digital input and switch on condition. See Figure 27.

**t_{OFF} (EN)**
Delay time between the 50% and 90% points of the digital input and switch off condition. See Figure 27.

**t_{TRANSITION}**
Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

**t_{BBM}**
Off time measured between the 80% point of both switches when switching from one address state to another. See Figure 26.

**Charge Injection**
A measure of the glitch impulse transferred from the digital input to the analog output during switching. See Figure 28.

**Off Isolation**
A measure of unwanted signal coupling through an off switch. See Figure 29.

**Crossstalk**
A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance. See Figure 30.

**Bandwidth**
The frequency at which the output is attenuated by 3 dB. See Figure 31.

**On Response**
The frequency response of the on switch.

**Insertion Loss**
The loss due to the on resistance of the switch. See Figure 31.

**THD + N**
The ratio of the harmonic amplitude plus noise of the signal to the fundamental. See Figure 32.

**AC Power Supply Rejection Ratio (ACPSRR)**
ACPSRR measures the ability of a part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of signal on the output to the amplitude of the modulation is the ACPSRR. See Figure 21.
OUTLINE DIMENSIONS

Figure 33. 8-Lead Mini Small Outline Package [MSOP] (RM-8)
Dimensions shown in millimeters

Figure 34. 8-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 2 mm Body, Very Very Thin, Dual Lead (CP-8-4)
Dimensions shown in millimeters

ORDERING GUIDE

<table>
<thead>
<tr>
<th>Model</th>
<th>Temperature Range</th>
<th>Package Description</th>
<th>Package Option</th>
<th>Branding</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADG1419BRMZ1</td>
<td>−40°C to +125°C</td>
<td>8-Lead Mini Small Outline Package [MSOP]</td>
<td>RM-8</td>
<td>S1L</td>
</tr>
<tr>
<td>ADG1419BRMZ-REEL71</td>
<td>−40°C to +125°C</td>
<td>8-Lead Mini Small Outline Package [MSOP]</td>
<td>RM-8</td>
<td>S1L</td>
</tr>
<tr>
<td>ADG1419BCPZ-REEL71</td>
<td>−40°C to +125°C</td>
<td>8-Lead Lead Frame Chip Scale Package [LFCSP_WD]</td>
<td>CP-8-4</td>
<td>1C</td>
</tr>
</tbody>
</table>

1 Z = RoHS Compliant Part.