FEATURES
8.0 GHz bandwidth
3.2 V to 3.6 V power supply
Separate charge pump supply (VP) allows extended tuning voltage in 3.3 V systems
Programmable, dual-modulus prescaler
8/9, 16/17, 32/33, or 64/65
Programmable charge pump currents
Programmable antibacklash pulse width
3-wire serial interface
Analog and digital lock detect
Hardware and software power-down mode
Loop filter design possible with ADIsimPLL
4 mm × 4 mm, 20-lead chip scale package

APPLICATIONS
Broadband wireless access
Satellite systems
Instrumentation
Wireless LANs
Base stations for wireless radio

GENERAL DESCRIPTION
The ADF4108 frequency synthesizer can be used to implement local oscillators in the upconversion and downconversion sections of wireless receivers and transmitters. It consists of a low noise digital PFD (phase frequency detector), a precision charge pump, a programmable reference divider, programmable A and B counters, and a dual-modulus prescaler (P/P + 1). The A (6-bit) and B (13-bit) counters, in conjunction with the dual-modulus prescaler (P/P + 1), implement an N divider (N = BP + A). In addition, the 14-bit reference counter (R counter), allows selectable REFIN frequencies at the PFD input. A complete phase-locked loop (PLL) can be implemented if the synthesizer is used with an external loop filter and voltage controlled oscillator (VCO). Its very high bandwidth means that frequency doublers can be eliminated in many high frequency systems, simplifying system architecture and reducing cost.

FUNCTIONAL BLOCK DIAGRAM

Figure 1.
ADF4108* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS
View a parametric search of comparable parts.

EVALUATION KITS
• ADF4108 Evaluation Board

DOCUMENTATION
Application Notes
• AN-30: Ask the Applications Engineer - PLL Synthesizers
• AN-349: Keys to Longer Life for CMOS
• AN-873: Lock Detect on the ADF4xxx Family of PLL Synthesizers

Data Sheet
• ADF4108: PLL Frequency Synthesizer Data Sheet

User Guides
• UG-160: Evaluation Board for Integer-N PLL Frequency Synthesizer
• UG-476: PLL Software Installation Guide

TOOLS AND SIMULATIONS
• ADIsimPLL™
• ADIsimRF

REFERENCE MATERIALS
Product Selection Guide
• RF Source Booklet

DESIGN RESOURCES
• ADF4108 Material Declaration
• PCN-PDN Information
• Quality And Reliability
• Symbols and Footprints

DISCUSSIONS
View all ADF4108 EngineerZone Discussions.

SAMPLE AND BUY
Visit the product page to see pricing options.

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# ADF4108 Data Sheet

## TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Features</td>
<td>1</td>
</tr>
<tr>
<td>Applications</td>
<td>1</td>
</tr>
<tr>
<td>General Description</td>
<td>1</td>
</tr>
<tr>
<td>Functional Block Diagram</td>
<td>1</td>
</tr>
<tr>
<td>Revision History</td>
<td>2</td>
</tr>
<tr>
<td>Specifications</td>
<td>3</td>
</tr>
<tr>
<td>Timing Characteristics</td>
<td>5</td>
</tr>
<tr>
<td>Absolute Maximum Ratings</td>
<td>6</td>
</tr>
<tr>
<td>ESD Caution</td>
<td>6</td>
</tr>
<tr>
<td>Pin Configuration and Function Descriptions</td>
<td>7</td>
</tr>
<tr>
<td>Typical Performance Characteristics</td>
<td>8</td>
</tr>
<tr>
<td>Theory of Operation</td>
<td>9</td>
</tr>
<tr>
<td>Reference Input Stage</td>
<td>9</td>
</tr>
<tr>
<td>RF Input Stage</td>
<td>9</td>
</tr>
<tr>
<td>Prescaler (P/P + 1)</td>
<td>9</td>
</tr>
<tr>
<td>A and B Counters</td>
<td>9</td>
</tr>
<tr>
<td>R Counter</td>
<td>9</td>
</tr>
<tr>
<td>Phase Frequency Detector and Charge Pump</td>
<td>10</td>
</tr>
<tr>
<td>MUXOUT and Lock Detect</td>
<td>10</td>
</tr>
<tr>
<td>Input Shift Register</td>
<td>10</td>
</tr>
<tr>
<td>Latch Summary</td>
<td>11</td>
</tr>
<tr>
<td>Reference Counter Latch Map</td>
<td>12</td>
</tr>
<tr>
<td>AB Counter Latch Map</td>
<td>13</td>
</tr>
<tr>
<td>Function Latch Map</td>
<td>14</td>
</tr>
<tr>
<td>Initialization Latch Map</td>
<td>15</td>
</tr>
<tr>
<td>Function Latch</td>
<td>16</td>
</tr>
<tr>
<td>Initialization Latch Map</td>
<td>17</td>
</tr>
<tr>
<td>Power Supply Considerations</td>
<td>17</td>
</tr>
<tr>
<td>Interfacing</td>
<td>18</td>
</tr>
<tr>
<td>ADuC812 Interface</td>
<td>18</td>
</tr>
<tr>
<td>ADSP-21xx Interface</td>
<td>18</td>
</tr>
<tr>
<td>PCB Design Guidelines for Chip Scale Package</td>
<td>19</td>
</tr>
<tr>
<td>Outline Dimensions</td>
<td>20</td>
</tr>
<tr>
<td>Ordering Guide</td>
<td>20</td>
</tr>
</tbody>
</table>

## REVISION HISTORY

**4/13—Rev. D to Rev. E**
- Changed RFinA to RFinB Parameter from ±320 mV to ±600 mV, Table 3...6

**1/13—Rev. C to Rev. D**
- Change to Table 1...4
- Added RFinA to RFinB Parameter, Table 4...6

**7/12—Rev. B to Rev. C**
- Changes to Figure 3...7
- Updated Outline Dimensions (Changed CP-20-1 to CP-20-6)...20
- Changes to Ordering Guide...20

**9/11—Rev. A to Rev. B**
- Changes to Normalized Phase Noise Floor (PNSYNTH) Parameter and Endnote 9, Table 1...4
- Added Normalized 1/f Noise (PN1_f) Parameter and Endnote 10, Table 1...4
- Changes to Figure 3 and Table 4...7
- Updated Outline Dimensions...20

**12/07—Rev. 0 to Rev. A**
- Removed TSSOP Package... Universal
- Changes to Features...1
- Changes to Table 1 Endnote 10 and Endnote 11...4
- Changes to Table 3...6
- Deleted Figure 3...7
- Changes to Table 4...7
- Changes to Figure 10 and Figure 11...8
- Updated Outline Dimensions...20
- Deleted Figure 24...20
- Changes to Ordering Guide...20

**4/06—Revision 0: Initial Version**

Rev. E | Page 2 of 20
**SPECIFICATIONS**

$AV_{DD} = DV_{DD} = 3.3\ V \pm 2\%$, $AV_{DD} \leq V_P \leq 5.5\ V$, $AGND = DGND = CP_{GND} = 0\ V$, $R_{SET} = 5.1\ k\Omega$, $dBm$ referred to $50\ \Omega$, $T_A = T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 1.**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>B Version$^1$</th>
<th>B Chips$^2$ (Typ)</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>RF CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RF Input Frequency ($RF_{IN}$)</td>
<td>1.0/8.0</td>
<td>1.0/8.0</td>
<td>GHz min/max</td>
<td>See Figure 11 for input circuit</td>
</tr>
<tr>
<td>RF Input Sensitivity</td>
<td>$-5/+5$</td>
<td>$-5/+5$</td>
<td>dBm min/max</td>
<td>For lower frequencies, ensure slew rate (SR) $&gt; 320\ V/\mu s$</td>
</tr>
<tr>
<td>Maximum Allowable Prescaler Output Frequency$^3$</td>
<td>300</td>
<td>300</td>
<td>MHz max</td>
<td>$P = 8$</td>
</tr>
<tr>
<td></td>
<td>325</td>
<td>325</td>
<td>MHz max</td>
<td>$P = 16$</td>
</tr>
<tr>
<td><strong>REFIN CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>REFIN Input Frequency</td>
<td>20/250</td>
<td>20/250</td>
<td>MHz min/max</td>
<td>For $f &lt; 20\ MHz$, ensure SR $&gt; 50\ V/\mu s$</td>
</tr>
<tr>
<td>REFIN Input Sensitivity$^4$</td>
<td>0.8/$V_{DD}$</td>
<td>0.8/$V_{DD}$</td>
<td>V p-p min/max</td>
<td>Biased at $AV_{DD}/2$ (^2)</td>
</tr>
<tr>
<td>REFIN Input Capacitance</td>
<td>10</td>
<td>10</td>
<td>pF max</td>
<td></td>
</tr>
<tr>
<td>REFIN Input Current</td>
<td>$\pm 100$</td>
<td>$\pm 100$</td>
<td>$\mu A$ max</td>
<td></td>
</tr>
<tr>
<td><strong>PHASE DETECTOR</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Phase Detector Frequency$^6$</td>
<td>104</td>
<td>104</td>
<td>MHz max</td>
<td>Programmable; see Figure 18</td>
</tr>
<tr>
<td><strong>CHARGE PUMP</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I$_{CP}$ Sink/Source</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High Value</td>
<td>5</td>
<td>5</td>
<td>$mA$ typ</td>
<td>With $R_{SET} = 5.1\ k\Omega$</td>
</tr>
<tr>
<td>Low Value</td>
<td>625</td>
<td>625</td>
<td>$\mu A$ typ</td>
<td></td>
</tr>
<tr>
<td>Absolute Accuracy</td>
<td>2.5</td>
<td>2.5</td>
<td>% typ</td>
<td>With $R_{SET} = 5.1\ k\Omega$</td>
</tr>
<tr>
<td>$R_{SET}$ Range</td>
<td>3.0/11</td>
<td>3.0/11</td>
<td>k$\Omega$ typ</td>
<td>See Figure 18</td>
</tr>
<tr>
<td>I$_{CP}$ Three-State Leakage</td>
<td>1</td>
<td>1</td>
<td>n$A$ typ</td>
<td>1 n$A$ typical; $T_A = 25^\circ C$</td>
</tr>
<tr>
<td>Sink and Source Current Matching</td>
<td>2</td>
<td>2</td>
<td>% typ</td>
<td>$0.5\ V \leq V_{CP} \leq V_P - 0.5\ V$</td>
</tr>
<tr>
<td>I$<em>{CP}$ vs. $V</em>{CP}$</td>
<td>1.5</td>
<td>1.5</td>
<td>% typ</td>
<td>$0.5\ V \leq V_{CP} \leq V_P - 0.5\ V$</td>
</tr>
<tr>
<td>I$_{CP}$ vs. Temperature</td>
<td>2</td>
<td>2</td>
<td>% typ</td>
<td>$V_{CP} = 0V/2$</td>
</tr>
<tr>
<td><strong>LOGIC INPUTS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IH}$, Input High Voltage</td>
<td>1.4</td>
<td>1.4</td>
<td>$V$ min</td>
<td></td>
</tr>
<tr>
<td>$V_{IL}$, Input Low Voltage</td>
<td>0.6</td>
<td>0.6</td>
<td>$V$ max</td>
<td></td>
</tr>
<tr>
<td>$I_{NH}, I_{NL}$, Input Current</td>
<td>$\pm 1$</td>
<td>$\pm 1$</td>
<td>$\mu A$ max</td>
<td></td>
</tr>
<tr>
<td>$C_{IN}$, Input Capacitance</td>
<td>10</td>
<td>10</td>
<td>pF max</td>
<td></td>
</tr>
<tr>
<td><strong>LOGIC OUTPUTS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OH}$, Output High Voltage</td>
<td>1.4</td>
<td>1.4</td>
<td>$V$ min</td>
<td>Open-drain output chosen; 1 k$\Omega$ pull-up resistor to 1.8 $V$</td>
</tr>
<tr>
<td>$V_{OH}$, Output High Voltage</td>
<td>$V_{DD} - 0.4$</td>
<td>$V_{DD} - 0.4$</td>
<td>$V$ min</td>
<td>CMOS output chosen</td>
</tr>
<tr>
<td>$I_{OH}$, Output High Current</td>
<td>100</td>
<td>100</td>
<td>$\mu A$ max</td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$, Output Low Voltage</td>
<td>0.4</td>
<td>0.4</td>
<td>$V$ max</td>
<td>$I_{OL} = 500\ \mu A$</td>
</tr>
<tr>
<td><strong>POWER SUPPLIES</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$AV_{DD}$</td>
<td>3.2/3.6</td>
<td>3.2/3.6</td>
<td>$V$ min/max</td>
<td></td>
</tr>
<tr>
<td>$DV_{DD}$</td>
<td>$AV_{DD}$</td>
<td>$AV_{DD}$</td>
<td>$V$ min/max</td>
<td></td>
</tr>
<tr>
<td>$V_P$</td>
<td>$AV_{DD}/5.5$</td>
<td>$AV_{DD}/5.5$</td>
<td>$V$ min/max</td>
<td>$AV_{DD} \leq V_P \leq 5.5\ V$</td>
</tr>
<tr>
<td>$I_{D} (A_{D0} + D_{D0})$$^7$</td>
<td>17</td>
<td>17</td>
<td>$mA$ max</td>
<td>15 mA typ</td>
</tr>
<tr>
<td>$I_P$</td>
<td>0.4</td>
<td>0.4</td>
<td>$mA$ max</td>
<td>$T_A = 25^\circ C$</td>
</tr>
<tr>
<td>Power-Down Mode ($A_{D0} + D_{D0}$)$^8$</td>
<td>10</td>
<td>10</td>
<td>$\mu A$ typ</td>
<td></td>
</tr>
<tr>
<td>Parameter</td>
<td>B Version</td>
<td>B Chips(^2) (Typ)</td>
<td>Unit</td>
<td>Test Conditions/Comments</td>
</tr>
<tr>
<td>-----------------------------------</td>
<td>-----------</td>
<td>---------------------</td>
<td>------------</td>
<td>--------------------------</td>
</tr>
<tr>
<td><strong>NOISE CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Normalized Phase Noise Floor</td>
<td>−223</td>
<td>−223</td>
<td>dBc/Hz typ</td>
<td>PLL loop B/W = 500 kHz, measured at 100 kHz offset</td>
</tr>
<tr>
<td>(PNSYNTH)(^9)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Normalized 1/f Noise (PN(_{1/f}))(^10)</td>
<td>−122</td>
<td>−122</td>
<td>dBc/Hz typ</td>
<td>10 kHz offset; normalized to 1 GHz</td>
</tr>
<tr>
<td>Phase Noise Performance(^11)</td>
<td>−81</td>
<td>−81</td>
<td>dBc/Hz typ</td>
<td>@ VCO output</td>
</tr>
<tr>
<td>7900 MHz Output(^12)</td>
<td>−82</td>
<td>−82</td>
<td>dBc typ</td>
<td>@ 1 kHz offset and 1 MHz PFD frequency</td>
</tr>
<tr>
<td>Spurious Signals</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7900 MHz Output(^12)</td>
<td>−82</td>
<td>−82</td>
<td>dBc typ</td>
<td></td>
</tr>
</tbody>
</table>

\(^1\) Operating temperature range (B version) is −40°C to +85°C.

\(^2\) The B chip specifications are given as typical values.

\(^3\) This is the maximum operating frequency of the CMOS counters. The prescaler value should be chosen to ensure that the RF input is divided down to a frequency that is less than this value.

\(^4\) AVDD = DVDD = 3.3 V.

\(^5\) AC coupling ensures AVDD/2 bias.

\(^6\) Guaranteed by design. Sample tested to ensure compliance.

\(^7\) \(T_A = 25^\circ C; AVDD = DVDD = 3.3 V; P = 32; RF\text{in} = 8 \text{GHz}, f_{\text{PFD}} = 200 \text{ kHz}, \text{REF}_{\text{in}} = 10 \text{ MHz}.

\(^8\) \(T_A = 25^\circ C; AVDD = DVDD = 3.3 V; R = 16,383; A = 63; B = 891; f = 32; \text{REF}_{\text{in}} = 7.0 \text{ GHz}.

\(^9\) The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20 log N (where N is the N divider value) and 10 log \(f_{\text{PFD}}\). PNSYNTH = PNTOT − 10 log \(f_{\text{PFD}}\) − 20 log N.

\(^10\) The PLL phase noise is composed of 1/f (flicker) noise plus the normalized PLL noise floor. The formula for calculating the 1/f noise contribution at an RF frequency, \(f_{\text{RF}}\), and at a frequency offset, \(f\), is given by \(PN = P_{N,1/f} + 10 \log(10 \text{ kHz}/f) + 20 \log(f_{\text{RF}}/1 \text{ GHz})\). All phase noise measurements were performed with the EV-ADF4108EBZ\(^1\) and the Agilent E5500 phase noise system. Both the normalized phase noise floor and flicker noise are modeled in ADIsimPLL.

\(^11\) The phase noise is measured with the EV-ADF4108EBZ evaluation board, with the ZComm CR80000Z VCO. The spectrum analyzer provides the \(f_{\text{REFIN}}\) for the synthesizer (\(f_{\text{REFIN}} = 10 \text{ MHz} @ 0 \text{ dBm}\)).

\(^12\) \(f_{\text{REFIN}} = 10 \text{ MHz}; f_{\text{PFD}} = 1 \text{ MHz}; f_{\text{RF}} = 7900 \text{ MHz}; N = 7900; \text{loop B/W} = 30 \text{ kHz}, \text{VCO} = \text{ZComm CR80000Z}.
TIMING CHARACTERISTICS

AVDD = DVDD = 3.3 V ± 2%, AVDD ≤ VP ≤ 5.5 V, AGND = DGND = CPGND = 0 V, RSET = 5.1 kΩ, dBm referred to 50 Ω, TA = TMIN to TMAX, unless otherwise noted.

Table 2.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Limit2 (B Version)</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>t1</td>
<td>10</td>
<td>ns min</td>
<td>DATA to CLOCK setup time</td>
</tr>
<tr>
<td>t2</td>
<td>10</td>
<td>ns min</td>
<td>DATA to CLOCK hold time</td>
</tr>
<tr>
<td>t3</td>
<td>25</td>
<td>ns min</td>
<td>CLOCK high duration</td>
</tr>
<tr>
<td>t4</td>
<td>25</td>
<td>ns min</td>
<td>CLOCK low duration</td>
</tr>
<tr>
<td>t5</td>
<td>10</td>
<td>ns min</td>
<td>CLOCK to LE setup time</td>
</tr>
<tr>
<td>t6</td>
<td>20</td>
<td>ns min</td>
<td>LE pulse width</td>
</tr>
</tbody>
</table>

1 Guaranteed by design but not production tested.
2 Operating temperature range (B Version) is −40°C to +85°C.

Figure 2. Timing Diagram
ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>AVDD to GND1</td>
<td>−0.3 V to +3.9 V</td>
</tr>
<tr>
<td>AVDD to DVDD</td>
<td>−0.3 V to +0.3 V</td>
</tr>
<tr>
<td>Vr to GND</td>
<td>−0.3 V to +5.8 V</td>
</tr>
<tr>
<td>Vr to AVDD</td>
<td>−0.3 V to +5.8 V</td>
</tr>
<tr>
<td>Digital I/O Voltage to GND</td>
<td>−0.3 V to VDD + 0.3 V</td>
</tr>
<tr>
<td>Analog I/O Voltage to GND</td>
<td>−0.3 V to Vr + 0.3 V</td>
</tr>
<tr>
<td>REFIN, RF InA, RF InB to GND</td>
<td>−0.3 V to VDD + 0.3 V</td>
</tr>
<tr>
<td>RF InA to RF InB</td>
<td>±600 mV</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>−40°C to +85°C</td>
</tr>
<tr>
<td>Industrial (B Version)</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>−65°C to +125°C</td>
</tr>
<tr>
<td>Maximum Junction Temperature</td>
<td>150°C</td>
</tr>
<tr>
<td>CSP θJA Thermal Impedance (Paddle Soldered)</td>
<td>30.4°C/W</td>
</tr>
<tr>
<td>Reflow Soldering</td>
<td></td>
</tr>
<tr>
<td>Peak Temperature (60 sec)</td>
<td>260°C</td>
</tr>
<tr>
<td>Time at Peak Temperature</td>
<td>40 sec</td>
</tr>
<tr>
<td>Transistor Count</td>
<td></td>
</tr>
<tr>
<td>CMOS</td>
<td>6425</td>
</tr>
<tr>
<td>Bipolar</td>
<td>303</td>
</tr>
</tbody>
</table>

^1 GND = AGND = DGND = 0 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance RF integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.
PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 4. Pin Function Descriptions

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>CPGND</td>
<td>Charge Pump Ground. This is the ground return path for the charge pump.</td>
</tr>
<tr>
<td>2, 3</td>
<td>AGND</td>
<td>Analog Ground. This is the ground return path of the prescaler.</td>
</tr>
<tr>
<td>4</td>
<td>RFINB</td>
<td>Complementary Input to the RF Prescaler. This point must be decoupled to the ground plane with a small bypass capacitor, typically 100 pF. See Figure 11.</td>
</tr>
<tr>
<td>5</td>
<td>RFINA</td>
<td>Input to the RF Prescaler. This small signal input is ac-coupled to the external VCO.</td>
</tr>
<tr>
<td>6, 7</td>
<td>AVDD</td>
<td>Analog Power Supply. This voltage may range from 3.2 V to 3.6 V. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin. AVDD must be the same value as DVDD.</td>
</tr>
<tr>
<td>8</td>
<td>REFIN</td>
<td>Reference Input. This is a CMOS input with a nominal threshold of VDD/2 and a dc equivalent input resistance of 100 kΩ. See Figure 10. This input can be driven from a TTL or CMOS crystal oscillator or it can be ac-coupled.</td>
</tr>
<tr>
<td>9, 10</td>
<td>DGND</td>
<td>Digital Ground.</td>
</tr>
<tr>
<td>11</td>
<td>CE</td>
<td>Chip Enable. A logic low on this pin powers down the device and puts the charge pump output into three-state mode. Taking the pin high powers up the device, depending on the status of the power-down bit, F2.</td>
</tr>
<tr>
<td>12</td>
<td>CLK</td>
<td>Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.</td>
</tr>
<tr>
<td>13</td>
<td>DATA</td>
<td>Serial Data Input. The serial data is loaded MSB first with the 2 LSBs being the control bits. This input is a high impedance CMOS input.</td>
</tr>
<tr>
<td>14</td>
<td>LE</td>
<td>Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches, the latch being selected using the control bits.</td>
</tr>
<tr>
<td>15</td>
<td>MUXOUT</td>
<td>This multiplexer output allows either the lock detect, the scaled RF, or the scaled reference frequency to be accessed externally.</td>
</tr>
<tr>
<td>16, 17</td>
<td>DVDD</td>
<td>Digital Power Supply. This may range from 3.2 V to 3.6 V. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. DVDD must be the same value as AVDD.</td>
</tr>
<tr>
<td>18</td>
<td>VP</td>
<td>Charge Pump Power Supply. This voltage should be greater than or equal to VDD. In systems where VDD is 3.3 V, it can be set to 5 V and used to drive a VCO with a tuning range of up to 5 V.</td>
</tr>
<tr>
<td>19</td>
<td>RSET</td>
<td>Connecting a resistor between this pin and CPGND sets the maximum charge pump output current. The nominal voltage potential at the RSET pin is 0.66 V. The relationship between ICP and RSET is</td>
</tr>
<tr>
<td></td>
<td></td>
<td>[ I_{CP,\text{MAX}} = \frac{25.5}{R_{SET}} ]</td>
</tr>
<tr>
<td></td>
<td></td>
<td>with RSET = 5.1 kΩ, ICP,\text{MAX} = 5 mA.</td>
</tr>
<tr>
<td>20</td>
<td>CP</td>
<td>Charge Pump Output. When enabled, this pin provides ( \pm I_{CP} ) to the external loop filter, which in turn drives the external VCO.</td>
</tr>
<tr>
<td></td>
<td>EP</td>
<td>Exposed Pad. The exposed pad must be connected to AGND.</td>
</tr>
</tbody>
</table>
TYPICAL PERFORMANCE CHARACTERISTICS

**PHASE NOISE (dBc/Hz)**

<table>
<thead>
<tr>
<th>RF INPUT POWER (dBm)</th>
<th>PHASE NOISE (dBc/Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>–0.150</td>
<td>–82.091dBc</td>
</tr>
<tr>
<td>–0.140</td>
<td>–82.091dBc</td>
</tr>
<tr>
<td>–0.130</td>
<td>–82.091dBc</td>
</tr>
<tr>
<td>–0.120</td>
<td>–82.091dBc</td>
</tr>
<tr>
<td>–0.110</td>
<td>–82.091dBc</td>
</tr>
<tr>
<td>–0.100</td>
<td>–82.091dBc</td>
</tr>
<tr>
<td>–0.090</td>
<td>–82.091dBc</td>
</tr>
<tr>
<td>–0.080</td>
<td>–82.091dBc</td>
</tr>
<tr>
<td>–0.070</td>
<td>–82.091dBc</td>
</tr>
<tr>
<td>–0.060</td>
<td>–82.091dBc</td>
</tr>
<tr>
<td>–0.050</td>
<td>–82.091dBc</td>
</tr>
<tr>
<td>–0.040</td>
<td>–82.091dBc</td>
</tr>
<tr>
<td>–0.030</td>
<td>–82.091dBc</td>
</tr>
<tr>
<td>–0.020</td>
<td>–82.091dBc</td>
</tr>
<tr>
<td>–0.010</td>
<td>–82.091dBc</td>
</tr>
<tr>
<td>–0.000</td>
<td>–82.091dBc</td>
</tr>
</tbody>
</table>

**RF INPUT FREQUENCY (GHz)**

<table>
<thead>
<tr>
<th>RF INPUT POWER (dBm)</th>
<th>PHASE NOISE (dBc/Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>–0.150</td>
<td>–82.091dBc</td>
</tr>
<tr>
<td>–0.140</td>
<td>–82.091dBc</td>
</tr>
<tr>
<td>–0.130</td>
<td>–82.091dBc</td>
</tr>
<tr>
<td>–0.120</td>
<td>–82.091dBc</td>
</tr>
<tr>
<td>–0.110</td>
<td>–82.091dBc</td>
</tr>
<tr>
<td>–0.100</td>
<td>–82.091dBc</td>
</tr>
<tr>
<td>–0.090</td>
<td>–82.091dBc</td>
</tr>
<tr>
<td>–0.080</td>
<td>–82.091dBc</td>
</tr>
<tr>
<td>–0.070</td>
<td>–82.091dBc</td>
</tr>
<tr>
<td>–0.060</td>
<td>–82.091dBc</td>
</tr>
<tr>
<td>–0.050</td>
<td>–82.091dBc</td>
</tr>
<tr>
<td>–0.040</td>
<td>–82.091dBc</td>
</tr>
<tr>
<td>–0.030</td>
<td>–82.091dBc</td>
</tr>
<tr>
<td>–0.020</td>
<td>–82.091dBc</td>
</tr>
<tr>
<td>–0.010</td>
<td>–82.091dBc</td>
</tr>
<tr>
<td>–0.000</td>
<td>–82.091dBc</td>
</tr>
</tbody>
</table>

**VDD = 3.3V, VP = 5V**

**ICP = 5mA**

**VCO = ZCOMM CRO8000Z**

**PHASE NOISE = –82dBc/Hz @ 1kHz**

**LOOP BANDWIDTH = 50kHz**

**VIDEO BANDWIDTH = 3kHz**

**AVERAGES = 1**

**OUTPUT POWER = –0.3dBm**

**VCO = ZCOMM CRO8000Z**

**Figure 4. S Parameter Data for the RF Input**

**Figure 5. RF Input Sensitivity**

**Figure 6. Phase Noise at 7.9 GHz**

**Figure 7. Reference Spurs at 7.9 GHz**

**Figure 8. Charge Pump Output Characteristics**

**Figure 9. Phase Noise (Referred to CP Output) vs. PFD Frequency**
THEORY OF OPERATION

REFERENCE INPUT STAGE

The reference input stage is shown in Figure 10. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REFIN pin on power-down.

RF INPUT STAGE

The RF input stage is shown in Figure 11. It is followed by a two-stage limiting amplifier to generate the CML clock levels needed for the prescaler.

PRESCALER (P/P + 1)

The dual-modulus prescaler (P/P + 1), along with the A and B counters, enables the large division ratio, N, to be realized (N = BP + A). The dual-modulus prescaler, operating at CML levels, takes the clock from the RF input stage and divides it down to a manageable frequency for the CMOS A and B counters. The prescaler is programmable. It can be set in software to 8/9, 16/17, 32/33, or 64/65. It is based on a synchronous 4/5 core. A minimum divide ratio is possible for contiguous output frequencies. This minimum is determined by P, the prescaler value, and is given by (P² – P).

A AND B COUNTERS

The A and B CMOS counters combine with the dual-modulus prescaler to allow a wide ranging division ratio in the PLL feedback counter. The counters are specified to work when the prescaler output is 300 MHz or less. Thus, with an RF input frequency of 4.0 GHz, a prescaler value of 16/17 is valid but a value of 8/9 is not valid.

Pulse Swallow Function

The A and B counters, in conjunction with the dual-modulus prescaler, make it possible to generate output frequencies that are spaced only by the reference frequency divided by R. The equation for the VCO frequency is as follows:

\[ f_{\text{VCO}} = \left( \left[ P \times B + A \right] \times \frac{f_{\text{REFIN}}}{R} \right) \]

where:
- \( f_{\text{VCO}} \) is the output frequency of external voltage controlled oscillator (VCO).
- \( P \) is the preset modulus of dual-modulus prescaler (8/9, 16/17, and so on.).
- \( B \) is the preset divide ratio of binary 13-bit counter (3 to 8191).
- \( A \) is the preset divide ratio of binary 6-bit swallow counter (0 to 63).
- \( f_{\text{REFIN}} \) is the external reference frequency oscillator.

R COUNTER

The 14-bit R counter allows the input reference frequency to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 16,383 are allowed.
PHASE FREQUENCY DETECTOR AND CHARGE PUMP

The phase frequency detector (PFD) takes inputs from the R counter and N counter \((N = BP + A)\) and produces an output proportional to the phase and frequency difference between them. Figure 13 is a simplified schematic. The PFD includes a programmable delay element that controls the width of the antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and minimizes phase noise and reference spurs. Two bits in the reference counter latch, ABP2 and ABP1, control the width of the pulse (see Figure 16). Use of the minimum antibacklash pulse width is not recommended.

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4108 allows the user to access various internal points on the chip. The state of MUXOUT is controlled by M3, M2, and M1 in the function latch. Figure 18 shows the full truth table. Figure 14 shows the MUXOUT section in block diagram form.

Lock Detect

MUXOUT can be programmed for two types of lock detect: digital lock detect and analog lock detect.

Digital lock detect is active high. When the lock detect precision (LDP) bit in the R counter latch is set to 0, digital lock detect is set high when the phase error on three consecutive phase detector (PD) cycles is less than 15 ns. With LDP set to 1, five consecutive cycles of less than 15 ns are required to set the lock detect. It stays set high until a phase error of greater than 25 ns is detected on any subsequent PD cycle.

The N-channel open-drain analog lock detect should be operated with an external pull-up resistor of 10 kΩ nominal. When lock has been detected, this output is high with narrow, low going pulses.

INPUT SHIFT REGISTER

The ADF4108 digital section includes a 24-bit input shift register, a 14-bit R counter, and a 19-bit N counter, comprising a 6-bit A counter and a 13-bit B counter. Data is clocked into the 24-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. These are the 2 LSBs, DB1 and DB0, as shown in the timing diagram of Figure 2. The truth table for these bits is shown in Table 5.

Table 5. C2 and C1 Truth Table

<table>
<thead>
<tr>
<th>C2</th>
<th>C1</th>
<th>Data Latch</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>R counter</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>N counter (A and B)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Function latch (including prescaler)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Initialization latch</td>
</tr>
</tbody>
</table>
### LATCH SUMMARY

**REFERENCE COUNTER LATCH**

<table>
<thead>
<tr>
<th>RESERVED</th>
<th>LOCK DETECTION</th>
<th>TEST MODE BITS</th>
<th>ANTI-BACKLASH WIDTH</th>
<th>14-BIT REFERENCE COUNTER</th>
<th>CONTROL BITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>DB23 DB22 DB21 DB20 DB19 DB18 DB17 DB16 DB15 DB14 DB13 DB12 DB11 DB10 DB9 DB8 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>X 0 0 LDP T2 T1 ABP2 ABP1 R14 R13 R12 R11 R10 R9 R8 R7 R6 R5 R4 R3 R2 R1 C2 (0) C1 (0)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**N COUNTER LATCH**

<table>
<thead>
<tr>
<th>RESERVED</th>
<th>GAIN</th>
<th>13-BIT B COUNTER</th>
<th>6-BIT A COUNTER</th>
<th>CONTROL BITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>DB23 DB22 DB21 DB20 DB19 DB18 DB17 DB16 DB15 DB14 DB13 DB12 DB11 DB10 DB9 DB8 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>X X G1 B13 B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 A6 A5 A4 A3 A2 A1 C2 (0) C1 (1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**FUNCTION LATCH**

<table>
<thead>
<tr>
<th>PRESCALER VALUE</th>
<th>POWER-DOWN</th>
<th>CURRENT SETTING 2</th>
<th>CURRENT SETTING 1</th>
<th>TIMER COUNTER CONTROL</th>
<th>FASTLOCK MODE</th>
<th>FASTLOCK ENABLE</th>
<th>CP THREE-STATE</th>
<th>POLARITY</th>
<th>MUXOUT CONTROL</th>
<th>POWER-DOWN</th>
<th>COUNTER RESET</th>
<th>CONTROL BITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>DB23 DB22 DB21 DB20 DB19 DB18 DB17 DB16 DB15 DB14 DB13 DB12 DB11 DB10 DB9 DB8 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0</td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P2 P1 PD2 CP6 CP5 CP4 CP3 CP2 CP1 TC4 TC3 TC2 TC1 F5 F4 F3 F2 M3 M2 M1 PD1 F1 C2 (1) C1 (0)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**INITIALIZATION LATCH**

<table>
<thead>
<tr>
<th>PRESCALER VALUE</th>
<th>POWER-DOWN</th>
<th>CURRENT SETTING 2</th>
<th>CURRENT SETTING 1</th>
<th>TIMER COUNTER CONTROL</th>
<th>FASTLOCK MODE</th>
<th>FASTLOCK ENABLE</th>
<th>CP THREE-STATE</th>
<th>POLARITY</th>
<th>MUXOUT CONTROL</th>
<th>POWER-DOWN</th>
<th>COUNTER RESET</th>
<th>CONTROL BITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>DB23 DB22 DB21 DB20 DB19 DB18 DB17 DB16 DB15 DB14 DB13 DB12 DB11 DB10 DB9 DB8 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P2 P1 PD2 CP6 CP5 CP4 CP3 CP2 CP1 TC4 TC3 TC2 TC1 F5 F4 F3 F2 M3 M2 M1 PD1 F1 C2 (1) C1 (1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Figure 15. Latch Summary*
REFERENCE COUNTER LATCH MAP

<table>
<thead>
<tr>
<th>RESERVED</th>
<th>LOCK DETECT</th>
<th>TEST MODE BITS</th>
<th>ANTI-BACKLASH PULSE WIDTH</th>
<th>14-BIT REFERENCE COUNTER</th>
<th>CONTROL BITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>DB23</td>
<td>DB22</td>
<td>DB21</td>
<td>DB20</td>
<td>DB19</td>
<td>DB18</td>
</tr>
<tr>
<td></td>
<td></td>
<td>X</td>
<td>T2</td>
<td>T1</td>
<td>ABP2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>R14</td>
<td>R13</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>R12</td>
<td>R11</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>R10</td>
<td>R9</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
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<td>R8</td>
<td>R7</td>
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<td>R6</td>
<td>R5</td>
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<td></td>
<td></td>
<td>R4</td>
<td>R3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>R2</td>
<td>R1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>C2 (0)</td>
<td>C1 (0)</td>
</tr>
</tbody>
</table>

X = DON'T CARE

14-BIT REFERENCE COUNTER

<table>
<thead>
<tr>
<th>R14</th>
<th>R13</th>
<th>R12</th>
<th>.......</th>
<th>R3</th>
<th>R2</th>
<th>R1</th>
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</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>.......</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>.......</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>.......</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>.......</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

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<table>
<thead>
<tr>
<th></th>
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</tbody>
</table>

DIVIDE RATIO

<table>
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<th>0</th>
<th>.......</th>
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</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>.......</td>
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</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>.......</td>
<td>1</td>
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<td>0</td>
</tr>
<tr>
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<td>1</td>
<td>1</td>
<td>.......</td>
<td>1</td>
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</table>

ANTIBACKLASH PULSE WIDTH

<table>
<thead>
<tr>
<th>ABP2</th>
<th>ABP1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

TEST MODE BITS SHOULD BE SET TO 00 FOR NORMAL OPERATION.

LDP OPERATION

<table>
<thead>
<tr>
<th>LDP</th>
<th>OPERATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>THREE CONSECUTIVE CYCLES OF PHASE DELAY LESS THAN 15ns MUST OCCUR BEFORE LOCK DETECT IS SET.</td>
</tr>
<tr>
<td>1</td>
<td>FIVE CONSECUTIVE CYCLES OF PHASE DELAY LESS THAN 15ns MUST OCCUR BEFORE LOCK DETECT IS SET.</td>
</tr>
</tbody>
</table>

BOTH OF THESE BITS MUST BE SET TO 0 FOR NORMAL OPERATION.

Figure 16. Reference Counter Latch Map
# AB COUNTER LATCH MAP

<table>
<thead>
<tr>
<th>RESERVED CP GAIN</th>
<th>13-BIT B COUNTER</th>
<th>6-BIT A COUNTER</th>
<th>CONTROL BITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>DB23 DB22 DB21 DB20 DB19 DB18 DB17 DB16 DB15 DB14 DB13 DB12 DB11 DB10 DB9 DB8 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>X X G1 B13 B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 A6 A5 A4 A3 A2 A1 CZ (0) C1 (1)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **X** = DON'T CARE

## A6 A5 A4 A3 A2 A1 B COUNTER DIVIDE RATIO

<table>
<thead>
<tr>
<th>A6</th>
<th>A5</th>
<th>A4</th>
<th>A3</th>
<th>A2</th>
<th>A1</th>
<th>B COUNTER DIVIDE RATIO</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>NOT ALLOWED</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>NOT ALLOWED</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>NOT ALLOWED</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>NOT ALLOWED</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>3</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>8188</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>8190</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>8191</td>
</tr>
</tbody>
</table>

## F4 (FUNCTION LATCH) FASTLOCK ENABLE G1 CP GAIN OPERATION

<table>
<thead>
<tr>
<th>F4 (FUNCTION LATCH)</th>
<th>FASTLOCK ENABLE</th>
<th>G1</th>
<th>CP GAIN</th>
<th>OPERATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>CHARGE PUMP CURRENT SETTING 1 IS PERMANENTLY USED.</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>CHARGE PUMP CURRENT SETTING 2 IS PERMANENTLY USED.</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>CHARGE PUMP CURRENT SETTING 1 IS USED.</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>CHARGE PUMP CURRENT IS SWITCHED TO SETTING 2. THE TIME SPENT IN SETTING 2 IS DEPENDENT ON WHICH FASTLOCK MODE IS USED. SEE FUNCTION LATCH DESCRIPTION.</td>
</tr>
</tbody>
</table>

- **N = BP + A, P IS PRESCALER VALUE SET IN THE FUNCTION LATCH. B MUST BE GREATER THAN OR EQUAL TO A. FOR CONTINUOUSLY ADJACENT VALUES OF (N × FREF), AT THE OUTPUT, NMIN IS (P^2 – P).**

---

*Figure 17. AB Counter Latch Map*
Figure 18. Function Latch Map
Figure 19. Initialization Latch Map
FUNCTION LATCH

The on-chip function latch is programmed with C2 and C1 set to 1 and 0, respectively. Figure 18 shows the input data format for programming the function latch.

Counter Reset

DB2 (F1) is the counter reset bit. When this bit is 1, the R counter and the AB counters are reset. For normal operation, this bit should be 0. Upon powering up, the F1 bit needs to be disabled (set to 0). Then, the N counter resumes counting in close alignment with the R counter. (The maximum error is one prescaler cycle.)

Power-Down

DB3 (PD1) and DB21 (PD2) provide programmable power-down modes. They are enabled by the CE pin.

When the CE pin is low, the device is immediately disabled regardless of the states of PD2 and PD1.

In the programmed asynchronous power-down, the device powers down immediately after latching a 1 into the PD1 bit, with the condition that PD2 has been loaded with a 0.

In the programmed synchronous power-down, the device powers down by the charge pump to prevent unwanted frequency jumps. Once the power-down is enabled by writing a 1 into PD1 (on condition that a 1 has also been loaded to PD2), the device goes into power-down on the occurrence of the next charge pump event.

When a power-down is activated (either synchronous or asynchronous mode, including CE pin activated power-down), the following events occur:

- All active dc current paths are removed.
- The R, N, and timeout counters are forced to their load state conditions.
- The charge pump is forced into three-state mode.
- The digital lock detect circuitry is reset.
- The RFIN input is debiased.
- The reference input buffer circuitry is disabled.
- The input register remains active and capable of loading and latching data.

MUXOUT Control

The on-chip multiplexer is controlled by M3, M2, and M1 on the ADF4108. Figure 18 shows the truth table.

Fastlock Enable Bit

DB9 of the function latch is the fastlock enable bit. Fastlock is enabled only when this bit is 1.

Fastlock Mode Bit

DB10 of the function latch is the fastlock mode bit. When fastlock is enabled, this bit determines which fastlock mode is used. If the fastlock mode bit is 0, then Fastlock Mode 1 is selected; and if the fastlock mode bit is 1, then Fastlock Mode 2 is selected.

Fastlock Mode 1

The charge pump current is switched to the contents of Current Setting 2.

The device enters fastlock by having a 1 written to the CP gain bit in the AB counter latch. The device exits fastlock by having a 0 written to the CP gain bit in the AB counter latch.

Fastlock Mode 2

The charge pump current is switched to the contents of Current Setting 2.

The device enters fastlock by having a 1 written to the CP gain bit in the AB counter latch. The device exits fastlock under the control of the timer counter. After the timeout period determined by the value in TC4:TC1, the CP gain bit in the AB counter latch is automatically reset to 0 and the device reverts to normal mode instead of fastlock. See Figure 18 for the timeout periods.

Timer Counter Control

The user has the option of programming two charge pump currents. The intent is that Current Setting 1 is used when the RF output is stable and the system is in a static state. Current Setting 2 is meant to be used when the system is dynamic and in a state of change (that is, when a new output frequency is programmed).

The normal sequence of events is as follows:

The user initially decides what the preferred charge pump currents are going to be. For example, the choice may be 2.5 mA as Current Setting 1 and 5 mA as Current Setting 2.

At the same time, it must be decided how long the secondary current is to stay active before reverting to the primary current. This is controlled by the timer counter control bits, DB14:DB11 (TC4:TC1) in the function latch. The truth table is given in Figure 18.

Now, to program a new output frequency, the user simply programs the AB counter latch with new values for A and B. At the same time, the CP gain bit can be set to 1, which sets the charge pump with the value in CPI6:CPI4 for a period of time determined by TC4:TC1. When this time is up, the charge pump current reverts to the value set by CPI3:CPI1. At the same time, the CP gain bit in the AB counter latch is reset to 0 and is now ready for the next time the user wishes to change the frequency.

Note that there is an enable feature on the timer counter. It is enabled when Fastlock Mode 2 is chosen by setting the fastlock mode bit (DB10) in the function latch to 1.
**Charge Pump Currents**

CPI3, CPI2, and CPI1 program Current Setting 1 for the charge pump. CPI6, CPI5, and CPI4 program Current Setting 2 for the charge pump. The truth table is given in Figure 18.

**Prescaler Value**

P2 and P1 in the function latch set the prescaler values. The prescaler value should be chosen so that the prescaler output frequency is always less than or equal to 300 MHz. Thus, with an RF frequency of 4 GHz, a prescaler value of 16/17 is valid but a value of 8/9 is not valid.

**PD Polarity**

This bit sets the phase detector polarity bit. See Figure 18.

**CP Three-State**

This bit controls the CP output pin. With the bit set high, the CP output is put into three-state. With the bit set low, the CP output is enabled.

**INITIALIZATION LATCH**

The initialization latch is programmed when C2 and C1 are set to 1 and 1. This is essentially the same as the function latch (programmed when C2, C1 = 1, 0).

However, when the initialization latch is programmed, an additional internal reset pulse is applied to the R and AB counters. This pulse ensures that the AB counter is at load point when the AB counter data is latched and the device will begin counting in close phase alignment.

If the latch is programmed for synchronous power-down (CE pin is high; PD1 bit is high; PD2 bit is low), the internal pulse also triggers this power-down. The prescaler reference and the oscillator input buffer are unaffected by the internal reset pulse and so close phase alignment is maintained when counting resumes.

When the first AB counter data is latched after initialization, the internal reset pulse is again activated. However, successive AB loads after this do not trigger the internal reset pulse.

**Device Programming After Initial Power-Up**

After initially powering up the device, there are three ways to program the device.

**Initialization Latch Method**

1. Apply VDD.
2. Program the initialization latch (11 in 2 LSBs of input word). Make sure that the F1 bit is programmed to 0.
3. Next, do a function latch load (10 in 2 LSBs of the control word), making sure that the F1 bit is programmed to a 0.
4. Then do an R load (00 in 2 LSBs).
5. Then do an AB load (01 in 2 LSBs).

When the initialization latch is loaded, the following occurs:

1. The function latch contents are loaded.
2. An internal pulse resets the R, AB, and timeout counters to load state conditions and also three-states the charge pump. Note that the prescaler band gap reference and the oscillator input buffer are unaffected by the internal reset pulse, allowing close phase alignment when counting resumes.
3. Latching the first AB counter data after the initialization word activates the same internal reset pulse. Successive AB loads do not trigger the internal reset pulse unless there is another initialization.

**CE Pin Method**

1. Apply VDD.
2. Bring CE low to put the device into power-down. This is an asynchronous power-down in that it happens immediately.
3. Program the function latch (10).
4. Program the R counter latch (00).
5. Program the AB counter latch (01).
6. Bring CE high to take the device out of power-down. The R and AB counters will now resume counting in close alignment.

Note that after CE goes high, a duration of 1 μs may be required for the prescaler band gap voltage and oscillator input buffer bias to reach steady state.

CE can be used to power the device up and down to check for channel activity. The input register does not need to be reprogrammed each time the device is disabled and enabled as long as it has been programmed at least once after VDD was initially applied.

**Counter Reset Method**

1. Apply VDD.
2. Do a function latch load (10 in 2 LSBs). As part of this, load 1 to the F1 bit. This enables the counter reset.
3. Do an R counter load (00 in 2 LSBs).
4. Do an AB counter load (01 in 2 LSBs).
5. Do a function latch load (10 in 2 LSBs). As part of this, load 0 to the F1 bit. This disables the counter reset.

This sequence provides the same close alignment as the initialization method. It offers direct control over the internal reset. Note that counter reset holds the counters at load point and three-states the charge pump, but does not trigger synchronous power-down.

**POWER SUPPLY CONSIDERATIONS**

The ADF4108 operates over a power supply range of 3.2 V to 3.6 V. The ADP3300ART-3.3 is a low dropout linear regulator from Analog Devices, Inc. It outputs 3.3 V with an accuracy of 1.4% and is recommended for use with the ADF4108.
INTERFACING

The ADF4108 has a simple SPI-compatible serial interface for writing to the device. CLK, DATA, and LE control the data transfer. When LE (latch enable) goes high, the 24 bits that have been clocked into the input register on each rising edge of CLK are transferred to the appropriate latch. See Figure 2 for the timing diagram and Table 5 for the latch truth table.

The maximum allowable serial clock rate is 20 MHz. This means that the maximum update rate possible for the device is 833 kHz or one update every 1.2 µs. This is certainly more than adequate for systems that have typical lock times in hundreds of microseconds.

ADUC812 INTERFACE

Figure 20 shows the interface between the ADF4108 and the ADuC812 MicroConverter®. Because the ADuC812 is based on an 8051 core, this interface can be used with any 8051-based microcontroller. The MicroConverter is set up for SPI master mode with CPHA = 0. To initiate the operation, the I/O port driving LE is brought low. Each latch of the ADF4108 needs a 24-bit word. This is accomplished by writing three 8-bit bytes from the MicroConverter to the device. When the third byte has been written, the LE input should be brought high to complete the transfer.

On first applying power to the ADF4108, it needs four writes (one each to the initialization latch, function latch, R counter latch, and N counter latch) for the output to become active.

I/O port lines on the ADuC812 are also used to control power-down (CE input) and to detect lock (MUXOUT configured as lock detect and polled by the port input).

When operating in the mode described, the maximum SCLOCK rate of the ADuC812 is 4 MHz. This means that the maximum rate at which the output frequency can be changed is 166 kHz.

ADSP-21xx INTERFACE

Figure 21 shows the interface between the ADF4108 and the ADSP-21xx digital signal processor. The ADF4108 needs a 24-bit serial word for each latch write. The easiest way to accomplish this using the ADSP-21xx family is to use the autobuffered transmit mode of operation with alternate framing. This provides a means for transmitting an entire block of serial data before an interrupt is generated. Set up the word length for 8 bits and use three memory locations for each 24-bit word. To program each 24-bit latch, store the three 8-bit bytes, enable the autobuffered mode, and then write to the transmit register of the DSP. This last operation initiates the autobuffer transfer.
PCB DESIGN GUIDELINES FOR CHIP SCALE PACKAGE

The lands on the chip scale package (CP-20-6) are rectangular. The printed circuit board pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This ensures that the solder joint size is maximized. The bottom of the chip scale package has a central thermal pad.

The thermal pad on the printed circuit board should be at least as large as this exposed pad. On the printed circuit board, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern. This ensures that shorting is avoided.

Thermal vias can be used on the printed circuit board thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated in the thermal pad at 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm and the via barrel should be plated with 1 oz. copper to plug the via.

The user should connect the printed circuit board thermal pad to AGND.
OUTLINE DIMENSIONS

Dimensions shown in millimeters

COMPLIANT TO JEDEC STANDARDS MO-220-WGGO-1.

ORDERING GUIDE

<table>
<thead>
<tr>
<th>Model</th>
<th>Temperature Range</th>
<th>Package Description</th>
<th>Package Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADF4108BCPZ</td>
<td>−40°C to +85°C</td>
<td>20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]</td>
<td>CP-20-6</td>
</tr>
<tr>
<td>ADF4108BCPZ-RL</td>
<td>−40°C to +85°C</td>
<td>20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]</td>
<td>CP-20-6</td>
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<tr>
<td>ADF4108BCPZ-RL7</td>
<td>−40°C to +85°C</td>
<td>20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]</td>
<td>CP-20-6</td>
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<td>EV-ADF4108EB1Z</td>
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<td>Evaluation Board</td>
<td>CP-20-6</td>
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<tr>
<td>EV-ADF4108EB2Z</td>
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<td>Evaluation Board</td>
<td>CP-20-6</td>
</tr>
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</table>

1 Z = RoHS Compliant Part.