The AD826 features high output current drive capability of 50 mA min per amp, and is able to drive unlimited capacitive loads. With a low power supply current of 15 mA max for both amplifiers, the AD826 is a true general purpose operational amplifier.

The AD826 is ideal for power sensitive applications such as video cameras and portable instrumentation. The AD826 can operate from a single +5 V supply, while still achieving 25 MHz of bandwidth. Furthermore the AD826 is fully specified from a single +5 V to ±15 V power supplies.

The AD826 excels as an ADC/DAC buffer or active filter in data acquisition systems and achieves a settling time of 70 ns to 0.01%, with a low input offset voltage of 2 mV max. The AD826 is available in small 8-lead plastic mini-DIP and SO packages.
**COMPARABLE PARTS**

View a parametric search of comparable parts.

**EVALUATION KITS**

- Universal Evaluation Board for Dual High Speed Operational Amplifiers

**DOCUMENTATION**

**Application Notes**
- AN-402: Replacing Output Clamping Op Amps with Input Clamping Amps
- AN-417: Fast Rail-to-Rail Operational Amplifiers Ease Design Constraints in Low Voltage High Speed Systems
- AN-581: Biasing and Decoupling Op Amps in Single Supply Applications
- AN-649: Using the Analog Devices Active Filter Design Tool

**Data Sheet**
- AD826: High Speed, Low Power Dual Operational Amplifier Data Sheet

**User Guides**
- UG-128: Universal Evaluation Board for Dual High Speed Op Amps in SOIC Packages

**TOOLS AND SIMULATIONS**

- Analog Filter Wizard
- Analog Photodiode Wizard
- Power Dissipation vs Die Temp
- VRMS/dBm/dBu/dBV calculators
- AD826 SPICE Macro-Model

**REFERENCE MATERIALS**

**Product Selection Guide**
- High Speed Amplifiers Selection Table

**Tutorials**
- MT-032: Ideal Voltage Feedback (VFB) Op Amp
- MT-033: Voltage Feedback Op Amp Gain and Bandwidth
- MT-047: Op Amp Noise
- MT-049: Op Amp Total Output Noise Calculations for Single-Pole System
- MT-050: Op Amp Total Output Noise Calculations for Second-Order System
- MT-052: Op Amp Noise Figure: Don't Be Misled
- MT-053: Op Amp Distortion: HD, THD, THD + N, IMD, SFDR, MTPR
- MT-056: High Speed Voltage Feedback Op Amps
- MT-058: Effects of Feedback Capacitance on VFB and CFB Op Amps
- MT-060: Choosing Between Voltage Feedback and Current Feedback Op Amps

**DESIGN RESOURCES**

- AD826 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

**DISCUSSIONS**

View all AD826 EngineerZone Discussions.

**SAMPLE AND BUY**

Visit the product page to see pricing options.

**TECHNICAL SUPPORT**

Submit a technical question or find your regional support number.

**DOCUMENT FEEDBACK**

Submit feedback for this data sheet.
## AD826—SPECIFICATIONS (® T_A = +25°C, unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>V_s</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DYNAMIC PERFORMANCE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Unity Gain Bandwidth</td>
<td></td>
<td>±5 V</td>
<td>30</td>
<td>35</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>±15 V</td>
<td>45</td>
<td>50</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td>±0, +5 V</td>
<td>25</td>
<td>29</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bandwidth for 0.1 dB Flatness</td>
<td>±5 V</td>
<td>10</td>
<td>20</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>±15 V</td>
<td>25</td>
<td>55</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>±0, +5 V</td>
<td>10</td>
<td>20</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Full Power Bandwidth¹</td>
<td>V_OUT = 5 V p-p</td>
<td>±5 V</td>
<td>15.9</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>R_LOAD = 500 Ω</td>
<td>±15 V</td>
<td>5.6</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Slew Rate</td>
<td>R_LOAD = 1 kΩ</td>
<td>±5 V</td>
<td>200</td>
<td>V/µs</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0, +5 V</td>
<td>150</td>
<td>200</td>
<td>V/µs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Settling Time to 0.1%</td>
<td>±2.5 V to +2.5 V</td>
<td>±5 V</td>
<td>45</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 V–10 V Step, AV = –1</td>
<td>±15 V</td>
<td>45</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>±2.5 V to +2.5 V</td>
<td>±5 V</td>
<td>70</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 V–10 V Step, AV = –1</td>
<td>±15 V</td>
<td>70</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>NOISE/HARMONIC PERFORMANCE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total Harmonic Distortion</td>
<td>F_C = 1 MHz</td>
<td>±15 V</td>
<td>–78</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage Noise</td>
<td>f = 10 kHz</td>
<td>±5 V, ±15 V</td>
<td>15</td>
<td>nV/√Hz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Current Noise</td>
<td>f = 10 kHz</td>
<td>±5 V, ±15 V</td>
<td>1.5</td>
<td>pA/√Hz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential Gain Error</td>
<td>NTSC</td>
<td>±15 V</td>
<td>0.07</td>
<td>0.1%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(R1 = 150 Ω)</td>
<td>Gain = +2</td>
<td>±5 V</td>
<td>0.12</td>
<td>0.15%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>±0, +5 V</td>
<td>0.15%</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential Phase Error</td>
<td>NTSC</td>
<td>±15 V</td>
<td>0.11</td>
<td>0.15 Degrees</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(R1 = 150 Ω)</td>
<td>Gain = +2</td>
<td>±5 V</td>
<td>0.12</td>
<td>0.15 Degrees</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>±0, +5 V</td>
<td>0.15 Degrees</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>DC PERFORMANCE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Offset Voltage</td>
<td>±5 V to ±15 V</td>
<td>0.5</td>
<td>2</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>T_MIN to T_MAX</td>
<td>3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Offset Drift</td>
<td>±5 V, ±15 V</td>
<td>10</td>
<td>3</td>
<td>µV/°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Bias Current</td>
<td>±5 V, ±15 V</td>
<td>3.3</td>
<td>6.6</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>T_MIN</td>
<td>10</td>
<td></td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>T_MAX</td>
<td>4.4</td>
<td></td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Offset Current</td>
<td>±5 V, ±15 V</td>
<td>25</td>
<td>300</td>
<td>nA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>T_MIN to T_MAX</td>
<td>250</td>
<td></td>
<td>nA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Offset Current Drift</td>
<td>±5 V</td>
<td>0.3</td>
<td></td>
<td>nA/°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Open-Loop Gain</td>
<td>V_OUT = ±2.5 V</td>
<td>±5 V</td>
<td>2</td>
<td>4</td>
<td>V/mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td>R_LOAD = 500 Ω</td>
<td>1.5</td>
<td></td>
<td>V/mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>T_MIN to T_MAX</td>
<td>1.5</td>
<td></td>
<td>V/mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>R_LOAD = 150 Ω</td>
<td>±15 V</td>
<td>3.5</td>
<td>6</td>
<td>V/mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td>T_MIN to T_MAX</td>
<td>2</td>
<td></td>
<td>V/mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>V_OUT = ±7.5 V</td>
<td>±15 V</td>
<td>2</td>
<td>4</td>
<td>V/mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td>R_LOAD = 150 Ω (50 mA Output)</td>
<td>±15 V</td>
<td>2</td>
<td>4</td>
<td>V/mV</td>
<td></td>
</tr>
<tr>
<td><strong>INPUT CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Resistance</td>
<td>±5 V</td>
<td>300</td>
<td></td>
<td>kΩ</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.5</td>
<td></td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>±5 V</td>
<td>+3.8</td>
<td>+4.3</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Common-Mode Voltage Range</td>
<td>±5 V</td>
<td>−3.7</td>
<td>−3.4</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>±15 V</td>
<td>+13</td>
<td>+14.3</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>−12</td>
<td>−13.4</td>
<td></td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>±0, +5 V</td>
<td>+3.8</td>
<td>+4.3</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Common-Mode Rejection Ratio</td>
<td>V_CM = ±2.5 V, T_MIN–T_MAX</td>
<td>±5 V</td>
<td>80</td>
<td>100</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td>V_CM = ±12 V</td>
<td>±15 V</td>
<td>86</td>
<td>120</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td>T_MIN to T_MAX</td>
<td>±15 V</td>
<td>80</td>
<td>100</td>
<td>dB</td>
<td></td>
</tr>
</tbody>
</table>
### Absolute Maximum Ratings

1. Supply Voltage: ±18 V
2. Internal Power Dissipation:
   - Plastic (N): See Derating Curves
   - Small Outline (R): See Derating Curves
3. Input Voltage (Common Mode): ±Vᵢ
4. Differential Input Voltage: ±5 V
5. Output Short Circuit Duration: See Derating Curves
6. Storage Temperature Range: -65°C to +125°C
7. Operating Temperature Range: -40°C to +85°C
8. Lead Temperature Range (Soldering 10 seconds): +300°C

### Absolute Maximum Ratings Notes

1. Full power bandwidth = slew rate/2πV_peak.
2. Specifications subject to change without notice.

### Matching Characteristics

**Dynamic**
- Crosstalk: f = 5 MHz
- Gain Flatness Match: G = +1, f = 40 MHz
- Slew Rate Match: G = -1

**DC**
- Input Offset Voltage Match: T_MIN – T_MAX
- Input Bias Current Match: T_MIN – T_MAX
- Open-Loop Gain Match: V_O = ±10 V, R_LOAD = 1 kΩ
- Common-Mode Rejection Ratio Match: V_CM = ±12 V, T_MIN – T_MAX
- Power Supply Rejection Ratio Match: VO = ±10 V, R_LOAD = 1 kΩ, T_MIN – T_MAX

### Power Supply

- Operating Range: Dual Supply ±5 V to ±15 V
- Single Supply ±5 V to ±15 V
- Quiescent Current/Amplifier: T_MIN to T_MAX
- Power Supply Rejection Ratio: V_S = ±5 V to ±15 V, T_MIN to T_MAX

### Notes

1. Full power bandwidth = slew rate/2πV_peak.
2. Specifications subject to change without notice.

### ESD Susceptibility

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although the AD826 features proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.
AD826 – Typical Characteristics

**Figure 1.** Common-Mode Voltage Range vs. Supply

**Figure 2.** Output Voltage Swing vs. Supply

**Figure 3.** Output Voltage Swing vs. Load Resistance

**Figure 4.** Quiescent Supply Current per Amp vs. Supply Voltage for Various Temperatures

**Figure 5.** Slew Rate vs. Supply Voltage

**Figure 6.** Closed-Loop Output Impedance vs. Frequency
Figure 7. Input Bias Current vs. Temperature

Figure 8. Short Circuit Current vs. Temperature

Figure 9. Unity Gain Bandwidth and Phase Margin vs. Temperature

Figure 10. Open-Loop Gain and Phase Margin vs. Frequency

Figure 11. Open-Loop Gain vs. Load Resistance

Figure 12. Power Supply Rejection vs. Frequency
Figure 13. Common-Mode Rejection vs. Frequency

Figure 14. Large Signal Frequency Response

Figure 15. Output Swing and Error vs. Settling Time

Figure 16. Harmonic Distortion vs. Frequency

Figure 17. Input Voltage Noise Spectral Density

Figure 18. Slew Rate vs. Temperature
Figure 19. Closed-Loop Gain vs. Frequency

Figure 20. Differential Gain and Phase vs. Supply Voltage

Figure 21. Crosstalk vs. Frequency

Figure 22. Closed-Loop Gain vs. Frequency, Gain = –1

Figure 23. Gain Flatness Matching vs. Supply, G = +1

Figure 24. Crosstalk Test Circuit
Figure 25. Noninverting Amplifier Configuration

Figure 26. Noninverting Large Signal Pulse Response, $R_L = 1 \text{ k}\Omega$

Figure 27. Noninverting Large Signal Pulse Response, $R_L = 150 \text{ \Omega}$

Figure 28. Noninverting Small Signal Pulse Response, $R_L = 1 \text{ k}\Omega$

Figure 29. Noninverting Small Signal Pulse Response, $R_L = 150 \text{ \Omega}$
Figure 30. Inverting Amplifier Configuration

Figure 31. Inverting Large Signal Pulse Response, $R_L = 1 \, \text{k}\Omega$

Figure 32. Inverting Large Signal Pulse Response, $R_L = 150 \, \Omega$

Figure 33. Inverting Small Signal Pulse Response, $R_L = 1 \, \text{k}\Omega$

Figure 34. Inverting Small Signal Pulse Response, $R_L = 150 \, \Omega$
THEORY OF OPERATION

The AD826 is a low cost, wide band, high performance dual operational amplifier which can drive heavy capacitive and resistive loads. It also achieves a constant slew rate, bandwidth and settling time over its entire specified temperature range.

The AD826 (Figure 35) consists of a degenerated NPN differential pair driving matched PNP s in a folded-cascode gain stage. The output buffer stage employs emitter followers in a class AB amplifier which delivers the necessary current to the load while maintaining low levels of distortion.

![Figure 35. Simplified Schematic](image)

The capacitor, \( C_f \), in the output stage mitigates the effect of capacitive loads. With low capacitive loads, the gain from the compensation node to the output is very close to unity. In this case, \( C_f \) is bootstrapped and does not contribute to the overall compensation capacitance of the device. As the capacitive load is increased, a pole is formed with the output impedance of the output stage. This reduces the gain, and therefore, \( C_f \) is incompletely bootstrapped. Effectively, some fraction of \( C_f \) contributes to the overall compensation capacitance, reducing the unity gain bandwidth. As the load capacitance is further increased, the bandwidth continues to fall, maintaining the stability of the amplifier.

INPUT CONSIDERATIONS

An input protection resistor (\( R_{IN} \) in Figure 25) is required in circuits where the input to the AD826 will be subjected to transient or continuous overload voltages exceeding the ±6 V maximum differential limit. This resistor provides protection for the input transistors by limiting their maximum base current.

For high performance circuits, it is recommended that a “balancing” resistor be used to reduce the offset errors caused by bias current flowing through the input and feedback resistors. The balancing resistor equals the parallel combination of \( R_{IN} \) and \( R_f \) and thus provides a matched impedance at each input terminal. The offset voltage error will then be reduced by more than an order of magnitude.

APPLYING THE AD826

The AD826 is a breakthrough dual amp that delivers precision and speed at low cost with low power consumption. The AD826 offers excellent static and dynamic matching characteristics, combined with the ability to drive heavy resistive and capacitive loads. As with all high frequency circuits, care should be taken to maintain overall device performance as well as their matching. The following items are presented as general design considerations.

Circuit Board Layout

Input and output runs should be laid out so as to physically isolate them from remaining runs. In addition, the feedback resistor of each amplifier should be placed away from the feedback resistor of the other amplifier, since this greatly reduces inter-amp coupling.

Choosing Feedback and Gain Resistors

In order to prevent the stray capacitance present at each amplifier’s summing junction from limiting its performance, the feedback resistors should be \( \leq 1 \, k\Omega \). Since the summing junction capacitance may cause peaking, a small capacitor (1 pF–5 pF) maybe paralleled with \( R_f \) to neutralize this effect. Finally, sockets should be avoided, because of their tendency to increase interlead capacitance.

Power Supply Considerations

To ensure the proper operation of the AD826, connect the positive supply before the negative supply. Also, proper power supply decoupling is critical to preserve the integrity of high frequency signals. In carefully laid out designs, decoupling capacitors should be placed in close proximity to the supply pins, while their lead lengths should be kept to a minimum. These measures greatly reduce undesired inductive effects on the amplifier’s response.

Though two 0.1 \( \mu \)F capacitors will typically be effective in decoupling the supplies, several capacitors of different values can be paralleled to cover a wider frequency range.
SINGLE SUPPLY OPERATION

An exciting feature of the AD826 is its ability to perform well in a single supply configuration (see Figure 37). The AD826 is ideally suited for applications that require low power dissipation and high output current and those which need to drive large capacitive loads, such as high-speed buffering and instrumentation.

Referring to Figure 36, careful consideration should be given to the proper selection of component values. The choices for this particular circuit are: \((R1 + R3)\left|\frac{1}{R2}\right|\) combine with \(C1\) to form a low frequency corner of approximately 30 Hz.

**Figure 36. Single Supply Amplifier Configuration**

R3 and C2 reduce the effect of the power supply changes on the output by low-pass filtering with a corner at \(\frac{1}{2\pi R3C2}\).

The values for \(R_L\) and \(C_L\) were chosen to demonstrate the AD826’s exceptional output drive capability. In this configuration, the output is centered around 2.5 V. In order to eliminate the static dc current associated with this level, \(C3\) was inserted in series with \(R_L\).

**Figure 37. Single Supply Pulse Response, \(G = +1\), \(R_L = 150\,\Omega\), \(C_L = 200\,\mu F\)**

PARALLEL AMPS PROVIDE 100 mA TO LOAD

By taking advantage of the superior matching characteristics of the AD826, enhanced performance can easily be achieved by employing the circuit in Figure 38. Here, two identical cells are paralleled to obtain even higher load driving capability than that of a single amplifier (100 mA min guaranteed). R1 and R2 are included to limit current flow between amplifier outputs that would arise in the presence of any residual mismatch.

**Figure 38. Parallel Amp Configuration**
**AD826**

**SINGLE-ENDED TO DIFFERENTIAL LINE DRIVER**
Outstanding CMRR (> 80 dB @ 5 MHz), high bandwidth, wide supply voltage range, and the ability to drive heavy loads, make the AD826 an ideal choice for many line driving applications. In this application, the AD830 high speed video difference amp serves as the differential line receiver on the end of a back terminated, 50 ft., twisted-pair transmission line (see Figure 40). The overall system is configured in a gain of +1 and has a −3 dB bandwidth of 14 MHz. Figure 39 is the pulse response with a 2 V p-p, 1 MHz signal input.

**Figure 39. Pulse Response**

**Figure 40. Differential Line Driver**

**LOW DISTORTION LINE DRIVER**
The AD826 can quickly be turned into a powerful, low distortion line driver (see Figure 41). In this arrangement the AD826 can comfortably drive a 75 Ω back-terminated cable, with a 5 MHz, 2 V p-p input; all of this while achieving the harmonic distortion performance outlined in the following table.

<table>
<thead>
<tr>
<th>Configuration</th>
<th>2nd Harmonic</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. No Load</td>
<td>−78.5 dBm</td>
</tr>
<tr>
<td>2. 150 Ω R_L Only</td>
<td>−63.8 dBm</td>
</tr>
<tr>
<td>3. 150 Ω R_L 7.5 Ω R_C</td>
<td>−70.4 dBm</td>
</tr>
</tbody>
</table>

In this application one half of the AD826 operates at a gain of 2.1 and supplies the current to the load, while the other provides the overall system gain of 2. This is important for two reasons: the first is to keep the bandwidth of both amplifiers the same, and the second is to preserve the AD826’s ability to operate from low supply voltages. R_C varies with the load and must be chosen to satisfy the following equation:

\[ R_C = MR_L \]

where M is defined by \((M + 1) G_S = G_D\) and \(G_D = \text{Driver’s Gain}, \ G_S = \text{System Gain}. \)

**Figure 41. Low Distortion Amplifier**
HIGH PERFORMANCE ADC BUFFER

Figure 42 is a schematic of a 12-bit high speed analog-to-digital converter. The AD826 dual op amp takes a single ended input and drives the AD872 A/D converter differentially, thus reducing 2nd harmonic distortion. Figure 43 is a FFT of a 1 MHz input, sampled at 10 MHz with a THD of −78 dB. The AD826 can be used to amplify low level signals so that the entire range of the converter is used. The ability of the AD826 to perform on a ±5 volt supply or even with a single 5 volts combined with its rapid settling time and ability to deliver high current to complicated loads make it a very good flash A/D converter buffer as well as a very useful general purpose building block.

Figure 42. A Differential Input Buffer for High Bandwidth ADCs

Figure 43. FFT, Buffered A/D Converter
OUTLINE DIMENSIONS

**Figure 44. 8-Lead Plastic Dual In-Line Package [PDIP]**
Narrow Body (N-8)
Dimensions shown in inches and (millimeters)

**Figure 45. 8-Lead Standard Small Outline Package [SOIC_N]**
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)

**ORDERING GUIDE**

<table>
<thead>
<tr>
<th>Model</th>
<th>Temperature Range</th>
<th>Package Description</th>
<th>Package Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD826AN</td>
<td>−40°C to +85°C</td>
<td>8-Lead PDIP</td>
<td>N-8</td>
</tr>
<tr>
<td>AD826ANZ</td>
<td>−40°C to +85°C</td>
<td>8-Lead PDIP</td>
<td>N-8</td>
</tr>
<tr>
<td>AD826AR</td>
<td>−40°C to +85°C</td>
<td>8-Lead SOIC_N</td>
<td>R-8</td>
</tr>
<tr>
<td>AD826AR-REEL</td>
<td>−40°C to +85°C</td>
<td>8-Lead SOIC_N</td>
<td>R-8</td>
</tr>
<tr>
<td>AD826AR-REEL7</td>
<td>−40°C to +85°C</td>
<td>8-Lead SOIC_N</td>
<td>R-8</td>
</tr>
<tr>
<td>AD826ARZ</td>
<td>−40°C to +85°C</td>
<td>8-Lead SOIC_N</td>
<td>R-8</td>
</tr>
<tr>
<td>AD826ARZ-REEL</td>
<td>−40°C to +85°C</td>
<td>8-Lead SOIC_N</td>
<td>R-8</td>
</tr>
</tbody>
</table>

1 Z = RoHS Compliant Part.
REVISION HISTORY

Changed Power Supply Bypassing Section to Power Supply Considerations Section .................................................. 10
Changes to Power Supply Considerations Section .................. 10
Updated Outline Dimensions ................................................. 14
Changes to Ordering Guide ................................................. 14