FEATURES

- Easy to use, single-ended-to-differential conversion
- Adjustable output common-mode voltage
- Externally adjustable gain
- Low harmonic distortion
  - $-94\, \text{dBc}$ SFDR at 5 MHz
  - $-85\, \text{dBc}$ SFDR at 20 MHz
- $-3\, \text{dB}$ bandwidth of 320 MHz, $G = +1$
- Fast settling to 0.01% of 16 ns
- Slew rate 1150 V/μs
- Fast overdrive recovery of 4 ns
- Low input voltage noise of 5 nV/√Hz
- 1 mV typical offset voltage
- Wide supply range $+3\, \text{V}$ to $±5\, \text{V}$
- Low power 90 mW on 5 V
- 0.1 dB gain flatness to 40 MHz
- Available in 8-Lead SOIC and MSOP packages

APPLICATIONS

- ADC drivers
- Single-ended-to-differential converters
- IF and baseband gain blocks
- Differential buffers
- Line drivers

GENERAL DESCRIPTION

The AD8138 is a major advancement over op amps for differential signal processing. The AD8138 can be used as a single-ended-to-differential amplifier or as a differential-to-differential amplifier. The AD8138 is as easy to use as an op amp and greatly simplifies differential signal amplification and driving. Manufactured on the proprietary ADI XFCB bipolar process, the AD8138 has a $-3\, \text{dB}$ bandwidth of 320 MHz and delivers a differential signal with the lowest harmonic distortion available in a differential amplifier. The AD8138 has a unique internal feedback feature that provides balanced output gain and phase matching, suppressing even order harmonics. The internal feedback circuit also minimizes any gain error that would be associated with the mismatches in the external gain setting resistors.

The differential output of the AD8138 helps balance the input to differential ADCs, maximizing the performance of the ADC. The AD8138 eliminates the need for a transformer with high performance ADCs, preserving the low frequency and dc information. The common-mode level of the differential output is adjustable by a voltage on the $V_{\text{OCM}}$ pin, easily level-shifting the input signals for driving single-supply ADCs. Fast overdrive recovery preserves sampling accuracy.

The AD8138 distortion performance makes it an ideal ADC driver for communication systems, with distortion performance good enough to drive state-of-the-art 10-bit to 16-bit converters at high frequencies. The high bandwidth and IP3 of the AD8138 also make it appropriate for use as a gain block in IF and baseband signal chains. The AD8138 offset and dynamic performance makes it well suited for a wide variety of signal processing and data acquisition applications.

The AD8138 is available in both SOIC and MSOP packages for operation over $-40°C$ to $+85°C$ temperatures.
COMPARABLE PARTS
View a parametric search of comparable parts.

EVALUATION KITS
- Universal Evaluation Board for Single Differential Amplifiers

DOCUMENTATION
Application Notes
- AN-0990: Terminating a Differential Amplifier in Single-Ended Input Applications
- AN-0992: Active Filter Evaluation Board for Differential Amplifiers
- AN-1026: High Speed Differential ADC Driver Design Considerations
- AN-1363: Meeting Biasing Requirements of Externally Biased RF/Microwave Amplifiers with Active Bias Controllers
- AN-584: Using the AD813X Differential Amplifier
- AN-589: Ways to Optimize the Performance of a Difference Amplifier
- AN-649: Using the Analog Devices Active Filter Design Tool

Data Sheet
- AD8138-DSCC: Military Data Sheet
- AD8138-EP: Enhanced Product Data Sheet
- AD8138: Low Distortion Differential ADC Driver Data Sheet

User Guides
- UG-474: Evaluation Board for Differential Amplifiers Offered in 8-Lead SOIC Packages
- UG-888: Evaluation Board for Differential Amplifiers Offered in 8-Lead MSOP Packages

TOOLS AND SIMULATIONS
- ADI DiffAmpCalc™
- AD8138 SPICE Macro-Model

REFERENCE DESIGNS
- CN0040
- CN0041
- CN0061

REFERENCE MATERIALS
Product Selection Guide
- High Speed Amplifiers Selection Table

Technical Articles
- Maximize Performance When Driving Differential ADCs

Tutorials
- MT-075: Differential Drivers for High Speed ADCs Overview
- MT-076: Differential Driver Analysis
- MT-218: Multiple Feedback Band-Pass Design Example
- MT-230: Noise Considerations in High Speed Converter Signal Chains

DESIGN RESOURCES
- AD8138 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS
View all AD8138 EngineerZone Discussions.

SAMPLE AND BUY
Visit the product page to see pricing options.

TECHNICAL SUPPORT
Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK
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12/00—Rev. A to Rev. B

9/99—Rev. 0 to Rev. A

3/99—Rev. 0: Initial Version
### SPECIFICATIONS

#### ±DIN TO ±OUT SPECIFICATIONS

At 25°C, \( V_S = \pm 5 \text{ V} \), \( V_{OCM} = 0 \), \( G = +1 \), \( R_{L, \text{dm}} = 500 \Omega \), unless otherwise noted. Refer to Figure 39 for test setup and label descriptions. All specifications refer to single-ended input and differential outputs, unless otherwise noted.

#### Table 1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DYNAMIC PERFORMANCE</strong></td>
<td>( V_{OUT} = 0.5 \text{ V p-p, } C_F = 0 \text{ pF} )</td>
<td>290</td>
<td>320</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>–3 dB Small Signal Bandwidth</td>
<td>( V_{OUT} = 0.5 \text{ V p-p, } C_F = 1 \text{ pF} )</td>
<td>225</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>Bandwidth for 0.1 dB Flatness</td>
<td>( V_{OUT} = 0.5 \text{ V p-p, } C_F = 0 \text{ pF} )</td>
<td>30</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>Large Signal Bandwidth</td>
<td>( V_{OUT} = 2 \text{ V p-p, } C_F = 0 \text{ pF} )</td>
<td>265</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>Slew Rate</td>
<td>( V_{OUT} = 2 \text{ V p-p, } C_F = 0 \text{ pF} )</td>
<td>1150</td>
<td></td>
<td></td>
<td>V/µs</td>
</tr>
<tr>
<td>Settling Time</td>
<td>( 0.01%, \ V_{OUT} = 2 \text{ V p-p, } C_F = 1 \text{ pF} )</td>
<td>16</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Overdrive Recovery Time</td>
<td>( V_N = 5 \text{ V to 0 V step, } G = +2 )</td>
<td>4</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

#### NOISE/HARMONIC PERFORMANCE\(^1\)

- Second Harmonic \( V_{OUT} = 2 \text{ V p-p, } 5 \text{ MHz, } R_L, dm = 800 \Omega \) | –94 | | | dBc |
- Third Harmonic \( V_{OUT} = 2 \text{ V p-p, } 5 \text{ MHz, } R_L, dm = 800 \Omega \) | –114 | | | dBc |
- IMD 20 MHz | | –77 | | dB |
- IP3 20 MHz | | 37 | | dBm |
- Voltage Noise (RTI) \( f = 100 \text{ kHz to 40 MHz} \) | | 5 | | nV/√Hz |
- Input Current Noise \( f = 100 \text{ kHz to 40 MHz} \) | | 2 | | pA/√Hz |

#### INPUT CHARACTERISTICS

- Offset Voltage | \( V_{OS, dm} = V_{OUT, dm}/2 \); \( V_{DIN+} = V_{DIN-} = V_{OCM} = 0 \text{ V} \) | –2.5 | ±1 | +2.5 | mV |
- Input Bias Current | \( T_{MIN} \text{ to } T_{MAX} \text{ variation} \) | 3.5 | 4 | 7 | µA/°C |
- Input Resistance | Differential | 6 | | | MΩ |
- Input Capacitance | Common mode | 3 | | | µF |
- Input Common-Mode Voltage | | 1 | | | pF |
- CMRR | \( \Delta V_{OUT, dm}/\Delta V_{IN, cm}; \Delta V_{IN, cm} = \pm 1 \text{ V} \) | –77 | | | dB |

#### OUTPUT CHARACTERISTICS

- Output Voltage Swing | Maximum \( \Delta V_{OUT} \); single-ended output | 7.75 | | | V p-p |
- Output Current | | 95 | | | mA |
- Output Balance Error | \( \Delta V_{OUT, cm}/\Delta V_{OUT, dm}; \Delta V_{OUT, dm} = 1 \text{ V} \) | –66 | | | dB |

\(^1\) Harmonic distortion performance is equal or slightly worse with higher values of \( R_{L, dm} \). See Figure 17 and Figure 18 for more information.
**V_{OCM} TO ±OUT SPECIFICATIONS**

At 25°C, V_{o} = ±5 V, V_{OCM} = 0, G = +1, R_{L, dm} = 500 Ω, unless otherwise noted. Refer to Figure 39 for test setup and label descriptions. All specifications refer to single-ended input and differential outputs, unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>DYNAMIC PERFORMANCE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>–3 dB Bandwidth</td>
<td></td>
<td>250</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>Slew Rate</td>
<td></td>
<td>330</td>
<td></td>
<td></td>
<td>V/µs</td>
</tr>
<tr>
<td>INPUT VOLTAGE NOISE (RTI)</td>
<td>f = 0.1 MHz to 100 MHz</td>
<td>17</td>
<td></td>
<td></td>
<td>nV/√Hz</td>
</tr>
<tr>
<td>DC PERFORMANCE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage Range</td>
<td></td>
<td>±3.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Input Resistance</td>
<td></td>
<td>200</td>
<td></td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td>Input Bias Current</td>
<td></td>
<td>0.5</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>V_{OCM} CMRR</td>
<td>( \Delta V_{OUT, dm}/\Delta V_{OCM}; \Delta V_{OCM} = ±1 V )</td>
<td>−75</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Gain</td>
<td>( \Delta V_{OUT, cm}/\Delta V_{OCM}; \Delta V_{OCM} = ±1 V )</td>
<td>0.9955</td>
<td>1</td>
<td>1.0045</td>
<td>V/V</td>
</tr>
<tr>
<td>POWER SUPPLY</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Range</td>
<td></td>
<td>±1.4</td>
<td>±5.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Quiescent Current</td>
<td></td>
<td>18</td>
<td>20</td>
<td>23</td>
<td>mA</td>
</tr>
<tr>
<td>Power Supply Rejection Ratio</td>
<td>T_{MIN} to T_{MAX} variation</td>
<td>40</td>
<td></td>
<td></td>
<td>μA/°C</td>
</tr>
<tr>
<td>OPERATING TEMPERATURE RANGE</td>
<td></td>
<td>−40</td>
<td></td>
<td>+85</td>
<td>°C</td>
</tr>
</tbody>
</table>
### ±DIN TO ±OUT SPECIFICATIONS

At 25°C, \( V_S = 5 \text{ V, } V_{DCM} = 2.5 \text{ V, } G = +1, \text{ and } R_{L,dm} = 500 \Omega \), unless otherwise noted. Refer to Figure 39 for test setup and label descriptions. All specifications refer to single-ended input and differential output, unless otherwise noted.

<table>
<thead>
<tr>
<th>Table 3.</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DYNAMIC PERFORMANCE</strong></td>
<td>−3 dB Small Signal Bandwidth</td>
<td>( V_{OUT} = 0.5 \text{ V p-p, } C_F = 0 \text{ pF} )</td>
<td>280</td>
<td>310</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{OUT} = 0.5 \text{ V p-p, } C_F = 1 \text{ pF} )</td>
<td>225</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td>Bandwidth for 0.1 dB Flatness</td>
<td>( V_{OUT} = 0.5 \text{ V p-p, } C_F = 0 \text{ pF} )</td>
<td>29</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td>Large Signal Bandwidth</td>
<td>( V_{OUT} = 2 \text{ V p-p, } C_F = 0 \text{ pF} )</td>
<td>265</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td>Slew Rate</td>
<td>( V_{OUT} = 2 \text{ V p-p, } C_F = 0 \text{ pF} )</td>
<td>950</td>
<td></td>
<td></td>
<td>V/µs</td>
</tr>
<tr>
<td></td>
<td>Settling Time</td>
<td>( V_{IN} = 2 \text{ V to 0 V step, } G = +2 )</td>
<td>16</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>Overdrive Recovery Time</td>
<td>( V_{IN} = 2.5 \text{ V to 0 V step, } G = +2 )</td>
<td>4</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td><strong>NOISE/HARMONIC PERFORMANCE</strong></td>
<td>Second Harmonic</td>
<td>( V_{OUT} = 2 \text{ V p-p, } 5 \text{ MHz, } R_L, dm = 800 \Omega )</td>
<td>−90</td>
<td></td>
<td></td>
<td>dBc</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{OUT} = 2 \text{ V p-p, } 20 \text{ MHz, } R_L, dm = 800 \Omega )</td>
<td>−79</td>
<td></td>
<td></td>
<td>dBc</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{OUT} = 2 \text{ V p-p, } 70 \text{ MHz, } R_L, dm = 800 \Omega )</td>
<td>−60</td>
<td></td>
<td></td>
<td>dBc</td>
</tr>
<tr>
<td></td>
<td>Third Harmonic</td>
<td>( V_{OUT} = 2 \text{ V p-p, } 5 \text{ MHz, } R_L, dm = 800 \Omega )</td>
<td>−100</td>
<td></td>
<td></td>
<td>dBc</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{OUT} = 2 \text{ V p-p, } 20 \text{ MHz, } R_L, dm = 800 \Omega )</td>
<td>−82</td>
<td></td>
<td></td>
<td>dBc</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{OUT} = 2 \text{ V p-p, } 70 \text{ MHz, } R_L, dm = 800 \Omega )</td>
<td>−53</td>
<td></td>
<td></td>
<td>dBc</td>
</tr>
<tr>
<td></td>
<td>IMD</td>
<td>20 MHz</td>
<td>−74</td>
<td></td>
<td></td>
<td>dBc</td>
</tr>
<tr>
<td></td>
<td>IP3</td>
<td>20 MHz</td>
<td>35</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td>Voltage Noise (RTI)</td>
<td>( f = 100 \text{ kHz to 40 MHz} )</td>
<td>5</td>
<td></td>
<td></td>
<td>nV/√Hz</td>
</tr>
<tr>
<td></td>
<td>Input Current Noise</td>
<td>( f = 100 \text{ kHz to 40 MHz} )</td>
<td>2</td>
<td></td>
<td></td>
<td>pA/√Hz</td>
</tr>
<tr>
<td><strong>INPUT CHARACTERISTICS</strong></td>
<td>Offset Voltage</td>
<td>( V_{OL,dm} = V_{OUT,dm}/2; V_{DIN+} = V_{DIN–} = V_{DCM} = 0 \text{ V} )</td>
<td>−2.5</td>
<td>±1</td>
<td>+2.5</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( T_{MIN} \text{ to } T_{MAX} \text{ variation} )</td>
<td>±4</td>
<td></td>
<td></td>
<td>µV/°C</td>
</tr>
<tr>
<td></td>
<td>Input Bias Current</td>
<td>( T_{MIN} \text{ to } T_{MAX} \text{ variation} )</td>
<td>3.5</td>
<td>7</td>
<td></td>
<td>µA/°C</td>
</tr>
<tr>
<td></td>
<td>Input Resistance</td>
<td>Differential</td>
<td>6</td>
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<td></td>
<td>MΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Common mode</td>
<td>3</td>
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<td></td>
<td>MΩ</td>
</tr>
<tr>
<td></td>
<td>Input Capacitance</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td></td>
<td>Input Common-Mode Voltage</td>
<td>( \Delta V_{OUT, dm}/\Delta V_{IN, cm}; \Delta V_{IN, cm} = 1 \text{ V} )</td>
<td>−0.3 to +3.2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>CMRR</td>
<td></td>
<td>−77</td>
<td>−70</td>
<td></td>
<td>dB</td>
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<tr>
<td><strong>OUTPUT CHARACTERISTICS</strong></td>
<td>Output Voltage Swing</td>
<td>Maximum ( \Delta V_{OUT}; \text{ single-ended output} )</td>
<td>2.9</td>
<td></td>
<td></td>
<td>V p-p</td>
</tr>
<tr>
<td></td>
<td>Output Current</td>
<td></td>
<td>95</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>Output Balance Error</td>
<td>( \Delta V_{OUT, cm}/\Delta V_{OUT, dm}; \Delta V_{OUT, dm} = 1 \text{ V} )</td>
<td>−65</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
</tbody>
</table>

1 Harmonic distortion performance is equal or slightly worse with higher values of \( R_L, dm \). See Figure 17 and Figure 18 for more information.
### V<sub>OCM</sub> TO ±OUT SPECIFICATIONS

At 25°C, V<sub>S</sub> = 5 V, V<sub>OCM</sub> = 2.5 V, G = +1, R<sub>L,dm</sub> = 500 Ω, unless otherwise noted. Refer to Figure 39 for test setup and label descriptions. All specifications refer to single-ended input and differential output, unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DYNAMIC PERFORMANCE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>−3 dB Bandwidth</td>
<td></td>
<td>220</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>Slew Rate</td>
<td></td>
<td>250</td>
<td></td>
<td></td>
<td>V/μs</td>
</tr>
<tr>
<td><strong>INPUT VOLTAGE NOISE (RTI)</strong></td>
<td>f = 0.1 MHz to 100 MHz</td>
<td>17</td>
<td></td>
<td></td>
<td>nV/√Hz</td>
</tr>
<tr>
<td>Input Voltage Range</td>
<td></td>
<td>1.0 to 3.8</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input Resistance</td>
<td></td>
<td>100</td>
<td></td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td>Input Offset Voltage</td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; = V&lt;sub&gt;OUT&lt;/sub&gt;, cm; V&lt;sub&gt;IN&lt;/sub&gt;+ = V&lt;sub&gt;IN&lt;/sub&gt;− = V&lt;sub&gt;OCM&lt;/sub&gt; = 0 V</td>
<td>-5</td>
<td>±1</td>
<td>+5</td>
<td>mV</td>
</tr>
<tr>
<td>Input Bias Current</td>
<td></td>
<td>0.5</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>V&lt;sub&gt;OCM&lt;/sub&gt; CMRR</td>
<td>∆V&lt;sub&gt;OUT&lt;/sub&gt;, cm/∆V&lt;sub&gt;OCM&lt;/sub&gt; ∆V&lt;sub&gt;OCM&lt;/sub&gt; = 2.5 V ±1 V</td>
<td>-70</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Gain</td>
<td>∆V&lt;sub&gt;OUT&lt;/sub&gt;, cm/∆V&lt;sub&gt;OCM&lt;/sub&gt; ∆V&lt;sub&gt;OCM&lt;/sub&gt; = 2.5 V ±1 V</td>
<td>0.9968</td>
<td>1</td>
<td>1.0032</td>
<td>V/V</td>
</tr>
<tr>
<td><strong>DC PERFORMANCE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Range</td>
<td></td>
<td>2.7</td>
<td></td>
<td>11</td>
<td>V</td>
</tr>
<tr>
<td>Quiescent Current</td>
<td>T&lt;sub&gt;MIN&lt;/sub&gt; to T&lt;sub&gt;MAX&lt;/sub&gt; variation</td>
<td>15</td>
<td>20</td>
<td>21</td>
<td>mA</td>
</tr>
<tr>
<td>Power Supply Rejection Ratio</td>
<td>∆V&lt;sub&gt;OUT&lt;/sub&gt;, cm/∆V&lt;sub&gt;i&lt;/sub&gt; ∆V&lt;sub&gt;i&lt;/sub&gt; = ±1 V</td>
<td>-90</td>
<td></td>
<td>-70</td>
<td>dB</td>
</tr>
<tr>
<td><strong>OPERATING TEMPERATURE RANGE</strong></td>
<td></td>
<td>-40</td>
<td></td>
<td>+85</td>
<td>°C</td>
</tr>
</tbody>
</table>
ABSOLUTE MAXIMUM RATINGS

Table 5.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Ratings</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>±5.5 V</td>
</tr>
<tr>
<td>(V_{\text{OCM}})</td>
<td>±(V_{\text{S}})</td>
</tr>
<tr>
<td>Internal Power Dissipation</td>
<td>550 mW</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>−40°C to +85°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>−65°C to +150°C</td>
</tr>
<tr>
<td>Lead Temperature (Soldering 10 sec)</td>
<td>300°C</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>150°C</td>
</tr>
</tbody>
</table>

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

\(\theta_{JA}\) is specified for the worst-case conditions, that is, \(\theta_{JA}\) is specified for the device soldered in a circuit board in still air.

Table 6.

<table>
<thead>
<tr>
<th>Package Type</th>
<th>(\theta_{JA})</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>8-Lead SOIC/4-Layer</td>
<td>121</td>
<td>°C/W</td>
</tr>
<tr>
<td>8-Lead MSOP/4-Layer</td>
<td>145</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

Maximum Power Dissipation

The maximum safe power dissipation in the AD8138 packages is limited by the associated rise in junction temperature (\(T_J\)) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8138. Exceeding a junction temperature of 150°C for an extended period can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package (\(P_d\)) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (\(V_S\)) times the quiescent current (\(I_S\)). The load current consists of the differential and common-mode currents flowing to the load, as well as currents flowing through the external feedback networks and internal common-mode feedback loop. The internal resistor tap used in the common-mode feedback loop places a negligible differential load on the output. RMS voltages and currents should be considered when dealing with ac signals.

Airflow reduces \(\theta_{JA}\). In addition, more metal directly in contact with the package leads from metal traces through holes, ground, and power planes reduces the \(\theta_{JA}\).

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 8-lead SOIC (121°C/W) and 8-lead MSOP (\(\theta_{JA} = 145°C/W\)) packages on a JEDEC standard 4-layer board. \(\theta_{JA}\) values are approximations.

![Figure 3. Maximum Power Dissipation vs. Temperature](image)

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.
### PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

**Figure 4. Pin Configuration**

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>−IN</td>
<td>Negative Input Summing Node.</td>
</tr>
<tr>
<td>2</td>
<td>$V_{OCM}$</td>
<td>Voltage applied to this pin sets the common-mode output voltage with a ratio of 1:1. For example, 1 V dc on $V_{OCM}$ sets the dc bias level on +OUT and −OUT to 1 V.</td>
</tr>
<tr>
<td>3</td>
<td>V+</td>
<td>Positive Supply Voltage.</td>
</tr>
<tr>
<td>4</td>
<td>+OUT</td>
<td>Positive Output. Note that the voltage at −DIN is inverted at +OUT (see Figure 42).</td>
</tr>
<tr>
<td>5</td>
<td>−OUT</td>
<td>Negative Output. Note that the voltage at +DIN is inverted at −OUT (see Figure 42).</td>
</tr>
<tr>
<td>6</td>
<td>V−</td>
<td>Negative Supply Voltage.</td>
</tr>
<tr>
<td>7</td>
<td>NC</td>
<td>No Connect.</td>
</tr>
<tr>
<td>8</td>
<td>+IN</td>
<td>Positive Input Summing Node.</td>
</tr>
</tbody>
</table>
TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, Gain = 1, R_G = R_F = R_L, dm = 499 V, T_A = 25°C; refer to Figure 39 for test setup.

Figure 5. Small Signal Frequency Response

Figure 6. Small Signal Frequency Response

Figure 7. 0.1 dB Flatness vs. Frequency

Figure 8. Large Signal Frequency Response

Figure 9. Large Signal Frequency Response

Figure 10. Small Signal Frequency Response for Various Gains
Figure 17. Harmonic Distortion vs. RLOAD

Figure 18. Harmonic Distortion vs. RLOAD

Figure 19. Intermodulation Distortion

Figure 20. Third-Order Intercept vs. Frequency

Figure 21. Large Signal Transient Response

Figure 22. Small Signal Transient Response
Figure 23. Large Signal Transient Response

VOUT, dm = 2 Vp-p
CF = 0 pF
VS = ±5 V
5ns

Figure 24. Large Signal Transient Response

CF = 0 pF
CF = 1 pF
VS = ±5 V
5ns

Figure 25. Settling Time

VOUT, dm
V+DIN
200 µV
VS = ±5 V
CF = 0 pF
CL = 20 pF
400 mV
5 ns

Figure 26. Output Overdrive

VOUT, dm
V+DIN
200 mV
VS = ±5 V
CF = 0 pF
CL = 5 pF
CL = 10 pF
CL = 20 pF
400 mV
2.5 ns

Figure 27. Large Signal Transient Response for Various Cap Loads (See Figure 40)

FREQUENCY (MHz)
CMRR (dB)
–20
–30
–40
–50
–60
–70
–80

Figure 28. CMRR vs. Frequency

VOUT, dm
VIN, cm
∆VOUT, dm/∆VIN, cm
200 mV
1V
4 ns

1 10 100 1k

01073-023
01073-024
01073-025
01073-026
01073-028
01073-029
**Figure 29. Output Balance Error vs. Frequency (See Figure 41)**

**Figure 30. PSRR vs. Frequency**

**Figure 31. Output Impedance vs. Frequency**

**Figure 32. Output Referred Differential Offset Voltage vs. Temperature**

**Figure 33. Input Bias Current vs. Temperature**

**Figure 34. Supply Current vs. Temperature**
Figure 35. \textit{V}_{\text{OM}} \textit{Frequency Response}

Figure 36. \textit{V}_{\text{OM}} \textit{Transient Response}

Figure 37. Current Noise (RTI)

Figure 38. Voltage Noise (RTI)
TEST CIRCUITS

Figure 39. Basic Test Circuit

Figure 40. Test Circuit for Cap Load Drive

Figure 41. Test Circuit for Output Balance
Differential voltage refers to the difference between two node voltages. For example, the output differential voltage (or equivalently output differential-mode voltage) is defined as

\[ V_{OUT, dm} = (V_{+OUT} - V_{-OUT}) \]

where \( V_{+OUT} \) and \( V_{-OUT} \) refer to the voltages at the +OUT and −OUT terminals with respect to a common reference.

Common-mode voltage refers to the average of two node voltages. The output common-mode voltage is defined as

\[ V_{OUT, cm} = \frac{(V_{+OUT} + V_{-OUT})}{2} \]

Balance is a measure of how well differential signals are matched in amplitude and exactly 180° apart in phase. Balance is most easily determined by placing a well-matched resistor divider between the differential voltage nodes and comparing the magnitude of the signal at the midpoint of the divider with the magnitude of the differential signal (see Figure 41). By this definition, output balance is the magnitude of the output common-mode voltage divided by the magnitude of the output differential mode voltage:

\[ Output\ Balance\ Error = \frac{V_{OUT, cm}}{V_{OUT, dm}} \]
THEORY OF OPERATION

The AD8138 differs from conventional op amps in that it has two outputs whose voltages move in opposite directions. Like an op amp, it relies on high open-loop gain and negative feedback to force these outputs to the desired voltages. The AD8138 behaves much like a standard voltage feedback op amp and makes it easy to perform single-ended-to-differential conversion, common-mode level-shifting, and amplification of differential signals. Also like an op amp, the AD8138 has high input impedance and low output impedance.

Previous differential drivers, both discrete and integrated designs, have been based on using two independent amplifiers and two independent feedback loops, one to control each of the outputs. When these circuits are driven from a single-ended source, the resulting outputs are typically not well balanced. Achieving a balanced output has typically required exceptional matching of the amplifiers and feedback networks.

DC common-mode level-shifting has also been difficult with previous differential drivers. Level-shifting has required the use of a third amplifier and feedback loop to control the output common-mode level. Sometimes the third amplifier has also been used to attempt to correct an inherently unbalanced circuit. Excellent performance over a wide frequency range has proven difficult with this approach.

The AD8138 uses two feedback loops to separately control the differential and common-mode output voltages. The differential feedback, set with external resistors, controls only the differential output voltage. The common-mode feedback controls only the common-mode output voltage. This architecture makes it easy to arbitrarily set the output common-mode level. It is forced, by internal common-mode feedback, to be equal to the voltage applied to $V_{OCM}$, without affecting the differential output voltage.

The AD8138 architecture results in outputs that are very highly balanced over a wide frequency range without requiring tightly matched external components. The common-mode feedback loop forces the signal component of the output common-mode voltage to be zeroed. The result is nearly perfectly balanced differential outputs of identical amplitude and exactly $180^\circ$ apart in phase.

ANALYZING AN APPLICATION CIRCUIT

The AD8138 uses high open-loop gain and negative feedback to force its differential and common-mode output voltages in such a way as to minimize the differential and common-mode error voltages. The differential error voltage is defined as the voltage between the differential inputs labeled $+IN$ and $-IN$ in Figure 42. For most purposes, this voltage can be assumed to be zero. Similarly, the difference between the actual output common-mode voltage and the voltage applied to $V_{OCM}$ can also be assumed to be zero. Starting from these two assumptions, any application circuit can be analyzed.

SETTING THE CLOSED-LOOP GAIN

Neglecting the capacitors $C_s$, the differential-mode gain of the circuit in Figure 42 can be determined to be described by

$$G = \frac{V_{OUT, \, dm}}{V_{IN, \, dm}} = \frac{R_F}{R_G}$$

This assumes the input resistors, $R_i$, and feedback resistors, $R_f$, on each side are equal.

ESTIMATING THE OUTPUT NOISE VOLTAGE

Similar to the case of a conventional op amp, the differential output errors (noise and offset voltages) can be estimated by multiplying the input referred terms, at $+IN$ and $-IN$, by the circuit noise gain. The noise gain is defined as

$$G_N = 1 + \frac{R_F}{R_G}$$

To compute the total output referred noise for the circuit of Figure 42, consideration must also be given to the contribution of the Resistors $R_s$ and $R_c$. Refer to Table 8 for the estimated output noise voltage densities at various closed-loop gains.

Table 8.

<table>
<thead>
<tr>
<th>Gain</th>
<th>$R_s$ (Ω)</th>
<th>$R_r$ (Ω)</th>
<th>Bandwidth −3 dB</th>
<th>Output Noise AD8138 Only</th>
<th>Output Noise AD8138 + $R_s$, $R_r$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>499</td>
<td>499</td>
<td>320 MHz</td>
<td>10 nV/√Hz</td>
<td>11.6 nV/√Hz</td>
</tr>
<tr>
<td>2</td>
<td>499</td>
<td>1.0 k</td>
<td>180 MHz</td>
<td>15 nV/√Hz</td>
<td>18.2 nV/√Hz</td>
</tr>
<tr>
<td>5</td>
<td>499</td>
<td>2.49 k</td>
<td>70 MHz</td>
<td>30 nV/√Hz</td>
<td>37.9 nV/√Hz</td>
</tr>
<tr>
<td>10</td>
<td>499</td>
<td>4.99 k</td>
<td>30 MHz</td>
<td>55 nV/√Hz</td>
<td>70.8 nV/√Hz</td>
</tr>
</tbody>
</table>
When using the AD8138 in gain configurations where \( R_f/R_G \) of one feedback network is unequal to \( R_f/R_G \) of the other network, there is a differential output noise due to input-referred voltage in the \( V_{OCM} \) circuitry. The output noise is defined in terms of the following feedback terms (refer to Figure 42):

\[
\beta_1 = \frac{R_G}{R_f + R_G}
\]

for −OUT to +IN loop, and

\[
\beta_2 = \frac{R_G}{R_f + R_G}
\]

for +OUT to −IN loop. With these defined,

\[
V_{nOUT, dm} = 2V_{nIN, V_{OCM}} \left( \frac{\beta_1 - \beta_2}{\beta_1 + \beta_2} \right)
\]

where \( V_{nOUT, dm} \) is the output differential noise, and \( V_{nIN, V_{OCM}} \) is the input-referred voltage noise in \( V_{OCM} \).

**THE IMPACT OF MISMATCHES IN THE FEEDBACK NETWORKS**

As previously mentioned, even if the external feedback networks \( (R_f/R_G) \) are mismatched, the internal common-mode feedback loop still forces the outputs to remain balanced. The amplitudes of the signals at each output remains equal and 180° out of phase. The input-to-output differential-mode gain varies proportionately to the feedback mismatch, but the output balance is unaffected.

Ratio matching errors in the external resistors result in a degradation of the ability of the circuit to reject input common-mode signals, much the same as for a four-resistor difference amplifier made from a conventional op amp.

In addition, if the dc levels of the input and output common-mode voltages are different, matching errors result in a small differential-mode output offset voltage. For the \( G = 1 \) case, with a ground referenced input signal and the output common-mode level set for 2.5 V, an output offset of as much as 25 mV (1% of the difference in common-mode levels) can result if 1% tolerance resistors are used. Resistors of 1% tolerance result in a worst-case input CMRR of about 40 dB, worst-case differential mode output offset of 25 mV due to 2.5 V level-shift, and no significant degradation in output balance error.

### CALCULATING THE INPUT IMPEDANCE OF AN APPLICATION

The effective input impedance of a circuit such as the one in Figure 42, at +DIN and −DIN, depends on whether the amplifier is being driven by a single-ended or differential signal source. For balanced differential input signals, the input impedance \( (R_{IN, dm}) \) between the inputs (+IN and −IN) is simply

\[
R_{IN, dm} = 2 \times R_G
\]

In the case of a single-ended input signal (for example if −DIN is grounded and the input signal is applied to +DIN), the input impedance becomes

\[
R_{IN, dm} = \left( \frac{R_G}{1 - \frac{R_f}{R_G}} \right)
\]

The input impedance of the circuit is effectively higher than it would be for a conventional op amp connected as an inverter because a fraction of the differential output voltage appears at the inputs as a common-mode signal, partially bootstrapping the voltage across the input resistor \( R_o \).

### INPUT COMMON-MODE VOLTAGE RANGE IN SINGLE-SUPPLY APPLICATIONS

The AD8138 is optimized for level-shifting, ground-referenced input signals. For a single-ended input, this would imply, for example, that the voltage at −DIN in Figure 42 would be 0 V when the negative power supply voltage of the amplifier (at \( V− \)) is also set to 0 V.

### SETTING THE OUTPUT COMMON-MODE VOLTAGE

The \( V_{OCM} \) pin of the AD8138 is internally biased at a voltage approximately equal to the midsupply point (average value of the voltages on \( V+ \) and \( V− \)). Relying on this internal bias results in an output common-mode voltage that is within about 100 mV of the expected value.

In cases where more accurate control of the output common-mode level is required, it is recommended that an external source, or resistor divider (made up of 10 kΩ resistors), be used. The output common-mode offset listed in the Specifications section assumes the \( V_{OCM} \) input is driven by a low impedance voltage source.

### DRIVING A CAPACITIVE LOAD

A purely capacitive load can react with the pin and bondwire inductance of the AD8138, resulting in high frequency ringing in the pulse response. One way to minimize this effect is to place a small capacitor across each of the feedback resistors. The added capacitance should be small to avoid destabilizing the amplifier. An alternative technique is to place a small resistor in series with the outputs of the amplifier, as shown in Figure 40.
LAYOUT, GROUNDING, AND BYPASSING

As a high speed device, the AD8138 is sensitive to the PCB environment in which it has to operate. Realizing its superior specifications requires attention to various details of good high speed PCB design.

The first requirement is for a good solid ground plane that covers as much of the board area around the AD8138 as possible. The only exception to this is that the two input pins (Pin 1 and Pin 8) should be kept a few millimeters from the ground plane, and ground should be removed from inner layers and the opposite side of the board under the input pins. This minimizes the stray capacitance on these nodes and helps preserve the gain flatness vs. frequency.

The power supply pins should be bypassed as close as possible to the device to the nearby ground plane. Good high frequency ceramic chip capacitors should be used. This bypassing should be done with a capacitance value of 0.01 µF to 0.1 µF for each supply. Further away, low frequency bypassing should be provided with 10 µF tantalum capacitors from each supply to ground.

The signal routing should be short and direct to avoid parasitic effects. Wherever there are complementary signals, a symmetrical layout should be provided to the extent possible to maximize the balance performance. When running differential signals over a long distance, the traces on the PCB should be close together or any differential wiring should be twisted together to minimize the area of the loop that is formed. This reduces the radiated energy and makes the circuit less susceptible to interference.
Transformers are among the oldest devices used to perform a single-ended-to-differential conversion (and vice versa). Transformers can also perform the additional functions of galvanic isolation, step-up or step-down of voltages, and impedance transformation. For these reasons, transformers always find uses in certain applications.

However, when driving the transformer in a single-ended manner, there is an imbalance at the output due to the parasitics inherent in the transformer. The primary (or driven) side of the transformer has one side at dc potential (usually ground), while the other side is driven. This can cause problems in systems that require good balance of the differential output signals of the transformer.

If the interwinding capacitance \( C_{\text{STRAY}} \) is assumed to be uniformly distributed, a signal from the driving source couples to the secondary output terminal that is closest to the driven side of the primary. On the other hand, no signal is coupled to the opposite terminal of the secondary because its nearest primary terminal is not driven (see Figure 43). The exact amount of this imbalance depends on the particular parasitics of the transformer, but is mostly a problem at higher frequencies.

The balance of a differential circuit can be measured by connecting an equal-valued resistive voltage divider across the differential outputs and then measuring the center point of the circuit with respect to ground. Since the two differential outputs are supposed to be of equal amplitude, but 180° opposite phase, there should be no signal present for perfectly balanced outputs.

The circuit in Figure 43 shows a Mini-Circuits® T1-6T transformer connected with its primary driven single-endedly and the secondary connected with a precision voltage divider across its terminals. The voltage divider is made up of two 500 \( \Omega \), 0.005% precision resistors. The voltage \( V_{\text{UNBAL}} \), which is also equal to the ac common-mode voltage, is a measure of how closely the outputs are balanced.

Figure 45 compares the transformer being driven single-endedly by a signal generator and being driven differentially using an AD8138. The top signal trace of Figure 45 shows the balance of the single-ended configuration, while the bottom shows the differentially driven balance response. The 100 MHz balance is 35 dB better when using the AD8138.
HIGH PERFORMANCE ADC DRIVING

The circuit in Figure 46 shows a simplified front-end connection for an AD8138 driving an AD9224, a 12-bit, 40 MSPS ADC. The ADC works best when driven differentially, which minimizes its distortion. The AD8138 eliminates the need for a transformer to drive the ADC and performs single-ended-to-differential conversion, common-mode level-shifting, and buffering of the driving signal.

The positive and negative outputs of the AD8138 are connected to the respective differential inputs of the AD9224 via a pair of 49.9 Ω resistors to minimize the effects of the switched-capacitor front end of the AD9224. For best distortion performance, it runs from supplies of ±5 V.

The AD8138 is configured with unity gain for a single-ended, input-to-differential output. The additional 23 Ω, 523 Ω total, at the input to −IN is to balance the parallel impedance of the 50 Ω source and its 50 Ω termination that drives the noninverting input.

The signal generator has a ground-referenced, bipolar output, that is, it drives symmetrically above and below ground.

Connecting V_{OCM} to the CML pin of the AD9224 sets the output common-mode of the AD8138 at 2.5 V, which is the mid-supply level for the AD9224. This voltage is bypassed by a 0.1 µF capacitor.

The full-scale analog input range of the AD9224 is set to 4 V p-p, by shorting the SENSE terminal to AVSS. This has been determined to be the scaling to provide minimum harmonic distortion.

For the AD8138 to swing at 4 V p-p, each output swings 2 V p-p while providing signals that are 180° out of phase. With a common-mode voltage at the output of 2.5 V, each AD8138 output swings between 1.5 V and 3.5 V.

A ground-referenced 4 V p-p, 5 MHz signal at D_{IN+} was used to test the circuit in Figure 46. When the combined-device circuit was run with a sampling rate of 20 MSPS, the spurious-free dynamic range (SFDR) was measured at −85 dBc.

![Figure 46. AD8138 Driving an AD9224, a 12-Bit, 40 MSPS ADC](image-url)
3 V OPERATION

The circuit in Figure 47 shows a simplified front-end connection for an AD8138 driving an AD9203, a 10-bit, 40 MSPS ADC that is specified to work on a single 3 V supply. The ADC works best when driven differentially to make the best use of the signal swing available within the 3 V supply. The appropriate outputs of the AD8138 are connected to the appropriate differential inputs of the AD9203 via a low-pass filter.

The AD8138 is configured for unity gain for a single-ended input to differential output. The additional 23 Ω at the input to −IN is to balance the impedance of the 50 Ω source and its 50 Ω termination that drives the noninverting input.

The signal generator has ground-referenced, bipolar output, that is, it can drive symmetrically above and below ground. Even though the AD8138 has ground as its negative supply, it can still function as a level-shifter with such an input signal.

The output common mode is raised up to midsupply by the voltage divider that biases VOCM. In this way, the AD8138 provides dc coupling and level-shifting of a bipolar signal, without inverting the input signal.

The low-pass filter between the AD8138 and the AD9203 provides filtering that helps to improve the signal-to-noise ratio (SNR). Lower noise can be realized by lowering the pole frequency, but the bandwidth of the circuit is lowered.

The circuit was tested with a −0.5 dBFS signal at various frequencies. Figure 48 shows a plot of the total harmonic distortion (THD) vs. frequency at signal amplitudes of 1 V and 2 V differential drive levels.

Figure 49 shows the signal-to-noise-and-distortion (SINAD) under the same conditions as above. For the smaller signal swing, the AD8138 performance is quite good, but its performance degrades when trying to swing too close to the supply rails.
OUTLINE DIMENSIONS

Figure 50. 8-Lead Standard Small Outline Package [SOIC] (R-8)
Dimensions shown in millimeters and (inches)

Figure 51. 8-Lead Mini Small Outline Package [MSOP] (RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

<table>
<thead>
<tr>
<th>Model</th>
<th>Temperature Range</th>
<th>Package Description</th>
<th>Package Option</th>
<th>Branding</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD8138AR</td>
<td>−40°C to +85°C</td>
<td>8-Lead SOIC</td>
<td>R-8</td>
<td></td>
</tr>
<tr>
<td>AD8138AR-REEL</td>
<td>−40°C to +85°C</td>
<td>8-Lead SOIC, 13” Tape and Reel</td>
<td>R-8</td>
<td></td>
</tr>
<tr>
<td>AD8138AR-REEL7</td>
<td>−40°C to +85°C</td>
<td>8-Lead SOIC, 7” Tape and Reel</td>
<td>R-8</td>
<td></td>
</tr>
<tr>
<td>AD8138ARZ</td>
<td>−40°C to +85°C</td>
<td>8-Lead SOIC</td>
<td>R-8</td>
<td></td>
</tr>
<tr>
<td>AD8138ARZ-RL</td>
<td>−40°C to +85°C</td>
<td>8-Lead SOIC, 13” Tape and Reel</td>
<td>R-8</td>
<td></td>
</tr>
<tr>
<td>AD8138ARZ-R7</td>
<td>−40°C to +85°C</td>
<td>8-Lead SOIC, 7” Tape and Reel</td>
<td>R-8</td>
<td></td>
</tr>
</tbody>
</table>
| AD8138ARM | −40°C to +85°C | 8-Lead MSOP | RM-8 | HBA
| AD8138ARM-REEL | −40°C to +85°C | 8-Lead MSOP, 13” Tape and Reel | RM-8 | HBA
| AD8138ARM-REEL7 | −40°C to +85°C | 8-Lead MSOP, 7” Tape and Reel | RM-8 | HBA
| AD8138ARMZ | −40°C to +85°C | 8-Lead MSOP | RM-8 | HBA#
| AD8138ARMZ-REEL | −40°C to +85°C | 8-Lead MSOP, 13” Tape and Reel | RM-8 | HBA#
| AD8138ARMZ-REEL7 | −40°C to +85°C | 8-Lead MSOP, 7” Tape and Reel | RM-8 | HBA# |

1 Z = RoHS Compliant Part. # denotes RoHS compliant part may be top or bottom marked.

REVISED: 6/02/11 
WITHDRAWN: 4/9/12 
REVISED: 11/19/13 
AD8138 
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