The AD8036 and AD8037 are wide bandwidth, low distortion clamping amplifiers. The AD8036 is unity gain stable. The AD8037 is stable at a gain of two or greater. These devices allow the designer to specify a high (V_{CH}) and low (V_{CL}) output clamp voltage. The output signal will clamp at these specified levels. Utilizing a unique patented CLAMPIN™ input clamp architecture, the AD8036 and AD8037 offer a 10× improvement in clamp performance compared to traditional output clamping devices. In particular, clamp error is typically 3 mV or less and distortion in the clamp region is minimized. This product can be used as a classical op amp or a clamp amplifier where a high and low output voltage are specified.

The AD8036 and AD8037, which utilize a voltage feedback architecture, meet the requirements of many applications which previously depended on current feedback amplifiers. The AD8036 and AD8037 exhibit an exceptionally fast and accurate pulse response (16 ns to 0.01%), extremely wide small-signal and large-signal bandwidths and ultralow distortion. The AD8036 achieves –66 dBc at 20 MHz, and 240 MHz small-signal and 195 MHz large-signal bandwidths. The AD8036 and AD8037’s recover from 2× clamp overdrive within 1.5 ns. These characteristics position the AD8036/AD8037 ideally for driving as well as buffering flash and high resolution ADCs.

In addition to traditional output clamp amplifier applications, the input clamp architecture supports the clamp levels as additional inputs to the amplifier. As such, in addition to static dc clamp levels, signals with speeds up to 240 MHz can be applied to the clamp pins. The clamp values can also be set to any value within the output voltage range provided that VH is greater than VL. Due to these clamp characteristics, the AD8036 and AD8037 can be used in nontraditional applications such as a full-wave rectifier, a pulse generator, or an amplitude modulator. These novel applications are only examples of some of the diverse applications which can be designed with input clamps.

The AD8036 is offered in chips, industrial (–40°C to +85°C) and military (–55°C to +125°C) package temperature ranges and the AD8037 in industrial. Industrial versions are available in plastic DIP and SOIC; MIL versions are packaged in cerdip.

**FEATURES**
- Superb Clamping Characteristics
  - 3 mV Clamp Error
  - 1.5 ns Overdrive Recovery
  - Minimized Nonlinear Clamping Region
- 240 MHz Clamp Input Bandwidth
  - ±3.9 V Clamp Input Range
- Wide Bandwidth
  - AD8036: AD8037
- Small Signal
  - 240 MHz: 270 MHz
- Large Signal (4 V p-p)
  - 195 MHz: 190 MHz
- Good DC Characteristics
  - 2 mV Offset
  - 10 μV/°C Drift
- Ultralow Distortion, Low Noise
  - –72 dBc typ @ 20 MHz
  - 4.5 nV/√Hz Input Voltage Noise
- High Speed
  - Slew Rate: 1500 V/μs
  - Settling: 10 ns to 0.1%, 16 ns to 0.01%
  - ±3 V to ±5 V Supply Operation

**APPLICATIONS**
- ADC Buffer
- IF/RF Signal Processing
- High Quality Imaging
- Broadcast Video Systems
- Video Amplifier
- Full Wave Rectifier

**PRODUCT DESCRIPTION**

The AD8036 and AD8037 are wide bandwidth, low distortion clamping amplifiers. The AD8036 is unity gain stable. The AD8036 is stable at a gain of two or greater. These devices allow the designer to specify a high (V_{CH}) and low (V_{CL}) output clamp voltage. The output signal will clamp at these specified levels. Utilizing a unique patented CLAMPIN™ input clamp architecture, the AD8036 and AD8037 offer a 10× improvement in clamp performance compared to traditional output clamping devices. In particular, clamp error is typically 3 mV or less and distortion in the clamp region is minimized. This product can be used as a classical op amp or a clamp amplifier where a high and low output voltage are specified.

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**FUNCTIONAL BLOCK DIAGRAM**

8-Lead Plastic DIP (N), Cerdip (Q), and SO Packages

**Figure 1. Clamp DC Accuracy vs. Input Voltage**

![Figure 1. Clamp DC Accuracy vs. Input Voltage](image-url)
### ELECTRICAL CHARACTERISTICS

**AD8036A**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>AD8036A</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
</tr>
<tr>
<td>DYNAMIC PERFORMANCE</td>
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<td></td>
</tr>
<tr>
<td>Bandwidth (–3 dB) Small Signal</td>
<td>$V_{OUT} \leq 0.4 \text{ V p-p}$</td>
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<td>Large Signal</td>
<td>$8036, V_{OUT} = 2.5 \text{ V p-p}; 8037, V_{OUT} = 3.5 \text{ V p-p}$</td>
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<tr>
<td>Bandwidth for 0.1 dB Flatness</td>
<td>$8036, R_L = 140 \Omega; 8037, R_L = 274 \Omega$</td>
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<tr>
<td>Slew Rate, Average +/-</td>
<td>$V_{OUT} = 4 \text{ V Step, 10–90%}$</td>
<td>900</td>
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<tr>
<td>Rise/Fall Time</td>
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<tr>
<td>Settling Time</td>
<td>$V_{OUT} = 0.5 \text{ V Step, 10–90%}$</td>
<td>2.6</td>
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<tr>
<td>Clamp Performance</td>
<td>$V_{CH}$ or $V_{CL}$</td>
<td>±3.3</td>
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<tr>
<td>Clamp Accuracy</td>
<td>$T_{MIN}-T_{MAX}$</td>
<td>±3</td>
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<tr>
<td>Clamp Nonlinearity Range</td>
<td>$V_{CH}$ or $V_{CL}$</td>
<td>±3</td>
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<tr>
<td>Clamp Input Bias Current</td>
<td>$8036, V_{H,L} = \pm 1 \text{ V}; 8037, V_{H,L} = \pm 0.5 \text{ V}$</td>
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<tr>
<td>Clamp Input Bandwidth –3 dB</td>
<td>$V_{CH}$ or $V_{CL}$</td>
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<tr>
<td>Clamp Overshoot Recovery</td>
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<td>DC PERFORMANCE</td>
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<tr>
<td>Offset Voltage Drift</td>
<td>$T_{MIN}-T_{MAX}$</td>
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<td>Input Bias Current</td>
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<tr>
<td>Input Offset Current</td>
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<td>Common-Mode Rejection Ratio</td>
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<td>Open-Loop Gain</td>
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<td>Input Capacitance</td>
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<td>OUTPUT CHARACTERISTICS</td>
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<td>Output Voltage Range</td>
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<td>Output Current</td>
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<tr>
<td>Short Circuit Current</td>
<td>$R_L = 150 \Omega$</td>
<td>240</td>
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</tbody>
</table>

### NOTES

1. See Max Ratings and Theory of Operation sections of data sheet.
2. See Max Ratings.
3. Nonlinearity is defined as the voltage delta between the set input clamp voltage ($V_{CH}$ or $V_{CL}$) and the voltage at which $V_{OUT}$ starts deviating from $V_{IN}$ (see Figure 73).
4. Measured at $A_v = 50$.
5. Measured with respect to the inverting input.

Specifications subject to change without notice.
ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
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<tr>
<td>Supply Voltage</td>
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<td>Voltage Swing x Bandwidth Product</td>
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<td>$</td>
<td>V_{H}-V_{IN}</td>
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<td>$</td>
<td>V_{L}-V_{IN}</td>
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<tr>
<td>Plastic DIP Package (N)</td>
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<tr>
<td>Small Outline Package (SO)</td>
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<tr>
<td>Input Voltage (Common Mode)</td>
<td>$\pm V_{S}$</td>
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<tr>
<td>Differential Input Voltage</td>
<td>$\pm 1.2$ V</td>
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<tr>
<td>Output Short Circuit Duration</td>
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</tr>
<tr>
<td>Storage Temperature Range N, R</td>
<td>–65°C to +85°C</td>
</tr>
<tr>
<td>Operating Temperature Range (A Grade)</td>
<td>–40°C to +85°C</td>
</tr>
<tr>
<td>Lead Temperature Range (Soldering 10 sec)</td>
<td>300°C</td>
</tr>
<tr>
<td>NOTE</td>
<td></td>
</tr>
<tr>
<td>1Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.</td>
<td></td>
</tr>
<tr>
<td>2Specification is for device in free air:</td>
<td></td>
</tr>
<tr>
<td>8-Lead Plastic DIP: $\theta_{JA} = 90$°C/W</td>
<td></td>
</tr>
<tr>
<td>8-Lead SOIC: $\theta_{JA} = 155$°C/W</td>
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</tr>
<tr>
<td>8-Lead Cerdip: $\theta_{JA} = 110$°C/W</td>
<td></td>
</tr>
</tbody>
</table>

METALIZATION PHOTO

Dimensions shown in inches and (nm).

Connect Substrate to –$V_{S}$.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by these devices is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Exceeding this limit temporarily may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

While the AD8036 and AD8037 are internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves.

Figure 2. Plot of Maximum Power Dissipation vs. Temperature

ORDERING GUIDE

<table>
<thead>
<tr>
<th>Model</th>
<th>Temperature Range</th>
<th>Package Description</th>
<th>Package Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD8036AN</td>
<td>–40°C to +85°C</td>
<td>Plastic DIP</td>
<td>N-8</td>
</tr>
<tr>
<td>AD8036AR</td>
<td>–40°C to +85°C</td>
<td>SOIC</td>
<td>SO-8</td>
</tr>
<tr>
<td>AD8036AR-REEL</td>
<td>–40°C to +85°C</td>
<td>13&quot; Tape and Reel</td>
<td>Q-8</td>
</tr>
<tr>
<td>AD8036AR-REEL7</td>
<td>–40°C to +85°C</td>
<td>7&quot; Tape and Reel</td>
<td>Q-8</td>
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<td>AD8036ACHIPS</td>
<td>–40°C to +85°C</td>
<td>Die</td>
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<td>AD8036-EB</td>
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<td>Evaluation Board</td>
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<td>AD8037AN</td>
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<td>N-8</td>
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<td>SO-8</td>
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<td>AD8037-EB</td>
<td>Plastic DIP</td>
<td>Evaluation Board</td>
<td>N-8</td>
</tr>
</tbody>
</table>

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8036/AD8037 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.
AD8036/AD8037

AD8036—Typical Characteristics

TPC 1. Noninverting Configuration, G = +1

TPC 2. Large Signal Transient Response; $V_O = 4\, \text{V}$ p-p, $G = +1$, $R_F = 140\, \Omega$

TPC 3. Small Signal Transient Response; $V_O = 400\, \text{mV}$ p-p, $G = +1$, $R_F = 140\, \Omega$

TPC 4. Noninverting Clamp Configuration, G = +1

TPC 5. Clamped Large Signal Transient Response (2× Overdrive); $V_O = 2\, \text{V}$ p-p, $G = +1$, $R_F = 140\, \Omega$, $V_H = +1\, \text{V}$, $V_L = -1\, \text{V}$

TPC 6. Clamped Small Signal Transient Response (2× Overdrive); $V_O = 400\, \text{mV}$ p-p, $G = +1$, $R_F = 140\, \Omega$, $V_H = +0.2\, \text{V}$, $V_L = -0.2\, \text{V}$
AD8037—Typical Characteristics

TPC 7. Noninverting Configuration, G = +2

TPC 10. Noninverting Clamp Configuration, G = +2

TPC 8. Large Signal Transient Response; $V_O = 4 \text{ V p-p}$, $G = +2$, $R_F = R_{IN} = 274 \Omega$

TPC 11. Clamped Large Signal Transient Response (2× Overdrive); $V_O = 2 \text{ V p-p}$, $G = +2$, $R_F = R_{IN} = 274 \Omega$, $V_H = +0.5 \text{ V}$, $V_L = -0.5 \text{ V}$

TPC 9. Small Signal Transient Response; $V_O = 400 \text{ mV p-p}$, $G = +2$, $R_F = R_{IN} = 274 \Omega$

TPC 12. Clamped Small Signal Transient Response (2× Overdrive); $V_O = 400 \text{ mV p-p}$, $G = +2$, $R_F = R_{IN} = 274 \Omega$, $V_H = +0.1 \text{ V}$, $V_L = -0.1 \text{ V}$
AD8036/AD8037

AD8036—Typical Characteristics

TPC 13. AD8036 Small Signal Frequency Response, $G = +1$

TPC 14. AD8036 0.1 dB Flatness, N Package (for R Package Add 20 $\Omega$ to $R_L$)

TPC 15. AD8036 Open-Loop Gain and Phase Margin vs. Frequency, $R_L = 100$ $\Omega$

TPC 16. AD8036 Small Signal −3 dB Bandwidth vs. $R_f$

TPC 17. AD8036 Large Signal Frequency Response, $G = +1$

TPC 18. AD8036 Clamp Input Bandwidth, $V_{HI}, V_L$
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TPC 20. AD8036 Harmonic Distortion vs. Frequency, \( R_L = 100 \, \Omega \)

TPC 21. AD8036 Third Order Intercept vs. Frequency

TPC 22. AD8036 Differential Gain and Phase Error, \( G = +1, R_L = 150 \, \Omega, F = 3.58 \, MHz \)

TPC 23. AD8036 Short-Term Settling Time to 0.01%, 2 V Step, \( G = +1, R_L = 100 \, \Omega \)

TPC 24. AD8036 Long-Term Settling Time, 2 V Step, \( G = +1, R_L = 100 \, \Omega \)
AD8036/AD8037

AD8037—Typical Characteristics

TPC 25. AD8037 Small Signal Frequency Response, G = +2

TPC 28. AD8037 Small Signal –3 dB Bandwidth vs. R_F, R_IN

TPC 26. AD8037 0.1 dB Flatness, N Package (for R Package Add 20 Ω to R_F)

TPC 29. AD8037 Large Signal Frequency Response, G = +2

TPC 27. AD8037 Open-Loop Gain and Phase Margin vs. Frequency, R_L = 100 Ω

TPC 30. AD8037 Clamp Input Bandwidth, V_H, V_L
TPC 31. AD8037 Harmonic Distortion vs. Frequency, $R_L = 500\ \Omega$

TPC 32. AD8037 Harmonic Distortion vs. Frequency, $R_L = 100\ \Omega$

TPC 33. AD8037 Third Order Intercept vs. Frequency

TPC 34. AD8037 Differential Gain and Phase Error
$G = +2, R_L = 150\ \Omega, F = 3.58\ \text{MHz}$

TPC 35. AD8037 Short-Term Settling Time to 0.01%, 2 V Step, $G = +2, R_L = 100\ \Omega$

TPC 36. AD8037 Long-Term Settling Time 2 V Step, $R_L = 100\ \Omega$
AD8036/AD8037—Typical Characteristics

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**TPC 40. AD8037 Noise vs. Frequency**

**TPC 38. AD8036 PSRR vs. Frequency**

**TPC 41. AD8037 PSRR vs. Frequency**

**TPC 39. AD8036 CMRR vs. Frequency**

**TPC 42. AD8037 CMRR vs. Frequency**
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TPC 44. AD8037 Output Resistance vs. Frequency

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AD8036/AD8037—Typical Characteristics

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TPC 57. AD8036 Clamp Overdrive (2×) Recovery

TPC 58. Harmonic Distortion as Output Approaches Clamp Voltage; \( V_o = 2 \text{ V p-p}, R_L = 100 \text{ }\Omega, f = 20 \text{ MHz} \)

TPC 59. AD8036/AD8037 Clamp Input Bias Current vs. Input Clamp Voltage

TPC 60. AD8037 Clamp Overdrive (2×) Recovery
AD8036/AD8037—Clamp Characteristics

TPC 61. AD8036 Clamp Settling (0.1%), \(V_H = +1 \, V\), \(V_L = -1 \, V\), 2× Overdrive

TPC 64. AD8037 Clamp Settling (0.1%), \(V_H = +0.5 \, V\), \(V_L = -0.5 \, V\), 2× Overdrive

TPC 62. AD8036 Clamp Recovery Settling Time (High), from 2× Overdrive to 0 V

TPC 65. AD8037 Clamp Recovery Settling Time (High), from 2× Overdrive to 0 V

TPC 63. AD8036 Clamp Recovery Settling Time (Low), from –2× Overdrive to 0 V

TPC 66. AD8037 Clamp Recovery Settling Time (Low), from –2× Overdrive to 0 V
THEORY OF OPERATION

General
The AD8036 and AD8037 are wide bandwidth, voltage feedback clamp amplifiers. Since their open-loop frequency response follows the conventional 6 dB/octave roll-off, their gain bandwidth product is basically constant. Increasing their closed-loop gain results in a corresponding decrease in small signal bandwidth. This can be observed by noting the bandwidth specification, between the AD8036 (gain of 1) and AD8037 (gain of 2). The AD8036/AD8037 typically maintain 65 degrees of phase margin. This high margin minimizes the effects of signal and noise peaking.

While the AD8036 and AD8037 can be used in either an inverting or noninverting configuration, the clamp function will only work in the noninverting mode. As such, this section shows connections only in the noninverting configuration. Applications that require an inverting configuration will be discussed in the Applications section. In applications that do not require clamping, Pins 5 and 8 (respectively V_L and V_H) may be left floating. See Input Clamp Amp Operation and Applications sections otherwise.

Feedback Resistor Choice
The value of the feedback resistor is critical for optimum performance on the AD8036 (gain +1) and less critical as the gain increases. Therefore, this section is specifically targeted at the AD8036.

At minimum stable gain (+1), the AD8036 provides optimum dynamic performance with R_F = 140 Ω. This resistor acts only as a parasitic suppressor against damped RF oscillations that can occur due to lead (input, feedback) inductance and parasitic capacitance. This value of R_F provides the best combination of wide bandwidth, low parasitic peaking, and fast settling time.

In fact, for the same reasons, a 100–130 Ω resistor should be placed in series with the positive input for other AD8036 noninverting configurations. The correct connection is shown in Figure 3.

Figure 3. Noninverting Operation
For general voltage gain applications, the amplifier bandwidth can be closely estimated as:

\[ f_{3 \text{dB}} = \frac{\omega_c}{2\pi} \left[ 1 + \left( \frac{R_F}{R_G} \right) \right] \]

This estimation loses accuracy for gains of +2/–1 or lower due to the amplifier’s damping factor. For these “low gain” cases, the bandwidth will actually extend beyond the calculated value (see Closed-Loop BW plots, TPCs 13 and 25).

Pulse Response
Unlike a traditional voltage feedback amplifier, where the slew speed is dictated by its front end dc quiescent current and gain bandwidth product, the AD8036 and AD8037 provide “on demand” current that increases proportionally to the input “step” signal amplitude. This results in slew rates (1200 V/µs) comparable to wideband current feedback designs. This, combined with relatively low input noise current (2.1 pA/√Hz), gives the AD8036 and AD8037 the best attributes of both voltage and current feedback amplifiers.

Large Signal Performance
The outstanding large signal operation of the AD8036 and AD8037 is due to a unique, proprietary design architecture. In order to maintain this level of performance, the maximum 350 V-MHz product must be observed, (e.g., @ 100 MHz, \( V_0 \leq 3.5 \text{ V p-p} \)).

Power Supply and Input Clamp Bypassing
Adequate power supply bypassing can be critical when optimizing the performance of a high frequency circuit. Inductance in the power supply leads can form resonant circuits that produce peaking in the amplifier’s response. In addition, if large current transients must be delivered to the load, then bypass capacitors (typically greater than 1 µF) will be required to provide the best settling time and lowest distortion. A parallel combination of at least 4.7 µF, and between 0.1 µF and 0.01 µF, is recommended. Some brands of electrolytic capacitors will require a small series damping resistor ~4.7 Ω for optimum results.

When the AD8036 and AD8037 are used in clamping mode, and a dc voltage is connected to clamp inputs V_H and V_L, a 0.1 µF bypassing capacitor is required between each input pin and ground in order to maintain stability.

Driving Capacitive Loads
The AD8036 and AD8037 were designed primarily to drive nonreactive loads. If driving loads with a capacitive component is desired, the best frequency response is obtained by the addition of a small series resistance as shown in Figure 4. The accompanying graph shows the optimum value for \( R_{\text{SERIES}} \) vs. capacitive load. It is worth noting that the frequency response of the circuit when driving large capacitive loads will be dominated by the passive roll-off of \( R_{\text{SERIES}} \) and \( C_L \). For capacitive loads of 6 pF or less, no \( R_{\text{SERIES}} \) is necessary.

Figure 4. Driving Capacitive Loads
INPUT CLAMPING AMPLIFIER OPERATION

The key to the AD8036 and AD8037’s fast, accurate clamp and amplifier performance is their unique patent pending CLAMPIN input clamp architecture. This new design reduces clamp errors by more than 10× over previous output clamp based circuits, as well as substantially increasing the bandwidth, precision and versatility of the clamp inputs.

Figure 6 is an idealized block diagram of the AD8036 connected as a unity gain voltage follower. The primary signal path comprises A1 (a 1200 V/µs, 240 MHz high voltage gain, differential to single-ended amplifier) and A2 (a G = +1 high current gain output buffer). The AD8037 differs from the AD8036 only in that A1 is optimized for closed-loop gains of two or greater.

The CLAMPIN section is comprised of comparators CH and CL, which drive switch S1 through a decoder. The unity-gain buffers in series with +VIN, VH, and VL inputs isolate the input pins from the comparators and S1 without reducing bandwidth or precision.

The two comparators have about the same bandwidth as A1 (240 MHz), so they can keep up with signals within the useful bandwidth of the AD8036. To illustrate the operation of the CLAMPIN circuit, consider the case where VH is referenced to 1 V, VL is open, and the AD8036 is set for a gain of +1, by connecting its output back to its inverting input through the recommended 140 Ω feedback resistor. Note that the main signal path always operates closed loop, since the CLAMPIN circuit only affects A1’s noninverting input.

If a 0 V to 2 V voltage ramp is applied to the AD8036’s +VIN for the connection just described, VOUT should track +VIN perfectly up to 1 V, then should limit at exactly 1 V as +VIN continues to 2 V.

In practice, the AD8036 comes close to this ideal behavior. As the +VIN input voltage ramps from zero to 1 V, the output of the high limit comparator CH starts in the off state, as does the output of CL. When +VIN just exceeds VIN (ideally, by say 1 µV, practically by about 18 mV), CH changes state, switching S1 from “A” to “B” reference level. Since the + input of A1 is now connected to VH, further increases in +VIN have no effect on the AD8036’s output voltage. In short, the AD8036 is now operating as a unity-gain buffer for the VH input, as any variation in VH for VH > 1 V, will be faithfully reproduced at VOUT.

Operation of the AD8036 for negative input voltages and negative clamp levels on VL is similar, with comparator CL controlling S1. Since the comparators see the voltage on the +VIN pin as their common reference level, then the voltage VH and VL are defined as “High” or “Low” with respect to +VIN. For example, if +VIN is set to zero volts, VH is open, and VL is +1 V, comparator CL will switch S1 to “C,” so the AD8036 will buffer the voltage on VL and ignore +VIN.

The performance of the AD8036 and AD8037 closely matches the ideal just described. The comparator’s threshold extends from 60 mV inside the clamp window defined by the voltages on VL and VH to 60 mV beyond the window’s edge. Switch S1 is implemented with current steering, so that A1’s +input makes a continuous transition from say, VIN to VH as the input voltage traverses the comparator’s input threshold from 0.9 V to 1.0 V for VH = 1.0 V.

The practical effect of these nonidealities is to soften the transition from amplification to clamping modes, without compromising the absolute clamp limit set by the CLAMPIN circuit. Figure 7 is a graph of VOUT vs. VIN for the AD8036 and a typical output clamp amplifier. Both amplifiers are set for G = +1 and VH = 1 V.

The worst case error between VOUT (ideally clamped) and VOUT (actual) is typically 18 mV times the amplifier closed-loop gain. This occurs when VIN equals VH (or VL). As VIN goes above and/or below this limit, VOUT will settle to within 5 mV of the ideal value.

In contrast, the output clamp amplifier’s transfer curve typically will show some compression starting at an input of 0.8 V, and can have an output voltage as far as 200 mV over the clamp limit. In addition, since the output clamp in effect causes the amplifier to operate open loop in clamp mode, the amplifier’s output impedance will increase, potentially causing additional errors.

The AD8036’s and AD8037’s CLAMPIN input clamp architecture works only for noninverting or follower applications and, since it operates on the input, the clamp voltage levels VH and VL, and input error limits will be multiplied by the amplifier’s

Figure 5. Recommended RSERIES vs. Capacitive Load

Figure 6. AD8036/AD8037 Clamp Amp System
closed-loop gain at the output. For instance, to set an output limit of ±1 V for an AD8037 operating at a gain of 3.0, \( V_H \) and \( V_L \) would need to be set to +0.333 V and -0.333 V, respectively. The only restriction on using the AD8036’s and AD8037’s +\( V_{IN} \), \( V_L \), \( V_H \) pins as inputs is that the maximum voltage difference between +\( V_{IN} \) and \( V_H \) or \( V_L \) should not exceed 6.3 V, and all three voltages be within the supply voltage range. For example, if \( V_L \) is set at -3 V, then \( V_{IN} \) should not exceed +3.3 V.

**AD8036/AD8037 APPLICATIONS**

The AD8036 and AD8037 use a unique input clamping circuit to perform the clamping function. As a result, they provide the clamping function better than traditional output clamping devices and provide additional flexibility to perform other unique applications.

There are, however, some restrictions on circuit configurations; and some calculations need to be performed in order to figure the clamping level, as a result of clamping being performed at the input stage.

The major restriction on the clamping feature of the AD8036/AD8037 is that clamping occurs only when using the amplifiers in the noninverting mode. To clamp in an inverting circuit, an additional inverting gain stage is required. Another restriction is that \( V_H \) be greater than \( V_L \) and that each be within the output voltage range of the amplifier (±3.9 V). \( V_H \) can go below ground and \( V_L \) can go above ground as long as \( V_H \) is kept higher than \( V_L \).

**Unity Gain Clamping**

The simplest circuit for calculating the clamp levels is a unity gain follower as shown in Figure 8. In this case, the AD8036 should be used since it is compensated for noninverting unity gain.

This circuit will clamp at an upper voltage set by \( V_H \) (the voltage applied to Pin 8) and a lower voltage set by \( V_L \) (the voltage applied to Pin 5).

**Clamping with Gain**

Figure 9 shows an AD8037 configured for a noninverting gain of two. The AD8037 is used in this circuit since it is compensated for gains of two or greater and provides greater bandwidth. In this case, the high clamping level at the output will occur at

\[
2 \times V_H \text{ and the low clamping level at the output will be } 2 \times V_L. 
\]

The equations governing the output clamp levels in circuits configured for noninverting gain are:

\[
V_{CH} = G \times V_H \\
V_{CL} = G \times V_L
\]

where:

- \( V_{CH} \) is the high output clamping level
- \( V_{CL} \) is the low output clamping level
- \( G \) is the gain of the amplifier configuration
- \( V_H \) is the high input clamping level (Pin 8)
- \( V_L \) is the low input clamping level (Pin 5)

*Amplifier offset is assumed to be zero.
Clamping with an Offset
Some op amp circuits are required to operate with an offset voltage. These are generally configured in the inverting mode where the offset voltage can be summed as one of the inputs. Since AD8036/AD8037 clamping does not function in the inverting mode, it is not possible to clamp with this configuration.

Figure 10 shows a noninverting configuration of an AD8037 that provides clamping and also has an offset. The circuit shows the AD8037 as a driver for an AD9002, an 8-bit, 125 MSPS A/D converter and illustrates some of the considerations for using an AD8037 with offset and clamping.

The usable input signal swing of the AD9002 is 2 V p-p. This is centered about the –1 V offset making the usable signal range from 0 V to –2 V. It is desirable to clamp the input signal so that it goes no more than 100 mV outside of this range in either direction. Thus, the high clamping level should be set at +0.1 V and the low clamping level should be set at –2.1 V as seen at the input of the AD9002 (output of AD8037).

Because the clamping is done at the input stage of the AD8037, the clamping level as seen at the output is affected by not only the gain of the circuit as previously described, but also by the offset. Thus, in order to obtain the desired clamp levels, $V_{H}$ must be biased at +0.55 V while $V_{L}$ must be biased at –0.55 V.

The clamping levels as seen at the output can be calculated by the following:

$$V_{CH} = V_{OFF} + G \times V_{H}$$
$$V_{CL} = V_{OFF} + G \times V_{L}$$

Where $V_{OFF}$ is the offset voltage that appears at the output. The resistors used to generate the voltages for $V_{H}$ and $V_{L}$ should be kept to a minimum in order to reduce errors due to clamp bias current. This current is dependent on $V_{H}$ and $V_{L}$ (see TPC 59) and will create a voltage drop across whatever resistance is in series with each clamp input. This extra error voltage is multiplied by the closed-loop gain of the amplifier and can be substantial, especially in high closed-loop gain configurations. A 0.1 μF bypass capacitor should be placed between input clamp pins $V_{H}$ and $V_{L}$ and ground to ensure stable operation.

The 1N5712 Schottky diode is used for protection from forward biasing the substrate diode in the AD9002 during power-up transients.

Programmable Pulse Generator
The AD8036/AD8037’s clamp output can be set accurately and has a well controlled flat level. This along with wide bandwidth and high slew rate make them very well suited for programmable level pulse generators.

Figure 11 is a schematic for a pulse generator that can directly accept TTL generated timing signals for its input and generate pulses at the output up to 24 V p-p with 2500 V/μs slew rate.

The output levels can be programmed to anywhere in the range –12 V to +12 V.
The circuit uses an AD8037 operating at a gain of two with an AD811 to boost the output to the ±12 V range. The AD811 was chosen for its ability to operate with ±15 V supplies and its high slew rate.

R1 and R2 act as a level shifter to make the TTL signal levels be approximately symmetrical above and below ground. This ensures that both the high and low logic levels will be clamped by the AD8037. For well controlled signal levels in the output pulse, the high and low output levels should result from the clamping action of the AD8037 and not be controlled by either the high or low logic levels passing through a linear amplifier. For good rise and fall times at the output pulse, a logic family with high speed edges should be used.

The high logic levels are clamped at two times the voltage at \( V_H \), while the low logic levels are clamped at two times the voltage at \( V_L \). The output of the AD8037 is amplified by the AD811 operating at a gain of 5. The overall gain of 10 will cause the high output level to be 10 times the voltage at \( V_H \), and the low output level to be 10 times the voltage at \( V_L \).

### High Speed, Full-Wave Rectifier

The clamping inputs are additional inputs to the input stage of the op amp. As such they have an input bandwidth comparable to the amplifier inputs and lend themselves to some unique functions when they are driven dynamically.

Figure 12 is a schematic for a full-wave rectifier, sometimes called an absolute value generator. It works well up to 20 MHz and can operate at significantly higher frequencies with some degradation in performance. The distortion performance is significantly better than diode based full-wave rectifiers, especially at high frequencies.
Thus for either positive or negative input signals, the output is unity times the absolute value of the input signal. The circuit can be easily configured to produce the negative absolute value of the input by applying the input to $V_H$ instead of $V_L$.

The circuit can get to within about 40 mV of ground during the time when the input crosses zero. This voltage is fixed over a wide frequency range and is a result of the switching between the conventional op amp input and the clamp input. But because there are no diodes to rapidly switch from forward to reverse bias, the performance far exceeds that of diode based full wave rectifiers.

The 40 mV offset mentioned can be removed by adding an offset to the circuit. A 27.4 kΩ input resistor to the inverting input will have a gain of 0.01, while changing the gain of the circuit by only 1%. A plus or minus 4 V dc level (depending on the polarity of the rectifier) into this resistor will compensate for the offset.

Full wave rectifiers are useful in many applications including AM signal detection, high frequency ac voltmeters and various arithmetic operations.

**Amplitude Modulator**

In addition to being able to be configured as an amplitude demodulator (AM detector), the AD8037 can also be configured as an amplitude modulator as shown in Figure 15.

The positive input of the AD8037 is driven with a square wave of sufficient amplitude to produce clamping action at both the high and low levels. This is the higher frequency carrier signal. The modulation signal is applied to both the input of a unity gain inverting amplifier and to $V_L$, the lower clamping input. $V_H$ is biased at 0.5 V dc.

To understand the circuit operation, it is helpful to first consider a simpler circuit. If both $V_L$ and $V_H$ were dc biased at −0.5 V and the carrier and modulation inputs driven as above, the output would be a 2 V p-p square wave at the carrier frequency riding on a waveform at the modulating frequency. The inverting input (modulation signal) is creating a varying offset to the 2 V p-p square wave at the output. Both the high and low levels clamp at twice the input levels on the clamps because the noise gain of the circuit is two.

When $V_L$ is driven by the modulation signal instead of being held at a dc level, a more complicated situation results. The resulting waveform is composed of a upper envelope and a lower envelope with the carrier square wave in between. The upper and lower envelope waveforms are $180°$ out of phase as in a typical AM waveform.

The upper envelope is produced by the upper clamp level being offset by the waveform applied to the inverting input. This offset is the opposite polarity of the input waveform because of the inverting configuration.

The lower envelope is produced by the sum of two effects. First, it is offset by the waveform applied to the inverting input as in the case of the simplified circuit above. The polarity of this offset is in the same direction as the upper envelope. Second, the output is driven in the opposite direction of the offset at twice the offset voltage by the modulation signal being applied to $V_L$. This results from the noise gain being equal to two, and since there is no inversion in this connection, it is opposite polarity from the offset.

The result at the output for the lower envelope is the sum of these two effects, which produces the lower envelope of an amplitude modulated waveform. See Figure 16.

The depth of modulation can be modified in this circuit by changing the amplitude of the modulation signal. This changes the amplitude of the upper and lower envelope waveforms.

The modulation depth can also be changed by changing the dc bias applied to $V_H$. In this case the amplitudes of the upper and lower envelope waveforms stay constant, but the spacing between them changes. This alters the ratio of the envelope amplitude to the amplitude of the overall waveform.
Layout Considerations
The specified high speed performance of the AD8036 and AD8037 requires careful attention to board layout and component selection. Proper RF design techniques and low pass parasitic component selection are mandatory.

The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance path. The ground plane should be removed from the area near the input pins to reduce stray capacitance.

Chip capacitors should be used for supply and input clamp bypassing (see Figure 17). One end should be connected to the ground plane and the other within 1/8 inch of each power and clamp pin. An additional large (0.47 µF–10 µF) tantalum electrolytic capacitor should be connected in parallel, though not necessarily so close, to supply current for fast, large signal changes at the output.

The feedback resistor should be located close to the inverting input pin in order to keep the stray capacitance at this node to a minimum. Capacitance variations of less than 1 pF at the inverting input will significantly affect high speed performance.

Stripline design techniques should be used for long signal traces (greater than about 1 inch). These should be designed with a characteristic impedance of 50 Ω or 75 Ω and be properly terminated at each end.

Evaluation Board
An evaluation board for both the AD8036 and AD8037 is available that has been carefully laid out and tested to demonstrate that the specified high speed performance of the device can be realized. For ordering information, please refer to the Ordering Guide.

The layout of the evaluation board can be used as shown or serve as a guide for a board layout.

Table I.

<table>
<thead>
<tr>
<th>Component</th>
<th>AD8036A Gain</th>
<th>AD8037A Gain</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>+1</td>
<td>+2</td>
</tr>
<tr>
<td>R_F</td>
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<td>R_C</td>
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<td>R_O (Nominal)</td>
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<td>49.9 Ω</td>
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<tr>
<td>R_S</td>
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<td>R_T (Nominal)</td>
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<td>49.9 Ω</td>
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<tr>
<td>Small Signal BW (MHz)</td>
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<td>90</td>
</tr>
</tbody>
</table>

Figure 17. Noninverting Configurations for Evaluation Boards