 FEATURES
Low Cost, Wide Bandwidth, Low Noise
Bandwidth: 240 MHz
Pulse Width Modulation: 500 ps
Rise Time/Fall Time: 1.5 ns
Input Current Noise: 3.0 pA/√Hz @ 100 MHz
Total Input RMS Noise: 26.5 nA to 100 MHz
Wide Dynamic Range
Optical Sensitivity: -36 dBm @ 155.52 Mbps
Peak Input Current: ±350 µA
Differential Outputs
Low Power: 5 V @ 25 mA
Wide Operating Temperature Range: -40°C to +85°C

APPLICATIONS
Fiber Optic Receivers: SONET/SDH, FDDI, Fibre Channel
Stable Operation with High Capacitance Detectors
Low Noise Preamplifiers
Single-Ended to Differential Conversion
I-to-V Converters

PRODUCT DESCRIPTION
The AD8015 is a wide bandwidth, single supply transimpedance amplifier optimized for use in a fiber optic receiver circuit. It is a complete, single chip solution for converting photodiode current into a differential voltage output. The 240 MHz bandwidth enables AD8015 application in FDDI receivers and SONET/SDH receivers with data rates up to 155 M bps. This high bandwidth supports data rates beyond 300 M bps. The differential outputs drive ECL directly, or can drive a comparator/fiber optic post amplifier.

In addition to fiber optic applications, this low cost, silicon alternative to GaAs-based transimpedance amplifiers is ideal for systems requiring a wide dynamic range preamplifier or single-ended to differential conversion. The IC can be used with a standard ECL power supply (-5.2 V) or a PECL (+5 V) power supply; the common mode at the output is ECL compatible. The AD8015 is available in die form, or in an 8-pin SOIC package.

Figure 1. Differential/Single-Ended Transimpedance vs. Frequency

Figure 2. Noise vs. Frequency (SO-8 Package with Added Capacitance)
COMPARABLE PARTS
View a parametric search of comparable parts.

DOCUMENTATION
Data Sheet
- AD8015: Wideband/Differential Output Transimpedance Amplifier Data Sheet

REFERENCE MATERIALS
Informational
- Optical and High Speed Networking ICs

DESIGN RESOURCES
- AD8015 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS
View all AD8015 EngineerZone Discussions.

SAMPLE AND BUY
Visit the product page to see pricing options.

TECHNICAL SUPPORT
Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK
Submit feedback for this data sheet.

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# AD8015 - SPECIFICATIONS

(50 Package @ T_A = +25°C and V_S = +5 V, unless otherwise noted)

## Dynamic Performance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>AD8015AR</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>3 dB</td>
<td>180</td>
</tr>
<tr>
<td>Pulse Width Modulation</td>
<td>10 µA to 200 µA Peak</td>
<td>500</td>
</tr>
<tr>
<td>Rise and Fall Time</td>
<td>10% to 90%</td>
<td>500</td>
</tr>
<tr>
<td>Settling Time</td>
<td>3%, 0.5 V Diff Output Step</td>
<td>1.5</td>
</tr>
</tbody>
</table>

## Input

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>AD8015AR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linear Input Current Range</td>
<td>±2.5%, Nonlinearity</td>
<td>±25</td>
</tr>
<tr>
<td>Max Input Current Range</td>
<td>Saturation</td>
<td>±200</td>
</tr>
<tr>
<td>Optical Sensitivity</td>
<td>155 M bps, Avg Power</td>
<td>-36</td>
</tr>
<tr>
<td>Input Stray Capacitance</td>
<td>Die, by Design</td>
<td>0.2</td>
</tr>
<tr>
<td>Input Bias Voltage</td>
<td>SOIC, by Design</td>
<td>0.4</td>
</tr>
</tbody>
</table>

## Noise

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>AD8015AR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Current Noise</td>
<td>Die, Single Ended at P_OUT, or Differential (P_OUT-N_OUT), C_STRAY = 0.3 pF</td>
<td>3.0</td>
</tr>
<tr>
<td>Total Input RMS Noise</td>
<td>f = 100 MHz</td>
<td>25.5</td>
</tr>
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</table>

## Transfer Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>AD8015AR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transresistance</td>
<td>Single Ended</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td>Differential</td>
<td>16</td>
</tr>
<tr>
<td>Power Supply</td>
<td>Single Ended</td>
<td>37.0</td>
</tr>
<tr>
<td></td>
<td>Differential</td>
<td>40</td>
</tr>
</tbody>
</table>

## Output

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>AD8015AR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Differential Offset</td>
<td>From Positive Supply</td>
<td>-1.5</td>
</tr>
<tr>
<td></td>
<td>Positive Input Current, R_L = ∞</td>
<td>1.0</td>
</tr>
<tr>
<td></td>
<td>Positive Input Current, R_L = 50 Ω</td>
<td>600</td>
</tr>
<tr>
<td>Output Impedance</td>
<td></td>
<td>40</td>
</tr>
</tbody>
</table>

## Power Supply

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>AD8015AR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Range</td>
<td>T_MIN to T_MAX</td>
<td>±4.5</td>
</tr>
<tr>
<td></td>
<td>Single Supply</td>
<td>±2.25</td>
</tr>
<tr>
<td></td>
<td>Dual Supply</td>
<td>25</td>
</tr>
</tbody>
</table>

## Absolute Maximum Ratings

1. Supply Voltage (+V_S to -V_S). .................... 12 V
2. Internal Power Dissipation  .................... 0.9 Watts
3. Storage Temperature Range .................... -65°C to +125°C
4. Operating Temperature Range (T_MIN to T_MAX)  ............... -40°C to +85°C
5. Maximum Junction Temperature  .................... +165°C
6. Lead Temperature Range (Soldering 10 sec)  ............... +300°C

## Notes

1. Settling Time is defined as the time elapsed from the application of a perfect step input to the time when the output has entered and remained within a specified error band symmetrical about the final value. This parameter includes propagation delay, slew time, overload recovery, and linear settling times.
2. Specifications subject to change without notice.

## ORDERING GUIDE

<table>
<thead>
<tr>
<th>Model</th>
<th>Temperature Range</th>
<th>Package</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD8015AR</td>
<td>-40°C to +85°C</td>
<td>8-Pin</td>
<td>SO-8</td>
</tr>
<tr>
<td>AD8015ACHIPS</td>
<td>-40°C to +85°C</td>
<td>Die</td>
<td>SO-8</td>
</tr>
</tbody>
</table>

## Caution

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8015 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.
FIBER OPTIC RECEIVER APPLICATIONS
In a fiber optic receiver, the photodiode can be placed from the I\textsubscript{IN} pin to either the positive or negative supply. The AD8015 converts the current from the photodiode to a differential voltage in these applications. The voltage at the V\textsubscript{BYP} pin is \(\approx 1.8\) V below the positive supply. This node must be bypassed with a capacitor (C1 in Figures 3 and 4 below) to the signal ground. If large levels of power supply noise exist, then connecting C1 to \(+V\textsubscript{S}\) is recommended for improved noise immunity. For optimum performance, choose C1 such that \(C_1 > 1/(2\pi \times 1000 \times f_{MIN})\); where \(f_{MIN}\) is the minimum useful frequency in Hz.

PHOTODIODE REFERRED TO POSITIVE SUPPLY
Figure 3 shows the AD8015 used in a circuit where the photodiode is referred to the positive supply. The back bias voltage on the photodiode is \(\approx 1.8\) V. This method of referring the photodiode provides greater power supply noise immunity (PSRR) than referring the photodiode to the negative supply. The signal path is referred to the positive rail, and the photodiode capacitance is not modulated by high frequency noise that may exist on the negative rail.

PHOTODIODE REFERRED TO NEGATIVE SUPPLY
Figure 4 shows the AD8015 used in a circuit where the photodiode is referred to the negative supply. This results in a larger back bias voltage than when referring the photodiode to the positive supply. The larger back bias voltage on the photodiode decreases the photodiode’s capacitance thereby increasing its bandwidth. The R2, C2 network shown in Figure 4 is added to decouple the photodiode to the positive supply. This improves PSRR.

FIBER OPTIC SYSTEM NOISE PERFORMANCE
The AD8015 maintains 26.5 nA referred to input (RTI) to 100 MHz. Calculations below translate this specification into minimum power level and bit error rate specifications for SONET and FDDI systems. The dominant sources of noise are: 10 kΩ feedback resistor current noise, input bipolar transistor base current noise, and input voltage noise.

The AD8015 has dielectrically isolated devices and bond pads that minimize stray capacitance at the I\textsubscript{IN} pin. Input voltage noise is negligible at lower frequencies, but can become the dominant noise source at high frequencies due to I\textsubscript{IN} pin stray capacitance. Minimizing the stray capacitance at the I\textsubscript{IN} pin is critical to maintaining low noise levels at high frequencies. The pins surrounding the I\textsubscript{IN} pin (Pins 1 and 3) have no internal connection and should be left unconnected in an application. This minimizes I\textsubscript{IN} pin package capacitance. It is best to have no ground plane or metal runs near Pins 1, 2, and 3 and to minimize capacitance at the I\textsubscript{IN} pin.

The AD8015AR (8-pin SOIC) I\textsubscript{IN} pin total stray capacitance is 0.4 pF without the photodiode. Photodiodes used for SONET or FDDI systems typically add 0.3 pF, resulting in roughly 0.7 pF total stray capacitance.
SONET OC-3 SENSITIVITY ANALYSIS

OC-3 Minimum Bandwidth = 0.7 × 155 MHz = 110 MHz

Total Current Noise = (π/2) × 26.5 nA
= 42 nA (assuming single pole response)

To maintain a BER < 1 × 10⁻¹⁰ (1 error per 10 billion bits):

Minimum current level needs to be > 13 × Total Current Noise
= 541 nA (peak)
Asume a typical photodiode current/power conversion ratio
= 0.85 A/W

Sensitivity (minimum power level) = 541/0.85 nW
= 637 nW (peak)
= -32.0 dBm (peak)
= -35.0 dBm (average)

The SONET OC-3 specification allows for a minimum power level of -31 dBm peak, or -34 dBm average. Using the AD8015 provides 1 dB margin.

FDDI SENSITIVITY ANALYSIS

FDDI Minimum Bandwidth = 0.7 × 125 MHz = 88 MHz

Total Current Noise = (π/2) × 88 MHz × 26.5 nA
= 39 nA (assuming single pole response)

To maintain a BER < 2.5 × 10⁻¹⁰ (1 error per 4 billion bits):

Minimum current level needs to be > 12.6 × Total Current Noise
= 492 nA (peak)
Asume a typical photodiode current/power conversion ratio
= 0.85 A/W

Sensitivity (minimum power level) = 492/0.85 nW
= 579 nW (peak)
= -32.4 dBm (peak)
= -35.4 dBm (average)

The FDDI specification allows for a minimum power level of -28 dBm peak, or -31 dBm average. Using the AD8015 provides 4.4 dB margin.

THEORY OF OPERATION

The simplified schematic is shown in Figure 5. Q1 and Q3 make up the input stage, with Q3 running at 300 µA and Q1 running at 2.7 mA. Q3 runs essentially as a grounded emitter. A large capacitor (0.01 µF) placed from V BYP to the positive supply shorts out the noise of R17, R21, and Q16. The first stage of the amplifier (Q3, R2, Q4, and C1) functions as an integrator, integrating current into the I IN pin. The integrator drives a differential stage (Q5, Q6, R5, R3, and R4) with gains of +3 and -3. The differential stage then drives emitter followers (Q41, Q42, Q60 and Q61). The positive output of the differential stage provides the feedback by driving R FB. The differential outputs are buffered using Q7 and Q8.

The bandwidth of the AD8015 is set to within ±20% of the nominal value, 240 MHz, by factory trimming R5 to 60 Ω. The following formula describes the AD8015 bandwidth:

\[ \text{Bandwidth} = \frac{1}{2 \pi \times C1 \times R_{FB} \times (R5 + 2 \times R_F / R4)} \]

where \( R_F \) (of Q5 and Q6) = 9 Ω each, constant over temperature, and \( R_{FB} / R4 = 43.5 \) constant over temperature.

The bandwidth equation simplifies, and the bandwidth depends only on the value of C1:

\[ \text{Bandwidth} = \frac{1}{2 \pi \times 3393 \times C1}. \]

![Figure 5. AD8015 Simplified Schematic](image-url)
Figure 6. Differential Output vs. Input Current

Figure 7. Single-Ended Output vs. Input Current

Figure 8. Bandwidth vs. Temperature

Figure 9. Gain vs. Frequency

Figure 10. Group Delay vs. Frequency

Figure 11. Differential Gain vs. Supply
APPLICATION
155 Mbps Fiber Optic Receiver
The AD8015 and AD807 can be used together for a complete 155 Mbps Fiber Optic Receiver (Transimpedance Amplifier, Post Amplifier with Signal Detect Output, and Clock Recovery and Data Retiming) as shown in Figure 16.

The PIN diode front end is connected to a single mode, 1300 nm laser source. The PIN diode has 3.3 V reverse bias, 0.8 A/W responsivity, 0.7 pF capacitance, and 2.5 GHz bandwidth.

The AD8015 outputs (P_OUT and N_OUT) drive a differential, constant impedance (50 Ω) low-pass π filter with a 3 dB cutoff of 100 MHz. The outputs of the low-pass filter are ac coupled to the AD807 inputs (PIN and NIN). The AD807 PLL damping factor is set at 10 using a 0.22 µF capacitor.

The entire circuit was enclosed in a shielded box. Table I summarizes results of tests performed using a 2^23–1 PRN sequence, and varying the average power at the PIN diode.

The circuit acquires and maintains lock with an average input power as low as -39.25 dBm.
Figure 16. 155 Mbps Fiber Optic Receiver Schematic

Table I. AD8015, AD807 Fiber Optic Receiver Circuit: Output Bit Error Rate & Output Jitter vs. Average Input Power

<table>
<thead>
<tr>
<th>Average Optical Input Power (dBm)</th>
<th>Output Bit Error Rate</th>
<th>Output Jitter (ps rms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-6.4</td>
<td>Loses Lock</td>
<td></td>
</tr>
<tr>
<td>-6.45</td>
<td>$1.2 \times 10^{-2}$</td>
<td></td>
</tr>
<tr>
<td>-6.50</td>
<td>$7.5 \times 10^{-3}$</td>
<td></td>
</tr>
<tr>
<td>-6.60</td>
<td>$9.4 \times 10^{-4}$</td>
<td></td>
</tr>
<tr>
<td>-6.70</td>
<td>$1 \times 10^{-14}$</td>
<td></td>
</tr>
<tr>
<td>-7.0 to -36.00</td>
<td>$1 \times 10^{-14}$</td>
<td>$&lt; 40$</td>
</tr>
<tr>
<td>-35.50</td>
<td>$3.0 \times 10^{-12}$</td>
<td>$&lt; 40$</td>
</tr>
<tr>
<td>-36.50</td>
<td>$4.8 \times 10^{-10}$</td>
<td></td>
</tr>
<tr>
<td>-37.00</td>
<td>$2.8 \times 10^{-8}$</td>
<td></td>
</tr>
<tr>
<td>-37.50</td>
<td>$8.2 \times 10^{-7}$</td>
<td></td>
</tr>
<tr>
<td>-38.00</td>
<td>$1.3 \times 10^{-5}$</td>
<td></td>
</tr>
<tr>
<td>-38.50</td>
<td>$1.1 \times 10^{-4}$</td>
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</tr>
<tr>
<td>-39.00</td>
<td>$1.0 \times 10^{-3}$</td>
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<tr>
<td>-39.1</td>
<td>$1.3 \times 10^{-3}$</td>
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<td>-39.20</td>
<td>$1.9 \times 10^{-3}$</td>
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<tr>
<td>-39.25</td>
<td>$2.2 \times 10^{-3}$</td>
<td></td>
</tr>
<tr>
<td>-39.30</td>
<td>Loses Lock</td>
<td></td>
</tr>
</tbody>
</table>
**AD8015**

**AC COUPLED PHOTODIODE APPLICATION FOR IMPROVED DYNAMIC RANGE**

AC coupling the photodiode current input to the AD8015 (Figure 17) extends fiber optic receiver overload by 3 dB while sacrificing only 1 dB of sensitivity (increasing receiver dynamic range by 2 dB). This application results in typical overload of -4 dBm, and typical sensitivity of -35 dBm. AC coupling the input also results in improved pulse width modulation performance.

Careful attention to minimize parasitic capacitance at the AD8015 input (from the photodetector input), $R_{AC}$ and $C_{AC}$ are critical for sensitivity performance in this application. Note that $C_{AC}$ of 0.01 µF was chosen for a low frequency cutoff equal to 2.2 kHz.

![Figure 17. AC Coupled Photodiode Application for Improved Dynamic Range](image)

**OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).

8-Lead Small Outline IC Package (SO-8)