FEATURES
12-Bit Monolithic A/D Converter
66 kHz Throughput Rate
12 µs Conversion Time
3 µs On-Chip Track/Hold Amplifier
Low Power
Power Save Mode: 2 mW typ
Normal Operation: 25 mW typ
70 dB SNR
Fast Data Access Time: 57 ns
Small 24-Lead SOIC and 0.3" DIP Packages

APPLICATIONS
Battery Powered Portable Systems
Digital Signal Processing
Speech Recognition and Synthesis
High Speed Modems
Control and Instrumentation

GENERAL DESCRIPTION
The AD7880 is a high speed, low power, 12-bit A/D converter which operates from a single +5 V supply. It consists of a 3 µs track/hold amplifier, a 12 µs successive-approximation ADC, versatile interface logic and a multiple-input-range circuit. The part also includes a power save feature.

An internal resistor network allows the part to accept both unipolar and bipolar input signals while operating from a single +5 V supply. Fast bus access times and standard control inputs ensure easy interfacing to modern microprocessors and digital signal processors.

The AD7880 features a total throughput time of 15 µs and can convert full power signals up to 33 kHz with a sampling frequency of 66 kHz.

In addition to the traditional dc accuracy specifications such as linearity, full-scale and offset errors, the AD7880 is also fully specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio.

The AD7880 is fabricated in Analog Devices' Linear Compatible CMOS (LC²MOS) process, a mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in a 24-pin, 0.3 inch-wide, plastic or hermetic dual-in-line package (DIP) as well as a small 24-lead SOIC package.

PRODUCT HIGHLIGHTS
1. Fast Conversion Time.
   12 µs conversion time and 3 µs acquisition time allow for large input signal bandwidth. This performance is ideally suited for applications in areas such as telecommunications, audio, sonar and radar signal processing.

2. Low Power Consumption.
   2 mW power consumption in the power-down mode makes the part ideally suited for portable, hand held, battery powered applications.

3. Multiple Input Ranges.
   The part features three user-determined input ranges, 0 V to +5 V, 0 V to 10 V and ±5 V. These unipolar and bipolar ranges are achieved with a 5 V only power supply.
## AD7880- SPECIFICATIONS

(V<sub>DD</sub> = +5 V ± 5%, V<sub>REF</sub> = V<sub>DD</sub>, AGND = DGND = 0 V, f<sub>CLKIN</sub> = 2.5 MHz, MODE = V<sub>DD</sub> unless otherwise noted. All Specifications T<sub>MIN</sub> to T<sub>MAX</sub> unless otherwise noted.)

### Dynamic Performance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>B Versions&lt;sup&gt;1&lt;/sup&gt;</th>
<th>C Versions&lt;sup&gt;1&lt;/sup&gt;</th>
<th>Units</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signal-to-Noise Ratio (SNR)</td>
<td>70</td>
<td>70</td>
<td>dB min</td>
<td>Typically SNR is 72 dB</td>
</tr>
<tr>
<td>Total Harmonic Distortion (THD)</td>
<td>-80</td>
<td>-80</td>
<td>dB typ</td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; = 1 kHz Sine Wave, f&lt;sub&gt;SAMPLE&lt;/sub&gt; = 66 kHz</td>
</tr>
<tr>
<td>Peak Harmonic or Spurious Noise</td>
<td>-80</td>
<td>-80</td>
<td>dB typ</td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; = 1 kHz Sine Wave, f&lt;sub&gt;SAMPLE&lt;/sub&gt; = 66 kHz</td>
</tr>
<tr>
<td>Intermodulation Distortion (IMD)</td>
<td>-80</td>
<td>-80</td>
<td>dB typ</td>
<td>fa = 0.983 kHz, fb = 1.05 kHz, f&lt;sub&gt;SAMPLE&lt;/sub&gt; = 66 kHz</td>
</tr>
<tr>
<td>Second Order Terms</td>
<td>-80</td>
<td>-80</td>
<td>dB typ</td>
<td>fa = 0.983 kHz, fb = 1.05 kHz, f&lt;sub&gt;SAMPLE&lt;/sub&gt; = 66 kHz</td>
</tr>
<tr>
<td>Third Order Terms</td>
<td>-80</td>
<td>-80</td>
<td>dB typ</td>
<td>fa = 0.983 kHz, fb = 1.05 kHz, f&lt;sub&gt;SAMPLE&lt;/sub&gt; = 66 kHz</td>
</tr>
</tbody>
</table>

### DC Accuracy

<table>
<thead>
<tr>
<th>Parameter</th>
<th>B Versions&lt;sup&gt;1&lt;/sup&gt;</th>
<th>C Versions&lt;sup&gt;1&lt;/sup&gt;</th>
<th>Units</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>12</td>
<td>12</td>
<td>Bits</td>
<td>All DC ACCURACY Specifications Apply for the Three Analog Input Ranges</td>
</tr>
<tr>
<td>Integral Nonlinearity</td>
<td>±1</td>
<td>±1</td>
<td>LSB max</td>
<td>Guaranteed Monotonic</td>
</tr>
<tr>
<td>Differential Nonlinearity</td>
<td>±1</td>
<td>±1</td>
<td>LSB max</td>
<td></td>
</tr>
<tr>
<td>Full-Scale Error</td>
<td>±15</td>
<td>±5</td>
<td>LSB max</td>
<td></td>
</tr>
<tr>
<td>Bipolar Zero Error</td>
<td>±10</td>
<td>±5</td>
<td>LSB max</td>
<td></td>
</tr>
<tr>
<td>Unipolar Offset Error</td>
<td>±5</td>
<td>±5</td>
<td>LSB max</td>
<td></td>
</tr>
</tbody>
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### Analog Input

<table>
<thead>
<tr>
<th>Parameter</th>
<th>B Versions&lt;sup&gt;1&lt;/sup&gt;</th>
<th>C Versions&lt;sup&gt;1&lt;/sup&gt;</th>
<th>Units</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage Ranges</td>
<td>0 to V&lt;sub&gt;REF&lt;/sub&gt;</td>
<td>0 to V&lt;sub&gt;REF&lt;/sub&gt;</td>
<td>Volts</td>
<td>See Figure 5</td>
</tr>
<tr>
<td>Input Range</td>
<td>0 to 2 V&lt;sub&gt;REF&lt;/sub&gt;</td>
<td>0 to 2 V&lt;sub&gt;REF&lt;/sub&gt;</td>
<td>Volts</td>
<td>See Figure 6</td>
</tr>
<tr>
<td>Input Resistance</td>
<td>10</td>
<td>10</td>
<td>MΩ min</td>
<td>0 to V&lt;sub&gt;REF&lt;/sub&gt; Range</td>
</tr>
<tr>
<td></td>
<td>5/12</td>
<td>5/12</td>
<td>kΩ min/max</td>
<td>8 kΩ typical: 0 to 2 V&lt;sub&gt;REF&lt;/sub&gt; Range</td>
</tr>
<tr>
<td>Input Capacitance, C&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>±10</td>
<td>±10</td>
<td>µF max</td>
<td></td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>10</td>
<td>pF max</td>
<td></td>
</tr>
</tbody>
</table>

### Reference Input

<table>
<thead>
<tr>
<th>Parameter</th>
<th>B Versions&lt;sup&gt;1&lt;/sup&gt;</th>
<th>C Versions&lt;sup&gt;1&lt;/sup&gt;</th>
<th>Units</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;REF&lt;/sub&gt; (For Specified Performance)</td>
<td>5</td>
<td>5</td>
<td>V</td>
<td>±5%: Normally V&lt;sub&gt;REF&lt;/sub&gt; = V&lt;sub&gt;DD&lt;/sub&gt; (See Reference Input Section)</td>
</tr>
<tr>
<td>I&lt;sub&gt;REF&lt;/sub&gt;</td>
<td>1.5</td>
<td>1.5</td>
<td>mA max</td>
<td></td>
</tr>
<tr>
<td>Nominal Reference Range</td>
<td>2.5/V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>2.5/V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>V min/max</td>
<td>See Figure 3 for Degradation in Performance Down to 2.5 V</td>
</tr>
</tbody>
</table>

### Logic Inputs

<table>
<thead>
<tr>
<th>Parameter</th>
<th>B Versions&lt;sup&gt;1&lt;/sup&gt;</th>
<th>C Versions&lt;sup&gt;1&lt;/sup&gt;</th>
<th>Units</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input High Voltage, V&lt;sub&gt;INH&lt;/sub&gt;</td>
<td>2.4</td>
<td>2.4</td>
<td>V min</td>
<td></td>
</tr>
<tr>
<td>Input Low Voltage, V&lt;sub&gt;INL&lt;/sub&gt;</td>
<td>0.8</td>
<td>0.8</td>
<td>V max</td>
<td></td>
</tr>
<tr>
<td>Input Current, I&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>±10</td>
<td>±10</td>
<td>µA max</td>
<td></td>
</tr>
<tr>
<td>Input Capacitance, C&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>10</td>
<td>10</td>
<td>pF max</td>
<td></td>
</tr>
</tbody>
</table>

### Mode Input

<table>
<thead>
<tr>
<th>Parameter</th>
<th>B Versions&lt;sup&gt;1&lt;/sup&gt;</th>
<th>C Versions&lt;sup&gt;1&lt;/sup&gt;</th>
<th>Units</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input High Voltage, V&lt;sub&gt;INH&lt;/sub&gt;</td>
<td>4</td>
<td>4</td>
<td>V min</td>
<td></td>
</tr>
<tr>
<td>Input Low Voltage, V&lt;sub&gt;INL&lt;/sub&gt;</td>
<td>1</td>
<td>1</td>
<td>V max</td>
<td></td>
</tr>
<tr>
<td>Input Current, I&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>±125</td>
<td>±125</td>
<td>µA max</td>
<td></td>
</tr>
<tr>
<td>Input Capacitance, C&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>10</td>
<td>10</td>
<td>pF max</td>
<td></td>
</tr>
</tbody>
</table>

### Logic Outputs

<table>
<thead>
<tr>
<th>Parameter</th>
<th>B Versions&lt;sup&gt;1&lt;/sup&gt;</th>
<th>C Versions&lt;sup&gt;1&lt;/sup&gt;</th>
<th>Units</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output High Voltage, V&lt;sub&gt;OH&lt;/sub&gt;</td>
<td>4.0</td>
<td>4.0</td>
<td>V min</td>
<td>I&lt;sub&gt;SOURCE&lt;/sub&gt; = 400 µA</td>
</tr>
<tr>
<td>Output Low Voltage, V&lt;sub&gt;OL&lt;/sub&gt;</td>
<td>0.4</td>
<td>0.4</td>
<td>V max</td>
<td>I&lt;sub&gt;SINK&lt;/sub&gt; = 1.6 mA</td>
</tr>
<tr>
<td>Floating-State Leakage Current</td>
<td>±10</td>
<td>±10</td>
<td>µA max</td>
<td></td>
</tr>
<tr>
<td>Floating-State Output Capacitance</td>
<td>10</td>
<td>10</td>
<td>pF max</td>
<td></td>
</tr>
</tbody>
</table>

### Conversion

<table>
<thead>
<tr>
<th>Parameter</th>
<th>B Versions&lt;sup&gt;1&lt;/sup&gt;</th>
<th>C Versions&lt;sup&gt;1&lt;/sup&gt;</th>
<th>Units</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conversion Time</td>
<td>12</td>
<td>12</td>
<td>µs max</td>
<td>f&lt;sub&gt;CLKIN&lt;/sub&gt; = 2.5 MHz</td>
</tr>
<tr>
<td>Track/Hold Acquisition Time</td>
<td>3</td>
<td>3</td>
<td>µs max</td>
<td></td>
</tr>
</tbody>
</table>

### Power Requirements

<table>
<thead>
<tr>
<th>Parameter</th>
<th>B Versions&lt;sup&gt;1&lt;/sup&gt;</th>
<th>C Versions&lt;sup&gt;1&lt;/sup&gt;</th>
<th>Units</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>+5</td>
<td>+5</td>
<td>V nom</td>
<td>±5% for Specified Performance</td>
</tr>
<tr>
<td>I&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>7.5</td>
<td>7.5</td>
<td>mA max</td>
<td>Typically 4 mA; M ODE = V&lt;sub&gt;DD&lt;/sub&gt;</td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>10</td>
<td>mA max</td>
<td>Typically 5 mA; M ODE = V&lt;sub&gt;DD&lt;/sub&gt;</td>
</tr>
<tr>
<td>Power Save Mode @ +25°C</td>
<td>750</td>
<td>750</td>
<td>µA max</td>
<td>Logic Inputs @ 0 V or V&lt;sub&gt;DD&lt;/sub&gt;; M ODE = 0 V</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>mA max</td>
<td>Logic Inputs @ 0 V or V&lt;sub&gt;DD&lt;/sub&gt;; M ODE = 0 V</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>37.5</td>
<td>37.5</td>
<td>mW max</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 5 V; Typically 20 mW; M ODE = V&lt;sub&gt;DD&lt;/sub&gt;</td>
</tr>
<tr>
<td></td>
<td>50</td>
<td>50</td>
<td>mW max</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 5 V; Typically 25 mW; M ODE = V&lt;sub&gt;DD&lt;/sub&gt;</td>
</tr>
<tr>
<td></td>
<td>3.75</td>
<td>3.75</td>
<td>mW max</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 5 V; Typically 2 mW; M ODE = 0 V</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>5</td>
<td>mW max</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 5 V; Typically 2.5 mW; M ODE = 0 V</td>
</tr>
</tbody>
</table>

### Notes

1. Temperature ranges are as follows: B/C Versions, –40°C to +85°C.
2. VIN = 0 to V<sub>REF</sub>.
3. SNR calculation includes distortion and noise components.
4. Sample tested @ +25°C to ensure compliance.
5. Specifications subject to change without notice.
TIMING CHARACTERISTICS\(^1\) \((V_{DD} = +5\, V \pm 5\% , \, V_{REF} = V_{DD}, \, AGND = DGND = 0\, V)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Limit at +25°C (All Versions)</th>
<th>Limit at T(<em>{\text{MIN}}, , T</em>{\text{MAX}}) (All Versions)</th>
<th>Units</th>
<th>Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>t(_1)</td>
<td>50</td>
<td>50</td>
<td>ns min</td>
<td>CONVST Pulse Width</td>
</tr>
<tr>
<td>t(_2)</td>
<td>130</td>
<td>130</td>
<td>ns min</td>
<td>CONVST to BUSY Falling Edge</td>
</tr>
<tr>
<td>t(_3)</td>
<td>0</td>
<td>0</td>
<td>ns min</td>
<td>BUSY to CS Setup Time</td>
</tr>
<tr>
<td>t(_4)</td>
<td>0</td>
<td>0</td>
<td>ns min</td>
<td>CS to RD Setup Time</td>
</tr>
<tr>
<td>t(_5)</td>
<td>0</td>
<td>0</td>
<td>ns min</td>
<td>CS to RD Hold Time</td>
</tr>
<tr>
<td>t(_6)</td>
<td>60</td>
<td>75</td>
<td>ns min</td>
<td>RD Pulse Width</td>
</tr>
<tr>
<td>t(_7)</td>
<td>57</td>
<td>70</td>
<td>ns max</td>
<td>Data Access Time after RD</td>
</tr>
<tr>
<td>t(_8)</td>
<td>5</td>
<td>5</td>
<td>ns min</td>
<td>Bus Relinquish Time after RD</td>
</tr>
</tbody>
</table>

NOTES
\(^1\) Timing specifications in bold print are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with \(t_{r} = t_{f} = 5\, \text{ns}\) (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

\(^2\) t\(_8\) is derived from the measured time taken by the data outputs to change by 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging the 50 pF capacitor. This means that the time, t\(_8\), quoted in the timing characteristics is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

Table I. Truth Table

<table>
<thead>
<tr>
<th>CS</th>
<th>CONVST</th>
<th>RD</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>X</td>
<td>Not Selected</td>
</tr>
<tr>
<td>1</td>
<td>j</td>
<td>1</td>
<td>Start Conversion g</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Enable ADC Data</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Data Bus Three Stated</td>
</tr>
</tbody>
</table>

ABSOLUTE MAXIMUM RATINGS\(^*\)

- \(V_{DD}\) to AGND .......................... -0.3 V to +7 V
- \(V_{DD}\) to DGND .......................... -0.3 V to +7 V
- AGND to DGND .............................. -0.3 V to \(V_{DD}\) + 0.3 V
- \(V_{\text{INA}}, \, V_{\text{INB}}\) to AGND (Figure 5) ... -0.3 V to \(V_{DD}\) + 0.3 V
- \(V_{\text{INA}}\) to AGND (Figure 6) ..... -0.6 V to \(2 \, V_{DD}\) + 0.6 V
- \(V_{\text{INA}}\) to AGND (Figure 7) ..... \(-V_{DD}\) - 0.3 V to \(V_{DD}\) + 0.3 V
- \(V_{\text{REF}}\) to AGND .......................... 0.3 V to \(V_{DD}\)
- Digital Inputs to DGND .......................... -0.3 V to \(V_{DD}\) + 0.3 V
- Digital Outputs to DGND .......................... -0.3 V to \(V_{DD}\) + 0.3 V

Operating Temperature Range
- Industrial (B, C Versions) .......................... -40°C to +85°C
- Storage Temperature Range .................. -65°C to +150°C
- Lead Temperature (Soldering, 10 secs) .......... +300°C
- Power Dissipation (Any Package) to +75°C .......................... 450 mW
- Derates above +75°C by .......................... 10 mW/°C

\(^*\) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD 7880 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.
AD7880

ORDERING GUIDE

<table>
<thead>
<tr>
<th>Model</th>
<th>Temperature Range</th>
<th>Full-Scale Error (LSBs)</th>
<th>Bipolar Zero Error (LSBs)</th>
<th>Package Option*</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD7880BN</td>
<td>-40°C to +85°C</td>
<td>±15</td>
<td>±10</td>
<td>N-24</td>
</tr>
<tr>
<td>AD7880BQ</td>
<td>-40°C to +85°C</td>
<td>±15</td>
<td>±10</td>
<td>Q-24</td>
</tr>
<tr>
<td>AD7880CN</td>
<td>-40°C to +85°C</td>
<td>±5</td>
<td>±5</td>
<td>N-24</td>
</tr>
<tr>
<td>AD7880CQ</td>
<td>-40°C to +85°C</td>
<td>±5</td>
<td>±5</td>
<td>Q-24</td>
</tr>
<tr>
<td>AD7880BR</td>
<td>-40°C to +85°C</td>
<td>±15</td>
<td>±10</td>
<td>R-24</td>
</tr>
<tr>
<td>AD7880CR</td>
<td>-40°C to +85°C</td>
<td>±5</td>
<td>±5</td>
<td>R-24</td>
</tr>
</tbody>
</table>

* N = Plastic DIP; Q = Cerdip; R = SOIC (Small Outline Integrated Circuit).

PIN CONFIGURATION

AD7880

NOTE VIEW (Not to Scale)

VDD 24
VDD 23
MODE 22
DB11 21
DB10 20
DB9 19
DB8 18
DB7 17
DB6 16
DB5 15
DB4 14
DB3 13
DB2 12
DB1 11
DB0 10
DGND 9
CLKIN 8
BUSY 7
RD 6
CONVST 5
CS 4
VREF 3
AGND 2
VINA 1

PIN FUNCTION DESCRIPTION

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Pin Mnemonic</th>
<th>Function</th>
</tr>
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<tbody>
<tr>
<td>1</td>
<td>VINA</td>
<td>Analog Input.</td>
</tr>
<tr>
<td>2</td>
<td>VINB</td>
<td>Analog Input.</td>
</tr>
<tr>
<td>3</td>
<td>AGND</td>
<td>Analog Ground.</td>
</tr>
<tr>
<td>4</td>
<td>VREF</td>
<td>Voltage Reference Input. This is normally tied to VDD.</td>
</tr>
<tr>
<td>5</td>
<td>CS</td>
<td>Chip Select. Active Low Logic input. The device is selected when this input is active.</td>
</tr>
<tr>
<td>6</td>
<td>CONVST</td>
<td>Convert Start. A low to high transition on this input puts the track/hold into hold mode and starts conversion. This input is asynchronous to the CLKIN and is independent of CS and RD.</td>
</tr>
<tr>
<td>7</td>
<td>RD</td>
<td>Read. Active Low Logic Input. This input is used in conjunction with CS low to enable data outputs.</td>
</tr>
<tr>
<td>8</td>
<td>BUSY</td>
<td>Active Low Logic Output. This status line indicates converter status. BUSY is low during conversion.</td>
</tr>
<tr>
<td>9</td>
<td>CLKIN</td>
<td>Clock Input. TTL-compatible logic input. Used as the clock source for the A/D converter. The mark/space ratio of the clock can vary from 40/60 to 60/40.</td>
</tr>
<tr>
<td>10</td>
<td>DGND</td>
<td>Digital Ground.</td>
</tr>
<tr>
<td>11...22</td>
<td>DB0-DB11</td>
<td>Three-State Data Outputs. These become active when CS and RD are brought low.</td>
</tr>
<tr>
<td>23</td>
<td>MODE</td>
<td>MODE Input. This input is used to put the device into the power save mode (MODE = 0 V). During normal operation, the MODE input will be a logic high (MODE = VDD).</td>
</tr>
<tr>
<td>24</td>
<td>VDD</td>
<td>Power Supply. This is nominally +5 V.</td>
</tr>
</tbody>
</table>
CIRCUIT INFORMATION
The AD7880 is a +5 V single supply 12-bit A/D converter. The part requires no external components apart from a 2.5 MHz external clock and power supply decoupling capacitors. It contains a 12-bit successive approximation ADC based on a fast-settling voltage-output DAC, a high speed comparator and SAR, as well as the necessary control logic. The charge balancing comparator used in the AD7880 provides the user with an inherent track-and-hold function. The ADC is specified to work with sampling rates up to 66 kHz.

CONVERTER DETAILS
The AD7880 conversion cycle is initiated on the rising edge of the CONVST pulse, as shown in the timing diagram of Figure 1. The rising edge of the CONVST pulse places the track/hold amplifier into "HOLD" mode. The conversion cycle then takes between 26 and 28 clock periods. The maximum specified conversion time is 12 µs. This corresponds to a conversion cycle time of 28 clock periods with a CLKIN frequency of 2.5 MHz and also includes internal propagation delays. During conversion the BUSY output will remain low, and the output databus drivers will be three-stated. When a conversion is completed, the BUSY output will go to a high level, and the result of the conversion can be read by bringing CS and RD low.

The track/hold amplifier acquires a 12-bit input signal in 3 µs. The overall throughput time for the AD7880 is equal to the conversion time plus the track/hold acquisition time. For a 2.5 MHz input clock the throughput time is 15 µs.

REFERENCE INPUT
For specified performance, it is recommended that the reference input be tied to VDD. The part, however, will operate with a reference down to 2.5 V though with reduced performance specifications. Figure 3 shows a graph of signal-to-noise ratio (SNR) versus VREF.

VREF must not be allowed to go above VDD by more than 100 mV.

ANALOG INPUT
The AD7880 has two analog input pins, VINA and VINB. Figure 4 shows the input circuitry to the ADC sampling comparator. The on-board attenuator network, made up of equal resistors, allows for various input ranges.

Table II. Analog Input Ranges

<table>
<thead>
<tr>
<th>Analog Input Range</th>
<th>VREF</th>
<th>Input Connections</th>
<th>Connection Diagram</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 V to +5 V</td>
<td>VDD</td>
<td>VINA</td>
<td>Figure 5</td>
</tr>
<tr>
<td>0 V to +10 V</td>
<td>VDD</td>
<td>VINA, AGND</td>
<td>Figure 6</td>
</tr>
<tr>
<td>±5 V</td>
<td>VDD</td>
<td>VINA, VREF</td>
<td>Figure 7</td>
</tr>
</tbody>
</table>

Figure 4. AD7880 Input Circuit
The AD7880 accommodates three separate input ranges, 0 to VREF, 0 to 2 VREF and ±VREF. The input configurations corresponding to these ranges are shown in Figures 5, 6 and 7.

With VREF = VDD and using a nominal VDD of +5 V, the input ranges are 0 V to 5 V, 0 V to 10 V and +5 V, as shown in Table II.

Figure 5. 0 to VREF Unipolar Input Configuration
Figure 6. 0 to 2 VREF Unipolar Input Configuration
Figure 7. ±VREF Bipolar Input Configuration
The AD7880 has two unipolar input ranges, 0 V to 5 V and 0 V to 10 V. Figure 5 shows the analog input for the 0 V to 5 V range. The designed code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs, ..., FS – 3/2 LSBs). The output code is straight binary with 1 LSB = FS/4096 = 5 V/4096 = 1.22 mV. The same applies for the 0 V to 10 V range, as shown in Figure 6, except that the LSB size is bigger. In this case 1 LSB = FS/4096 = 10 V/4096 = 2.44 mV. The ideal input/output transfer characteristic for both these unipolar ranges is shown in Figure 8.

The AD7880 is specified to operate with a 2.5 MHz clock connected to the CLKIN input pin. This pin may be driven directly by CMOS or TTL buffers. The mark/space ratio on the clock can vary from 40/60 to 60/40. As the clock frequency is slowed down, it can result in slightly degraded accuracy performance. This is due to leakage effects on the hold capacitor in the internal track-and-hold amplifier. Figure 10 is a typical plot of accuracy versus clock frequency for the ADC.

The charge balanced comparator used in the AD7880 for the A/D conversion provides the user with an inherent track/hold function. The track/hold amplifier acquires an input signal to 12-bit accuracy in less than 3 µs. The overall throughput time is equal to the conversion time plus the track/hold amplifier acquisition time. For a 2.5 MHz input clock, the throughput time is 15 µs.

The operation of the track/hold amplifier is essentially transparent to the user. The track/hold amplifier goes from its tracking mode to its hold mode at the start of conversion, i.e., on the rising edge of CONVST as shown in Figure 1.

In most Digital Signal Processing (DSP) applications, offset and full-scale errors have little or no effect on system performance. Offset error can always be eliminated in the analog domain by ac coupling. Full-scale error effect is linear and does not cause problems as long as the input signal is within the full dynamic range of the ADC. Some applications will require that the input signal range match the maximum possible dynamic range of the ADC. In such applications, offset and full-scale error will have to be adjusted to zero.

The following sections describe suggested offset and full-scale adjustment techniques which rely on adjusting the inherent offset of the op amp driving the input to the ADC as well as tweaking an additional external potentiometer as shown in Figure 11.
Unipolar Adjustments
In the case of the 0 V to 5 V unipolar input configuration, unipolar offset error must be adjusted before full-scale error. Adjustment is achieved by trimming the offset of the op amp driving the analog input of the AD7880. This is done by applying an input voltage of 0.61 mV (1/2 LSB) to V1 in Figure 11 and adjusting the op amp offset voltage until the ADC output code flickers between 0000 0000 0000 and 0000 0000 0001. For full-scale adjustment, an input voltage of 4.9982 V (FS–3/2 LSBs) is applied to V1 and R2 is adjusted until the output code flickers between 1111 1111 1110 and 1111 1111 1111.

The same procedure is required for the 0 V to 10 V input configuration of Figure 6. An input voltage of 1.22 mV (1/2 LSB) is applied to V1 in Figure 11 and the op amp’s offset voltage is adjusted until the ADC output code flickers between 0000 0000 0000 and 0000 0000 0001. For full-scale adjustment, an input voltage of 9.9963 V (FS–3/2 LSBs) is applied to V1 and R2 is adjusted until the output code flickers between 1111 1111 1110 and 1111 1111 1111.

Bipolar Adjustments
Bipolar zero and full-scale errors for the bipolar input configuration of Figure 7 are adjusted in a similar fashion to the unipolar case. Again, bipolar zero error must be adjusted before full-scale error. Bipolar zero error adjustment is achieved by trimming the offset of the op amp driving the analog input of the AD7880 while the input voltage is 1/2 LSB below ground. This is done by applying an input voltage of –1.22 mV (1/2 LSB) to V1 in Figure 11 and adjusting the op amp offset voltage until the ADC output code flickers between 0111 1111 1111 and 1000 0000 0000. For full-scale adjustment, an input voltage of 4.9982 V (FS/2–3/2 LSBs) is applied to V1 and R2 is adjusted until the output code flickers between 1111 1111 1110 and 1111 1111 1111.

DYNAMIC SPECIFICATIONS
The AD7880 is specified and tested for dynamic performance specifications as well as traditional dc specifications such as integral and differential nonlinearity. The ac specifications are required for signal processing applications such as speech recognition, spectrum analysis and high speed modems. These applications require information on the ADC’s effect on the spectral content of the input signal. Hence, the parameters for which the AD7880 is specified include SNR, harmonic distortion, intermodulation distortion and peak harmonics. These terms are discussed in more detail in the following sections.

Signal-to-Noise Ratio (SNR)
SNR is the measured signal-to-noise ratio at the output of the ADC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency (FS/2) excluding dc. SNR is dependent upon the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to noise ratio for a sine wave input is given by:

\[
SNR = (6.02N + 1.76) \text{ dB}
\]

where N is the number of bits.

Thus for an ideal 12-bit converter, SNR = 74 dB.

The output spectrum from the ADC is evaluated by applying a sine wave signal of very low distortion to the VIN input which is sampled at a 66 kHz sampling rate. A Fast Fourier Transform (FFT) plot is generated from which the SNR data can be obtained. Figure 12 shows a typical 2048 point FFT plot of the AD7880 with an input signal of 2.5 kHz and a sampling frequency of 61 kHz. The SNR obtained from this graph is 73 dB. It should be noted that the harmonics are taken into account when calculating the SNR.

Effective Number of Bits
The formula given in Equation 1 relates the SNR to the number of bits. Rewriting the formula, as in Equation 2, it is possible to get a measure of performance expressed in effective number of bits (N).

\[
N = \frac{SNR - 1.76}{6.02}
\]

The effective number of bits for a device can be calculated directly from its measured SNR.

Figure 13 shows a plot of effective number of bits versus input frequency for an AD7880 with a sampling frequency of 61 kHz. The effective number of bits typically remains better than 11.5 for frequencies up to 12 kHz.
Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of harmonics to the rms value of the fundamental. For the AD7880, THD is defined as:

$$\text{THD} = 20\log_10 \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where $V_1$ is the rms amplitude of the fundamental and $V_2$, $V_3$, $V_4$, $V_5$ and $V_6$ are the rms amplitudes of the second through the sixth harmonic. The THD is also derived from the FFT plot of the ADC output spectrum.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, $f_a$ and $f_b$, any active device with nonlinearities will create distortion products at sum and difference frequencies of $m f_a \pm n f_b$ where $m$, $n = 0$, 1, 2, 3, etc. Intermodulation terms are those for which neither $m$ nor $n$ are equal to zero. For example, the second order terms include $(f_a + f_b)$ and $(f_a - f_b)$, while the third order terms include $(2f_a + f_b)$, $(2f_a - f_b)$, $(f_a + 2f_b)$ and $(f_a - 2f_b)$.

Using the CCIF standard where two input frequencies near the top end of the input bandwidth are used, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves, while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs. In this case, the input consists of two, equal amplitude, low distortion, sine waves. Figure 14 shows a typical IMD plot for the AD7880.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to FS/2 and excluding dc) to the rms value of the fundamental. Normally, the value of this specification will be determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor the peak will be a noise peak.
MICROPROCESSOR INTERFACING

The AD 7880 high speed bus timing allows direct interfacing to real-time digital signal processors, DSPs, as well as modern high-speed, 16-bit microprocessors. Suitable microprocessor interfaces are shown in Figures 15 through 20.

AD7880-ADSP-2100 Interface

Figure 15 shows an interface between the AD 7880 and the ADSP-2100. Conversion is initiated using a timer to drive the CONVST input asynchronously to the microprocessor. This allows very accurate control of the sampling instant. When conversion is complete, the AD 7880 BUSY line goes high. An inverter on this BUSY output drives the IRQ line low thus providing an interrupt to the AD SP-2100 when conversion is completed. The conversion result is then read from the AD 7880 into the ADSP-2100 with the following instruction:

\[ MR0 = DM(ADC) \]

where MR0 is the ADSP-2100 M R0 Register and ADC is the AD 7880 address.

AD7880-ADSP-2101/ADSP-2102 Interface

The interface outlined in Figure 15 also forms the basis for an interface between the AD 7880 and the ADSP-2101/ADSP-2102. The READ line of the AD SP-2101/ADSP-2102 is labeled RD. In this interface, the RD pulse width of the processor can be programmed using the Data Memory Wait State Control Register. The instruction used to read a conversion result is as outlined for the AD SP-2100.

AD7880-TMS32010 Interface

An interface between the AD 7880 and the TMS32010 is shown in Figure 16. Once again the conversion is initiated using an external timer and the TMS32010 is interrupted when conversion is completed. The following instruction is used to read the conversion result from the AD 7880:

\[ IN D,ADC \]

where D is Data Memory Address and ADC is the AD 7880 address.

AD7880-TMS320C25 Interface

Some applications may require that the conversion be initiated by the microprocessor rather than an external timer. One option is to decode the AD 7880 CONVST from the address bus so that...
a write operation starts a conversion. Data is read at the end of the conversion sequence as before. Figure 19 shows an example of initiating conversion using this method. A similar implementation can be used for DSPs. Note that for all interfaces, a read operation should not be attempted during conversion.

**AD7880-MC 68000 Interface**

An interface between the AD7880 and the MC68000 is shown in Figure 18. As before, conversion is initiated using an external timer. The AD7880 BUSY line can be used to interrupt the processor or, alternatively, software delays can ensure that conversion has been completed before a read to the AD7880 is attempted. Because of the nature of its interrupts, the 68000 requires additional logic (not shown in Figure 18) to allow it to be interrupted correctly. For further information on 68000 interrupts, consult the 68000 user’s manual.

The MC68000 AS and R/W outputs are used to generate a separate RD input signal for the AD7880. CS is used to drive the 68000 DTACK input to allow the processor to execute a normal read operation to the AD7880. The conversion results are read using the following 68000 instruction:

```
MOVE.W ADC, D0
```

where D0 is the 68000 D0 register

ADC is the AD7880 address

**AD7880–8086 Interface**

Figure 19 shows an interface between the AD7880 and the 8086 microprocessor. Unlike the previous interface examples, the microprocessor initiates conversion. This is achieved by gating the 8086 WR signal with a decoded address output (different to the AD7880 CS address). Conversion is initiated and the result is read from the AD7880 using the following instruction:

```
MOV AX, ADC
```

where AX is the 8086 accumulator and

ADC is the AD7880 address

**AD7880–6809 Interface**

The AD7880 can also interface quite easily with 8-bit microprocessors. The 12-bit parallel data output from the AD7880 can be read into the microprocessor as an 8+4 byte structure. Figure 20 shows an interface to the MC6809 8-bit microprocessor. As in previous cases, conversion is initiated using an external timer. At the end of conversion, BUSY triggers a one-shot which drives the IRQ interrupt input of the microprocessor. A double read is then performed to two unique addresses. The first read fetches the lower 8 bits (DB0–DB7) and loads the 74HC374 latch with the upper 4 bits (DB8–DB11). The second read fetches these upper 4 bits.

---

**Figure 18. AD7880–MC68000 Interface**

**Figure 19. AD7880–8086 Interface**

**Figure 20. AD7880–6809 Interface**
APPLICATION HINTS
Good printed circuit board (PCB) layout is as important as the circuit design itself in achieving high speed A/D performance. The AD7880’s comparator is required to make bit decisions on an LSB size of 1.22 mV. To achieve this, the designer must be conscious of noise both in the ADC itself and in the preceding analog circuitry. Switching mode power supplies are not recommended, as the switching spikes will feed through to the comparator causing noisy code transitions. Other causes of concern are ground loops and digital feedthrough from microprocessors. These are factors which influence any ADC, and a proper PCB layout which minimizes these effects is essential for best performance.

LAYOUT HINTS
Ensure that the layout for the printed circuit board has the digital and analog signal lines separated as much as possible. Take care not to run digital tracks alongside analog signal tracks. Guard (screen) the analog input with AGND.

Establish a single point analog ground (star ground) separate from the logic system ground at the AD7880 AGND pin or as close as possible to the AD7880. Connect all other grounds and the AD7880 GND to this single analog ground point. Do not connect any other digital grounds to this analog ground point.

Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC, so make the foil width for these tracks as wide as possible. The use of ground planes minimizes impedance paths and also guards the analog circuitry from digital noise. The circuit layout of Figures 26 and 27 have both analog and digital ground planes which are kept separated and only joined together at the AD7880 AGND pin.

NOISE
Keep the input signal leads to V_IN and signal return leads from AGND as short as possible to minimize input noise coupling. In applications where this is not possible, use a shielded cable between the source and the ADC. Reduce the ground circuit impedance as much as possible since any potential difference in grounds between the signal source and the ADC appears as an error voltage in series with the input signal.

ANALOG INPUT BUFFERING
To achieve specified performance, it is recommended that the analog input (V_INA, V_INB) be driven from a low impedance source. This necessitates the use of an input buffer amplifier. The choice of op amp will be a function of the particular application and the desired analog input range. The data acquisition circuit, described in this data sheet allows for various op amp configurations. Figure 21 shows the analog input buffer circuit.

The options available to drive the supply of the op amp are:

- Single +5 V (derived from PCB 5 V supply)
- Dual Supply (externally supplied to V+ and V-)

The simplest configuration is the 0 V to 5 V range of Figure 5. A single supply 5 V op amp is recommended for such an implementation. This will allow for operation of the AD7880 in the 0 V to 5 V unipolar range without supplying an external supply to V+ and V-. The 5 V supply is derived from the systems +5 V V_DD supply.

When it is required to drive the AD7880 with the 0 V to 10 V input range, an external supply must be connected to V+ (see Figure 21).

In bipolar operation, positive and negative supplies must be connected to V+ and V-.

The AD711 is a general purpose op amp which could be used to drive the analog input of the AD7880.

POWER-DOWN CONTROL (MODE INPUT)
The AD7880 is designed for systems which need to have minimum power consumption. This includes such applications as hand held, portable battery powered systems and remote monitoring systems. As well as consuming minimum power under normal operating conditions, typically 20 mW, the AD7880 can be put into a power-down or sleep mode when not required to convert signals. When in this power-down mode, the AD7880 consumes approximately 2 mW of power.

The AD7880 is powered down by bringing the MODE input pin to a Logic Low in conjunction with keeping the RD input control High. The AD7880 will remain in the power-down mode until MODE is brought to a Logic High again. The MODE input should be driven with CD4000 or HCMOS logic levels.

It is recommended that one “dummy” conversion be implemented before reading conversion data from the AD7880 after it has been in the power-down mode. This is required to reset all internal logic and control circuitry. In a remote monitoring system where, say, 10 conversions are required to be taken with a sampling interval of 1 second, an additional 11th conversion must be carried out. Figure 22 gives a plot of power consumption.
AD7880

as a function of time for such operation. The total conversion time for each cycle is \(11 \times 15 \mu s\) (where \(15 \mu s\) is the time taken for a single conversion) corresponding to \(1.65 \times 10^{-6}\) secs. Hence:

\[
\text{Average Power} = \text{Power}_{\text{CONVERTING}} + \text{Power}_{\text{POWER-DOWN}} = (20 \text{ mW} \times (1.65 \times 10^{-4})/(10)) + (2 \text{ mW} \times (9.9998)/(10)) = 2.029 \text{ mW}
\]

AD7880 DATA ACQUISITION LAYOUT

Figure 24 shows the AD7880 in a data acquisition circuit. The corresponding printed circuit board (PCB) layout and silkscreen are shown in Figures 25 to 27.

The only additional component required for a full data acquisition system is an antialiasing filter. There is a component grid provided near the analog input on the PCB which may be used for such a filter or any other input conditioning circuitry. To facilitate this option there is a shorting link (labeled LK1 on the PCB) on the analog input track. With LK1 in place, the analog input connects to the buffer amplifier driving the AD7880. With LK1 removed, a wire link is needed to connect the analog input to the PCB component grid.

INTERFACE CONNECTIONS

The data acquisition board contains a parallel connection port labeled SKT4. This is a 26-contact IDC Connector and provides for direct microprocessor connection to the board. This connector, the pinout of which is shown in Figure 23, contains all data, control and status signals of the AD7880 (with the exception of the CONVST and the CLKIN inputs both of which are provided via SKT2 and SKT3 respectively). It also contains decoded R/W and STRB inputs which are necessary for interfacing to many microprocessors including the TMS320C25 and the Motorola 68000 series. Link LK7 selects RD directly or alternatively, the decoded version. Note that the AD7880 CS input must be decoded prior to the AD7880 evaluation board.

SKT1, SKT2 and SKT3 are three sub-miniature connectors (SMC) which provide input connections for the analog input, the CONVST input and the CLKIN input. Three different input ranges can be accepted by the AD7880 each of which is configured by selecting shorting plug options A, B or C of LK4. Position A corresponds to the 0 V to 5 V unipolar configuration of Figure 5, position B corresponds to the bipolar ±5 V configuration of Figure 7 and position C allows for a 0 V to +10 V unipolar range as shown in Figure 6.

POWER SUPPLY CONNECTIONS

The PCB requires a single +5 V power supply (labeled VDD). Good decoupling allows this supply to drive the AD7880 VDD which also drives the VREF input as well as the op amp power supply. In circumstances where bipolar ±5 V or a unipolar 0 V to 10 V input ranges are required, provision has been allowed for the connection of separate op amp power supplies (+15 V, ±12 V, ±5 V, etc.) to V+ and V−. LK2 and LK3 shorting links allow for the selection of user defined op amp power supplies or the on-board single +5 V supply.

LINK OPTIONS

There are seven link options which must be set before using the board. These are outlined below:

- **LK1**: Connects the analog input to a buffer amplifier. The analog input may also be connected to a component grid for signal conditioning.
- **LK2, LK3**: Allows for various op amp power supplies to be used to drive the input buffer of the AD7880. External supplies may be connected to V+ and V−. Alternatively, the AD7880’s +5 V system supply and AGND can be selected to drive a single supply op amp.
- **LK4**: Configures the various analog input ranges, 0 V to 5 V, 0 V to 10 V or ±5 V.
- **LK5**: Selects reference input to VREF of AD7880. Normally connected to VDD. An external reference could also be wired in.
- **LK6**: Selects power-down or sleep mode. The shorting plug is connected to VDD for normal operation.
- **LK7**: Connects the AD7880 RD input directly to the RD input of SKT4 or to a decoded STRB and R/W input. This shorting plug setting depends on the microprocessor, e.g., the TMS5320C25 requires a decoded RD signal.

![Figure 23. SKT4, IDC Connector Pinout](image)

**COMPONENT LIST**

- **IC1**: Op Amp*
- **IC2**: AD7880 Analog-to-Digital Converter
- **IC3**: 74HC00 Quad NAND Gate
- **C1, C3, C5**: 10 µF Capacitors
- **C2, C4, C6, C7**: 0.1 µF Capacitors
- **R1, R2**: 10 kΩ Pull-up Resistors
- **LK1, LK2, LK3**: Shorting Links
- **LK4, LK5, LK6, LK7**:
- **SKT1, SKT2, SKT3**: Sub-Miniature Connectors
  - Vendor No: Seallectro 50-051-0000 (Socket)
  - Seallectro 50-007-0000 (Plug)
- **SKT4**: 26-Contact (2 Row) IDC Connector

**NOTE**

*See ANALOG INPUT BUFFERING section.
Figure 24. Data Acquisition Circuit Using the AD7880

Figure 25. PCB Silkscreen for Figure 24
Figure 26. PCB Component Side Layout for Figure 24

Figure 27. PCB Solder Side Layout for Figure 24
OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).

24-Lead Plastic DIP (N-24)

NOTES:
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. PLASTIC LEADS WILL BE EITHER SOLDER DIPPED OR TIN LEAD PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

24-Lead Cerdip (Q-24)

NOTES:
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERDIP LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

24-Lead SOIC (R-24)

NOTES:
- LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.