AD7821

FEATURES
Fast Conversion Time: 660 ns Max
100 kHz Track-and-Hold Function
1 MHz Sample Rate
Unipolar and Bipolar Input Ranges
Ratiometric Reference Inputs
No External Clock
Extended Temperature Range Operation
Skinny 20-Lead DIPs, SOIC, and 20-Terminal
Surface-Mount Packages

GENERAL DESCRIPTION
The AD7821 is a high speed, 8-bit, sampling, analog-to-digital converter that offers improved performance over the popular AD7820. It offers a conversion time of 660 ns (versus 1.36 µs for the AD7820) and 100 kHz signal bandwidth (versus 6.4 kHz). The sampling instant is better defined and occurs on the falling edge of WR or RD. The provision of a VSS pin (Pin 19) allows the part to operate from ±5 V supplies and to digitize bipolar input signals. Alternatively, for unipolar inputs, the VSS pin can be grounded and the AD7821 will operate from a single +5 V supply, like the AD7820.

The AD7821 has a built-in track-and-hold function capable of digitizing full-scale signals up to 100 kHz max. It also uses a half-flash conversion technique that eliminates the need to generate a CLK signal for the ADC.

The AD7821 is designed with standard microprocessor control signals (CS, RD, WR, RDY, INT) and latched, three-state data outputs capable of interfacing to high speed data buses. An overflow output (OFL) is also provided for cascading devices to achieve higher resolution.

The AD7821 is fabricated in Linear Compatible CMOS (LC2MOS), an advanced, mixed technology process combining precision bipolar circuits with low power CMOS logic. The part features a low power dissipation of 50 mW.

PRODUCT HIGHLIGHTS
1. Fast Conversion Time
   The half-flash conversion technique, coupled with fabrication on Analog Devices' LC2MOS process, enables a very fast conversion time. The conversion time for the WR-RD mode is 660 ns, with 700 ns for the RD mode.

2. Built-In Track-and-Hold
   This allows input signals with slew rates up to 1.6 V/µs to be converted to 8 bits without an external track-and-hold. This corresponds to a 5 V peak-to-peak, 100 kHz sine wave signal.

3. Total Unadjusted Error
   The AD7821 features an excellent total unadjusted error figure of less than ±1 LSB over the full operating temperature range.

4. Unipolar/Bipolar Input Ranges
   The AD7821 is specified for single-supply (+5 V) operation with a unipolar full-scale range of 0 to +5 V, and for dual-supply (±5 V) operation with a bipolar input range of ±2.5 V. Typical performance characteristics are given for other input ranges.

5. Dynamic Specifications for DSP Users
   In addition to the traditional ADC specifications, the AD7821 is specified for ac parameters, including signal-to-noise ratio, distortion, and slew rate.
COMPARABLE PARTS
View a parametric search of comparable parts.

DOCUMENTATION
Application Notes
- AN-299: Simple Circuit Provides Ratiometric Reference Levels for AD782X Family of Half-Flash ADCs

Data Sheet
- AD7821: High Speed, μP-Compatible, CMOS, 8-Bit Sampling ADC Data Sheet
- AD7821: Military Data Sheet

REFERENCE MATERIALS
Technical Articles
- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES
- AD7821 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS
View all AD7821 EngineerZone Discussions.

SAMPLE AND BUY
Visit the product page to see pricing options.

TECHNICAL SUPPORT
Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK
Submit feedback for this data sheet.
**AD7821—SPECIFICATIONS**  
\[ V_{DD} = +5 \text{ V} \pm 5\% , \text{ GND} = 0 \text{ V} . \text{ Unipolar Input Range: } V_{SS} = \text{ GND}, V_{REF(+)} = 5 \text{ V} ,\]  
\[ V_{REF(-)} = \text{ GND} . \text{ Bipolar Input Range: } V_{SS} = -5 \text{ V} \pm 5\% , V_{REF(+)} = 2.5 \text{ V} , V_{REF(-)} = -2.5 \text{ V} . \text{ These test conditions apply unless otherwise stated. All specifications } T_{\text{MIN}} \text{ to } T_{\text{MAX}} \text{ unless otherwise noted. Specifications apply for RD Mode (Pin 7 = } 0 \text{ V).} \]

### Parameter | K Version | B, T Versions | Unit | Comments
--- | --- | --- | --- | ---
**UNIPOLAR INPUT RANGE**
Resolution | 8 | 8 | Bits |  
Total Unadjusted Error | \( \pm 1 \) | \( \pm 1 \) | LSB max |  
Minimum Resolution for which No Missing Codes are Guaranteed | 8 | 8 | Bits |  
**BIPOLAR INPUT RANGE**
Resolution | 8 | 8 | Bits |  
Zero Code Error | \( \pm 1 \) | \( \pm 1 \) | LSB max |  
Full Scale Error | \( \pm 1 \) | \( \pm 1 \) | LSB max |  
Signal-to-Noise Ratio (SNR) | 45 | 45 | dB min | \[ V_{DD} = 99.85 \text{ kHz Full-Scale Sine Wave with } f_{\text{SAMPLING}} = 500 \text{ kHz} \]
Zero Code Error | \( \pm 1 \) | \( \pm 1 \) | LSB max |  
Full Scale Error | \( \pm 1 \) | \( \pm 1 \) | LSB max |  
Signal-to-Noise Ratio (SNR) | 45 | 45 | dB min | \[ V_{DD} = 99.85 \text{ kHz Full-Scale Sine Wave with } f_{\text{SAMPLING}} = 500 \text{ kHz} \]
Total Harmonic Distortion (THD) | \(-50 \) | \(-50 \) | dB max | \[ V_{DD} = 99.85 \text{ kHz Full-Scale Sine Wave with } f_{\text{SAMPLING}} = 500 \text{ kHz} \]
Peak Harmonic or Spurious Noise | \(-50 \) | \(-50 \) | dB max | \[ f_a (84.72 \text{ kHz}) \text{ and } f_b (94.97 \text{ kHz}) \text{ Full-Scale Sine Waves with } f_{\text{SAMPLING}} = 500 \text{ kHz} \]
Intermodulation Distortion (IMD) | \(-50 \) | \(-50 \) | dB max | Second Order Terms | Third Order Terms |  
Slew Rate, Tracking | 1.6 | 1.6 | V/\( \mu \)s |  
**REFERENCE INPUT**
Input Resistance | 1.0/4.0 | 1.0/4.0 | kΩ min/kΩ max |  
Input Voltage Range | \[ V_{REF(+)} / V_{DD} \] | \[ V_{REF(-)} / V_{DD} \] | V min/V max |  
Input Voltage Range | \[ V_{REF(+)} / V_{REF(+)} \] | \[ V_{REF(-)} / V_{REF(+)} \] | V min/V max |  
**ANALOG INPUT**
Input Voltage Range | \( \pm 3 \) | \( \pm 3 \) | μA max | \(-5 \text{ V} \leq V_{DD} \leq +5 \text{ V} \) |  
Input Capacitance | 55 | 55 | pF typ |  
**LOGIC INPUTS**
\( CS, WR, RD \)
\[ V_{\text{IH}} \] | 2.4 | 2.4 | V min |  
\[ V_{\text{IL}} \] | 0.8 | 0.8 | V max |  
\[ I_{\text{IH}} (CS, RD) \] | 1 | 1 | μA max |  
\[ I_{\text{IH}} (WR) \] | 3 | 3 | μA max |  
\[ I_{\text{IL}} \] | \(-1 \) | \(-1 \) | μA max |  
Input Capacitance | 8 | 8 | pF max | Typically 5 pF |  
\( \text{MODE} \)
\[ V_{\text{IH}} \] | 3.5 | 3.5 | V min |  
\[ V_{\text{IL}} \] | 1.5 | 1.5 | V max |  
\[ I_{\text{IH}} \] | 200 | 200 | μA max | 50 μA typ |  
\[ I_{\text{IL}} \] | \(-1 \) | \(-1 \) | μA max |  
Input Capacitance | 8 | 8 | pF max | Typically 5 pF |  
**LOGIC OUTPUTS**
\( DB_0–DB_7, O\_FL, INT \)
\[ V_{\text{OH}} \] | 4.0 | 4.0 | V min | \[ I_{\text{SOURCE}} = 360 \mu A \] |  
\[ V_{\text{OL}} \] | 0.4 | 0.4 | V max | \[ I_{\text{SINK}} = 1.6 \mu A \] | Floating State Leakage |  
\[ I_{\text{OUT}} (DB_0–DB_7) \] | \( \pm 3 \) | \( \pm 3 \) | μA max |  
Output Capacitance\(^4\) (DB_0–DB_7) | 8 | 8 | pF max | Typically 5 pF |  
\[ V_{\text{OL}} \] | 0.4 | 0.4 | V max | \[ I_{\text{SINK}} = 2.6 \mu A \] | Floating State Leakage |  
\[ I_{\text{OUT}} \] | \( \pm 3 \) | \( \pm 3 \) | μA max |  
Output Capacitance\(^4\) | 8 | 8 | pF max | Typically 5 pF |  
**POWER SUPPLY**
\[ I_{\text{DD}} \] | 20 | 20 | mA max | \[ CS = RD = 0 \text{ V} \] |  
\[ I_{\text{SS}} \] | 100 | 100 | μA max | \[ CS = RD = 0 \text{ V} \] |  
Power Dissipation | 50 | 50 | mW typ |  
Power Supply Sensitivity | \( \pm 1/4 \) | \( \pm 1/4 \) | LSB max | \[ V_{\text{DD}} = 4.75 \text{ V to } 5.25 \text{ V}, (V_{\text{REF(+)}}, 4.75 \text{ V max for Unipolar Mode}) \]

**NOTES**
\( ^1 \)Temperature Ranges are as follows: K Version = \(-40°C \leq C \leq +85°C\); B Version = \(-40°C \leq C \leq +85°C\); T Version = \(-55°C \leq C \leq +125°C\).  
\( ^2 \)LSB = 19.53 mV for both the unipolar (0 V to +5 V) and bipolar (–2.5 V to +2.5 V) input ranges.  
\( ^3 \)See Terminology.  
\( ^4 \)Sample tested at \(+25°C\) to ensure compliance.  
\( ^5 \)See Typical Performance Characteristics.  
Specifications subject to change without notice.
TIMING CHARACTERISTICS

(VDD = +5 V ± 5%, VSS = 0 V or –5 V ± 5%; Unipolar or Bipolar Input Range)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Limit at +25°C (All Versions)</th>
<th>Limit at TMIN, TMAX (K, B Versions)</th>
<th>Limit at TMIN, TMAX (T Version)</th>
<th>Unit</th>
<th>Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>tCSS</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ns</td>
<td>CS to RD/WR Setup Time</td>
</tr>
<tr>
<td>tCSH</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ns</td>
<td>CS to RD/WR Hold Time</td>
</tr>
<tr>
<td>tRD</td>
<td>70</td>
<td>85</td>
<td>100</td>
<td>ns</td>
<td>CS to RDY Delay. Pull-Up</td>
</tr>
<tr>
<td>tCRD</td>
<td>700</td>
<td>875</td>
<td>975</td>
<td>max</td>
<td>Conversion Time (RD Mode)</td>
</tr>
<tr>
<td>tACCL</td>
<td>160</td>
<td>205</td>
<td>240</td>
<td>ns</td>
<td>Data Access Time (RD Mode)</td>
</tr>
<tr>
<td>tCH</td>
<td>150</td>
<td>185</td>
<td>235</td>
<td>max</td>
<td>CIL = 20 pF</td>
</tr>
<tr>
<td>tIN</td>
<td>500</td>
<td>610</td>
<td>700</td>
<td>min</td>
<td>CIL = 20 pF</td>
</tr>
<tr>
<td>tREAD1</td>
<td>65</td>
<td>75</td>
<td>85</td>
<td>ns</td>
<td>Data Hold Time</td>
</tr>
<tr>
<td>tACCL</td>
<td>65</td>
<td>75</td>
<td>85</td>
<td>ns</td>
<td>Delay Time between Conversions</td>
</tr>
<tr>
<td>tSHF</td>
<td>80</td>
<td>110</td>
<td>130</td>
<td>max</td>
<td>CIL = 20 pF</td>
</tr>
<tr>
<td>tDS</td>
<td>30</td>
<td>35</td>
<td>40</td>
<td>max</td>
<td>CIL = 20 pF</td>
</tr>
</tbody>
</table>

NOTES

1. Sample tested at +25°C to ensure compliance. All input control signals are specified with tRISE = tFALL = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

2. CL = 50 pF.

3. Measured with load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

4. Defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 2.

Specifications subject to change without notice.

Test Circuits

**Figure 1. Load Circuits for Data Access Time Test**

**Figure 2. Load Circuits for Data Hold Time Test**

ORDERING GUIDE

<table>
<thead>
<tr>
<th>Model1</th>
<th>Temperature Range</th>
<th>Total Unadjusted Error (LSB)</th>
<th>Package Option2</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD7821KN</td>
<td>–40°C to +85°C</td>
<td>±1 max</td>
<td>N-20</td>
</tr>
<tr>
<td>AD7821KP</td>
<td>–40°C to +85°C</td>
<td>±1 max</td>
<td>P-20A</td>
</tr>
<tr>
<td>AD7821KR</td>
<td>–40°C to +85°C</td>
<td>±1 max</td>
<td>RW-20</td>
</tr>
<tr>
<td>AD7821BQ</td>
<td>–40°C to +85°C</td>
<td>±1 max</td>
<td>Q-20</td>
</tr>
<tr>
<td>AD7821TQ</td>
<td>–55°C to +125°C</td>
<td>±1 max</td>
<td>Q-20</td>
</tr>
<tr>
<td>AD7821TE</td>
<td>–55°C to +125°C</td>
<td>±1 max</td>
<td>E-20A</td>
</tr>
</tbody>
</table>

NOTES

1. To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact local sales office for military data sheet.

2. E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC.
AD7821

ABSOLUTE MAXIMUM RATINGS*

<table>
<thead>
<tr>
<th>Rating</th>
<th>Min.</th>
<th>Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD to GND</td>
<td>–0.3 V</td>
<td>7 V</td>
</tr>
<tr>
<td>VSS to GND</td>
<td>+0.3 V</td>
<td>7 V</td>
</tr>
<tr>
<td>Digital Input Voltage to GND</td>
<td>–0.3 V</td>
<td>VDD + 0.3 V</td>
</tr>
<tr>
<td>(Pins 6–8, 13)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Digital Output Voltage to GND</td>
<td>–0.3 V</td>
<td>VDD + 0.3 V</td>
</tr>
<tr>
<td>(Pins 2–5, 9, 14–18)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VREF(+) to GND</td>
<td>VSS – 0.3 V</td>
<td>VDD + 0.3 V</td>
</tr>
<tr>
<td>VREF(–) to GND</td>
<td>VSS – 0.3 V</td>
<td>VDD + 0.3 V</td>
</tr>
<tr>
<td>VIN to GND</td>
<td>VSS – 0.3 V</td>
<td>VDD + 0.3 V</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>–40°C to +85°C</td>
<td></td>
</tr>
<tr>
<td>Commercial (K Version)</td>
<td>–40°C to +85°C</td>
<td></td>
</tr>
<tr>
<td>Industrial (B Version)</td>
<td>–40°C to +125°C</td>
<td></td>
</tr>
<tr>
<td>Extended (T Version)</td>
<td>–55°C to +150°C</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>–65°C to +150°C</td>
<td></td>
</tr>
<tr>
<td>Lead Temperature (Soldering, 10 sec)</td>
<td>+300°C</td>
<td></td>
</tr>
<tr>
<td>Power Dissipation (Any Package) to +75°C</td>
<td>450 mW</td>
<td></td>
</tr>
<tr>
<td>Derates above +75°C by</td>
<td>6 mW/°C</td>
<td></td>
</tr>
</tbody>
</table>

*Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7821 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

WARNING!

ESD SENSITIVE DEVICE

CAUTION

ESD SENSITIVE DEVICE

PIN FUNCTION DESCRIPTIONS

<table>
<thead>
<tr>
<th>Pin</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>V IN</td>
<td>Analog Input: Range VREF(–) ≤ VIN ≤ VREF(+)</td>
</tr>
<tr>
<td>2</td>
<td>DB0</td>
<td>Three-State Data Output (LSB)</td>
</tr>
<tr>
<td>3–5</td>
<td>DB1–DB3</td>
<td>Three-State Data Outputs</td>
</tr>
<tr>
<td>6</td>
<td>WR/RDY</td>
<td>WRITE control input/READY status output. See Digital Interface section.</td>
</tr>
<tr>
<td>7</td>
<td>MODE</td>
<td>Mode Selection Input. It determines whether the device operates in the WR-RD or RD mode. This input is internally pulled low through a 50 µA current source. See Digital Interface section.</td>
</tr>
<tr>
<td>8</td>
<td>RD</td>
<td>READ Input. RD must be low to access data from the part. See Digital Interface section.</td>
</tr>
<tr>
<td>9</td>
<td>INT</td>
<td>INTERRUPT Output. INT going low indicates that the conversion is complete. INT returns high on the rising edge of CS or RD. See Digital Interface section.</td>
</tr>
<tr>
<td>10</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>11</td>
<td>VREF(–)</td>
<td>Lower limit of reference span. Range: VSS ≤ VREF(–) ≤ VREF(+)</td>
</tr>
<tr>
<td>12</td>
<td>VREF(+)</td>
<td>Upper limit of reference span. Range: VREF(–) &lt; VREF(+) ≤ VDD</td>
</tr>
<tr>
<td>13</td>
<td>CS</td>
<td>Chip Select Input. The device is selected when this input is low.</td>
</tr>
<tr>
<td>14–16</td>
<td>DB4–DB6</td>
<td>Three-State Data Outputs</td>
</tr>
<tr>
<td>17</td>
<td>DB7</td>
<td>Three-State Data Output (MSB)</td>
</tr>
<tr>
<td>18</td>
<td>OFL</td>
<td>Overflow Output. If the analog input is higher than (VREF(+) – 1/2 LSB), OFL will be low at the end of conversion. It is a non-three-state output which can be used to cascade two or more devices to increase resolution.</td>
</tr>
<tr>
<td>19</td>
<td>VSS</td>
<td>Negative Supply Voltage VSS = 0 V; Unipolar Operation VSS = –5 V; Bipolar Operation</td>
</tr>
<tr>
<td>20</td>
<td>VDD</td>
<td>Positive Supply Voltage, +5 V</td>
</tr>
</tbody>
</table>
**TERMINOLOGY**

**LEAST SIGNIFICANT BIT (LSB)**
An ADC with 8-bit resolution can resolve one part in $2^8$ (1/256 of full scale). For the AD7821 operating in either the unipolar or bipolar input range with 5 V full scale, one LSB is 19.53 mV.

**TOTAL UNADJUSTED ERROR**
This is a comprehensive specification which includes relative accuracy, offset error, and full-scale error.

**SLEW RATE**
Slew rate is the maximum allowable rate of change of input signal such that the digital sample values are not in error.

**TOTAL HARMONIC DISTORTION (THD)**
Total harmonic distortion is the ratio of the square root of the sum of the squares of the rms value of the harmonics to the rms value of the fundamental. For the AD7821, total harmonic distortion is defined as

$$20 \log \left( \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1} \right) dB$$

where $V_1$ is the rms amplitude of the fundamental and $V_2$, $V_3$, $V_4$, $V_5$, and $V_6$ are the rms amplitudes of the individual harmonics.

**INTERMODULATION DISTORTION**
With inputs consisting of sine waves at two frequencies, $f_a$ and $f_b$, any active device with nonlinearities will create distortion products, of order $(m+n)$, at sum and difference frequencies of $m f_a + n f_b$, where $m, n = 0, 1, 2, 3, ...$. Intermodulation terms are those for which $m$ or $n$ is not equal to zero. For example, the second order terms include $(f_a + f_b)$ and $(f_a - f_b)$, and the third order terms include $(2f_a + f_b)$, $(2f_a - f_b)$, $(f_a + 2f_b)$ and $(f_a - 2f_b)$. For the AD7821 intermodulation distortion is calculated separately for both the second and third order terms.

**SIGNAL-TO-NOISE RATIO (SNR)**
Signal-to-noise ratio is measured signal-to-noise at the output of the ADC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all nonfundamental signals (excluding dc) up to half the sampling frequency. SNR is dependent on the number of quantization levels used in the digitization process. The theoretical SNR for a sine wave input is given by:

$$SNR = (6.02N + 1.76) dB$$

where $N$ is the number of bits in the ADC. Thus, for an ideal 8-bit ADC, SNR = 50 dB.

**PEAK HARMONIC OR SPURIOUS NOISE**
Peak harmonic or spurious noise is the rms value of the largest nonfundamental frequency (excluding dc) up to half the sampling frequency to the rms value of the fundamental.
AD7821—Typical Performance Characteristics

TPC 1. Conversion Time (RD Mode) vs. Temperature

TPC 2. Power Supply Current vs. Temperature (Not Including Reference Ladder)

TPC 3. Accuracy vs. tWR

TPC 4. Accuracy vs. tRD

TPC 5. Accuracy vs. tP

TPC 6. Accuracy vs. VREF
\[ V_{REF} = V_{REF(+) - V_{REF(-)}} \]

TPC 7. Effective Number of Bits vs. Input Signal (±2.5 V) Frequency

TPC 8. tINTL, Internal Time Delay vs. Temperature

TPC 9. Output Current vs. Temperature
CIRCUIT INFORMATION

BASIC DESCRIPTION

The AD7821 uses a half flash conversion technique (see Functional Block Diagram), whereby two 4-bit flash ADCs are used to achieve an 8-bit result. Each 4-bit flash ADC contains 15 comparators, which compare an unknown input voltage to the reference ladder, to achieve a 4-bit result. The MS (most significant) flash ADC converts an unknown analog input voltage (V_{IN}) to provide the 4 MS data bits. An internal DAC, driven by the 4 MS data bits, then recreates an analog approximation of the input voltage. The DAC output voltage is subtracted from the analog input, and the difference is converted by the LS (least significant) ADC to provide the 4 LS data bits. The MS flash ADC also has one additional comparator to detect over-range on the analog input.

OPERATING SEQUENCE

The AD7821 has two operating modes. The RD mode allows a conversion to be started and data to be read with a single, extended, READ operation (i.e., CS and RD are taken low). The conversion process is timed out by internal one-shots. The WR-RD mode uses WR to start a conversion and RD to read the data and allows the conversion timing to be externally controlled. The operating sequence for the WR-RD mode is shown in Figure 3.

REFERENCE AND INPUT

The V_{REF}(-) and V_{REF}(+) reference inputs on the AD7821 are fully differential and define the zero and full-scale input range of the ADC. The transfer characteristic of the part is defined by the integer value of the following expression:

\[
\text{Data (LSBs)} = 256 \left[ \frac{V_{IN} - V_{REF}(-)}{V_{REF}(+) - V_{REF}(-)} \right] + 0.5
\]

As a result, the analog input (V_{IN}) of the device can easily be set up to provide both unipolar and bipolar operation. The data output code for unipolar and bipolar operation is Natural Binary and Offset Binary, respectively.

The span of the analog input voltage can easily be varied. By reducing the reference span, V_{REF}(+) – V_{REF}(-), to less than 5 V, the sensitivity of the converter can be increased (i.e., if V_{REF} = 2 V then 1 LSB = 7.8 mV). The reference flexibility also allows the input span for unipolar operation to be offset from zero (V_{REF}(-) > GND). Additionally, the input/reference arrangement facilitates ratiometric operation.

Figures 4 and 5 show some configurations that are possible. For minimum noise, a 47 \mu F capacitor in parallel with a 0.1 \mu F capacitor should be connected between the reference inputs and GND.

INPUT CURRENT

The analog input of the AD7821 behaves somewhat differently than conventional ADCs. This is due to the ADC’s sampled data comparators, which take varying amounts of input current depending on the cycle of the converter.

The equivalent input circuit of the AD7821 is shown in Figure 6. When a conversion ends (e.g., falling edge of INT, WR-RD mode, tRD > tINTL) all the input switches are closed and V_{IN} is connected to the comparators of the internal LS and MS ADCs. Therefore, V_{IN} is simultaneously connected to 31 input capacitors of 1 pF each.
The input capacitors must charge to the input voltage through the on resistance of the analog switches (about 2 kΩ to 5 kΩ). In addition, about 12 pF of input stray capacitance must be charged.

The analog input can be modeled as an equivalent RC network as shown in Figure 7. As Rs (source impedance) increases, the input capacitance takes longer to charge.

The comparators track the analog input between conversions. A minimum delay time (tP) of 350 ns is required between conversions to allow for voltage source settling and comparator tracking time. This allows input time constants of 50 ns without settling time problems. Typical total input capacitance values of 55 pF allow Rs to be 0.9 kΩ without lengthening tP to give VIN more time to settle.

**INHERENT TRACK-AND-HOLD**

A major benefit of the AD7821’s input structure is its ability to measure a variety of high speed signals without the help of an external track-and-hold. Any ADC which does not have a built-in track-and-hold, regardless of its speed, requires the analog input to remain stable to at least 1/2 LSB for the duration of the conversion to maintain full accuracy. This requires the use of a track-and-hold whenever the input is a high-speed signal. The AD7821’s sampled-data comparators, by nature of their input switching, inherently accomplish this track-and-hold function. Although the conversion time for the AD7821 is 660 ns (WR-RD mode, tWR + tRD + tACC1), the time for which VIN must be stable to 1/2 LSB is much smaller. The AD7821 tracks VIN between conversions only, and its value on the falling edge of WR or RD in the WR-RD or RD modes, respectively, is the measured value.

**SINUSOIDAL INPUTS**

The bandwidth of the built-in track-and-hold is 100 kHz max (150 kHz typ, 5 V p-p). This is limited by the analog bandwidth of the comparators and timing skew between the comparator switches. This means that the analog input frequency can be up to 100 kHz without the aid of an external track-and-hold. The Nyquist criterion requires that the sampling rate be at least twice the input frequency (i.e., \( \geq 2 \times 100 \text{ kHz} \)). This requires an ideal antialiasing filter with an infinite roll-off. To ease the problem of antialiasing filter design, the sampling rate is usually set much greater than the Nyquist criterion. The maximum sampling rate (fMAX) for the AD7821 in the WR-RD mode, \( \langle \text{tRD} < \text{tINTL} \rangle \), can be calculated as follows:

\[
\begin{align*}
\text{f}_{\text{MAX}} &= \frac{1}{t_{WR} + t_{RD} + t_{RI} + t_{P}} \\
\text{t}_{WR} &= \text{Write Pulsewidth} \\
\text{t}_{RD} &= \text{Delay Time between WR and RD Pulses} \\
\text{t}_{RI} &= \text{RD to INT Delay} \\
\text{t}_{P} &= \text{Delay Time between Conversions}
\end{align*}
\]

This permits a maximum sampling rate for the AD7821 of 1 MHz, which is much greater than the Nyquist criterion for sampling a 100 kHz analog input signal.

**DIGITAL SIGNAL PROCESSING APPLICATIONS**

In Digital Signal Processing (DSP) application areas such as voice recognition, echo cancellation, and adaptive filtering, the dynamic characteristics (Signal-to-Noise Ratio, Harmonic Distortion, Intermodulation Distortion) of an ADC are critical. Since the AD7821 is a very fast ADC with a built-in track-and-hold function, it is specified dynamically as well as with standard dc specifications (Total Unadjusted Error, and so on).
**SIGNAL-TO-NOISE RATIO AND DISTORTION**

The dynamic performance of the AD7821 is evaluated by applying a very low distortion sine wave signal to the analog input (V_{IN}) which is then sampled at a 512 kHz sampling rate. A Fast Fourier Transform (FFT) plot is then generated from which Signal-to-Noise Ratio (SNR) and harmonic distortion data are obtained.

Figure 8 shows a 2048 point FFT plot of the AD7821 with an input signal of 100.25 kHz. The SNR is 49.1 dB. It should be noted that the harmonics are taken into account when calculating the SNR. The theoretical relationship between SNR and resolution (N) is expressed by the following equation:

\[ \text{SNR} = (6.02N + 1.76) \text{dB} \]  

\[ \text{SNR} = 60 \log_{10}(A^2 - V^2)^{1/2} \]

where \( A \) is the peak amplitude of the sine wave and \( P(V) \) is the probability of occurrence at a voltage \( V \).

If a particular step is wider than the ideal 1 LSB width, then the code associated with that step will accumulate more counts than for the code for an ideal step. Likewise, a step narrower than the ideal width will have fewer counts. Missing codes are easily seen because a missing code means zero counts for a particular code. The absence of large spikes in the plot indicates small differential nonlinearity.

Figure 10 shows a histogram plot for the AD7821, which corresponds very well with the ideal shape. The plot indicates very small differential nonlinearity and no missing codes for an input frequency of 100.25 kHz.

**EFFECTIVE NUMBER OF BITS**

By working backwards from Equation (1) it is possible to get a measure of ADC performance expressed in effective number of bits (N). A plot of the effective number of bits versus input frequency is given in the Typical Performance Characteristics section. The effective number of bits typically falls between 7.7 and 7.9, corresponding to SNR figures of 48.1 dB and 49.7 dB.

**INTERMODULATION DISTORTION**

For intermodulation distortion (IMD), an FFT plot consisting of very low distortion sine waves at two frequencies is generated by sampling an analog input applied to the ADC. Figure 9 shows a 2048 point plot for IMD.

**HISTOGRAM PLOT**

When a sine wave of specified frequency is applied to the V_{IN} input of the AD7821 and several thousand samples are taken, it is possible to plot a histogram showing the frequency of occurrence of each of the 256 ADC codes. A perfect ADC produces a probability density function described by the equation:

\[ P(V) = \frac{1}{\pi(A^2 - V^2)^{1/2}} \]

The two modes of operation given in the data sheet are suitable for DSP applications because the sampling instant of the AD7821 is well defined. V_{IN} is sampled on the falling edge of WR or RD in the WR-RD or RD modes, respectively.

**DIGITAL INTERFACE**

The AD7821 has two basic interface modes which are determined by the status of the MODE pin. When this pin is low, the converter is in the RD mode, with this pin high, the AD7821 is set up for the WR-RD mode.

The RD mode is designed for microprocessors that can be driven into a WAIT state. A READ operation (i.e., CS and RD are taken low) starts a conversion and data is read when the conversion is complete. The WR-RD mode does not require microprocessor WAIT states. A WRITE operation (i.e., CS and WR are taken low) initiates a conversion, and a READ operation reads the result when the conversion is complete.
**AD7821**

**RD Mode (MODE = 0)**

The timing diagram for the RD mode is shown in Figure 11. This mode is intended for use with microprocessors that have a WAIT state facility, whereby a READ instruction cycle can be extended to accommodate slow memory devices. A conversion is started by taking CS and RD low (READ operation). Both CS and RD are then kept low until output data appears.

![Figure 11. RD Mode](image)

In this mode, Pin 6 of the AD7821 is configured as a status output, RDY. This RDY output can be used to drive the processor READY or WAIT input. It is an open-drain output (no internal-pull-up device) which goes low after the falling edge of CS and goes high impedance at the end of conversion. An INT line is also provided which goes low when a conversion is complete. INT returns high on the rising edge of CS or RD.

**WR-RD Mode (MODE = 1)**

In the WR-RD mode, Pin 6 is configured as a WRITE (WR) input for the AD7821. With CS low, conversion is initiated on the falling edge of WR. Two options exist for reading data from the converter.

In the first of these options the processor waits for the INT status line to go low before reading the data (see Figure 12a).

INT typically goes low within 380 ns after the rising edge of WR. It indicates that conversion is complete and that the data result is in the output latch. With CS low, the data outputs (DB0–DB7) are activated when RD goes low. INT is reset by the rising edge of RD or CS.

![Figure 12a. WR-RD Mode (tRD > tINTL)](image)

The alternative option can be used to shorten the conversion time. This is a method for bypassing the internal time-out circuit. The INT line is ignored and RD can be brought low 250 ns after the rising edge of WR. In this case RD going low transfers the data result into the output latch and activates the data output (DB0–DB7). INT is driven low on the falling edge of RD and is reset on the rising edge of RD or CS. The timing for this interface is shown in Figure 12b.

![Figure 12b. WR-RD Mode (tRD < tINTL)](image)

The AD7821 can also be used in standalone operation in the WR-RD mode. CS and RD are tied low, and a conversion is initiated by bringing WR low. Output data is valid 530 ns (tINTL + tRD) after the rising edge of WR. The timing diagram for this mode is shown in Figure 13.

![Figure 13. WR-RD Mode Stand-Alone Operation, CS = RD = 0](image)
MICROPROCESSOR INTERFACING
The AD7821 is designed for easy interfacing to microprocessors as a memory mapped peripheral or an I/O device. This reduces to a minimum the amount of external logic required for interfacing.

AD7821 – 68008 INTERFACE
Figure 14 shows an AD7821 interface to the 68008 microprocessor. The ADC is configured for the RD interface mode. This means that one read instruction starts a conversion and reads the result when the conversion is completed. The read cycle is stretched out over the entire conversion period by taking the INT line back to the DTACK input of the 68008. Starting a conversion and reading the relevant data consists of a <MOVE B Dn, addr> instruction, where addr is the decoded ADC address and Dn is the data register into which the result is placed.

AD7821 – 8088 INTERFACE
A typical interface to the 8088 is shown in Figure 15. The AD7821 is configured for the RD interface mode. One read instruction starts a conversion and reads the result. The read cycle is stretched out over the entire conversion period by taking the RDY line back to the READY input of the 8088. Starting a conversion and reading the result consists of a <MOVE AX, (addr)> instruction, where addr is the decoded ADC address and AX is the 8088 data register into which the conversion result is placed.

AD7821 – TMS32010 INTERFACE
A typical interface to the TMS32010 is shown in Figure 16. The AD7821 is mapped at a port address and the interface is designed for the maximum TMS32010 clock frequency of 20 MHz. In this case, the AD7821 is configured in the WR-RD interface mode. This means that a write instruction starts a conversion and a read instruction reads the result when the conversion is completed. A precise timer or clock source is used to start a conversion in applications requiring equidistant sampling intervals. The scheme used, whereby the AD7821 generates an interrupt to the TMS32010, is limited in that it does not allow the AD7821 to be sampled at its maximum rate. This is because the time between samples has to be long enough to allow the TMS32010 to service its interrupt and read data from the AD7821. Constant interruption of the TMS32010 by the AD7821, every time the ADC completes a conversion, is not a very efficient use of the processor time. To overcome these problems, some buffer memory or FIFO could be placed between the AD7821 and the TMS32010. The INT line of the AD7821 could be used to trigger a pulse which drives its CS and RD lines and places the AD7821 data into a FIFO or buffer memory. The microprocessor can then read a batch of data from the FIFO or buffer memory at some convenient time. Reading data from the AD7821, after an INT has been received, consists of a <IN A, PA> instruction (PA is the decoded ADC address).

AD7821 – 8051 INTERFACE
Figure 17 shows the AD7821 interface to the 8051 microcomputer. The AD7821 is configured in the WR-RD interface mode and is connected to the 8051 ports. The processor starts conversion and then polls INT, until it goes low, before reading the conversion result. Data is read from the AD7821 by using the <MOV A, 90H> instruction (90H is the address for Port 1).
APPLYING THE AD7821
The AD7821 is specified for a unipolar input range of 0 V to +5 V and a bipolar input range of –2.5 V to +2.5 V. The \( V_{\text{REF}}(\text{–}) \) and \( V_{\text{REF}}(+) \) voltages required for these input ranges are outlined below. See the Typical Performance Characteristics section for operation with unspecified input voltage ranges.

**UNIPOLAR OPERATION**
Figure 18 gives the configuration and reference voltages required for 0 V to +5 V operation. The nominal transfer characteristic for this input range is shown in Figure 19. The output code is Natural Binary with 1 LSB = \((5/256) \) V = 19.5 mV.

**BIPOLAR OPERATION**
Figure 18 gives the configuration and reference voltages required for –2.5 V to +2.5 V operation. The nominal transfer characteristic for this input range is shown in Figure 20. The output code is Offset Binary with 1 LSB = \( ([+2.5 - (-2.5)]/256) \) V = 19.5 mV.

**16-CHANNEL TELECOM A/D CONVERTER**
The fast sampling rate (1 MHz) and bipolar operation of the AD7821 makes it useful in telecom applications for sampling a number of input channels using a multiplexer. Figure 21 shows a circuit for such an application.

The maximum signal frequency required for acceptable quality in telecom applications is 3 kHz. The circuit given in Figure 21 permits each of the 16-input channels to be sampled at a rate of 16 kHz maximum. The sampling rate takes into account such multiplexer parameters as \( t_{\text{ON}} \), settling time, and so on. The circuit also eases the problem of the antialiasing filter design by sampling at a rate much greater than that required by the Nyquist criterion.

---

Figure 18. Unipolar/Bipolar Operation

Figure 19. Nominal Transfer Characteristic for Unipolar (0 V to +5 V) Operation

Figure 20. Nominal Transfer Characteristic for Bipolar (–2.5 V to +2.5 V) Operation
SIMULTANEOUS SAMPLING ADCs

The AD7821’s inherent track-and-hold and well defined sampling instant makes it useful in such applications as sonar, where a number of input channels are required to be sampled simultaneously. Figure 22 shows a circuit for such an application.

The actual sampling instant at which $V_{in}$ is measured occurs approximately 50 ns after the falling edge of WR or RD in the WR-RD or RD modes, respectively, due to internal logic delays. However, the internal logic delay and, therefore, the sampling instant can vary from device to device, but is typically within ±5 ns. This means that a maximum common input sine wave of ±2.5 V at 32 kHz, applied to any number of AD7821s in the circuit of Figure 22, will yield a maximum difference between the converter outputs of typically ±1/4 LSB.
OUTLINE DIMENSIONS

Dimensions shown in inches and (millimeters)

20-Lead Ceramic DIP - Glass Hermetic Seal [CERDIP] (Q-20)
Dimensions shown in inches and (millimeters)

20-Terminal Ceramic Leaded Chip Carrier [LCC] (E-20A)
Dimensions shown in millimeters and (inches)

Dimensions shown in millimeters and (inches)
Revision History

<table>
<thead>
<tr>
<th>Location</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>10/02—Data Sheet changed from REV. A to REV. B.</td>
<td></td>
</tr>
<tr>
<td>Update Format</td>
<td>1</td>
</tr>
<tr>
<td>Changes to FUNCTIONAL BLOCK DIAGRAM</td>
<td>2</td>
</tr>
<tr>
<td>Edit to SPECIFICATIONS</td>
<td>5</td>
</tr>
<tr>
<td>Change to TOTAL HARMONIC DISTORTION formula</td>
<td>7</td>
</tr>
<tr>
<td>Changes to INPUT CURRENT section</td>
<td>8</td>
</tr>
<tr>
<td>Change to Figure 7</td>
<td>8</td>
</tr>
<tr>
<td>Change to formula in SINUSOIDAL INPUTS section</td>
<td>14</td>
</tr>
</tbody>
</table>

OUTLINE DIMENSIONS

20-Lead Plastic Leaded Chip Carrier [PLCC] (P-20A)
Dimensions shown in inches and (millimeters)