

1.1 Scope.

This specification covers the detail requirements for a programmable gain instrumentation amplifier. The gain equation is $\frac{40,000}{R_G} + 1 \pm 20\%$ with external resistor gain programming.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD624SD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-16.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 18\text{V}$
Internal Power Dissipation	280mW
Rated Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature Range (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 22^\circ\text{C}/\text{W}$
 $\theta_{JA} = 95^\circ\text{C}/\text{W}$

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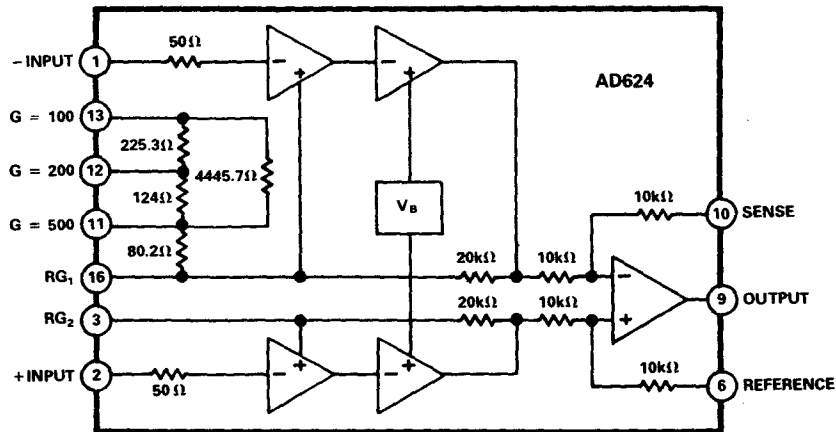
Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Gain Error 1	GE ₁	-1	0.05	0.05			G = 1, V _O = ±10V	±% max
Gain Error 100	GE ₁₀₀	-1	0.25	0.25			G = 100, V _O = ±10V	±% max
Gain Error 200	GE ₂₀₀	-1	0.5	0.5			G = 200, V _O = ±10V	±% max
Gain Error 500	GE ₅₀₀	-1	0.5	0.5			G = 500, V _O = ±10V	±% max
Gain Error Drift 1	TCGE ₁	-1	5				G = 1, V _O = ±10V	± ppm/°C max
Gain Error Drift 100	TCGE ₁₀₀	-1	10				G = 100, V _O = ±10V	± ppm/°C max
Gain Error Drift 200	TCGE ₂₀₀	-1	10				G = 200, V _O = ±10V	± ppm/°C max
Gain Error Drift 500	TCGE ₅₀₀	-1	15				G = 500, V _O = ±10V	± ppm/°C max
Input Offset Voltage	V _{OSI}	-1	75	75			V _{IN} = 0V	± μV max
Input Offset Voltage Drift	TCV _{OSI}	-1	2		2		G = 500, V _{IN} = 0V	± μV/°C max
Output Offset Voltage	V _{OSO}	-1	3	3			V _{IN} = 0V	± mV max
Output Offset Drift	TCV _{OSO}	-1	50		50		G = 1, V _{IN} = 0V	± μV/°C max
Input Bias Current	I _B	-1	50	50			G = 1	± nA max
Input Offset Current	I _{OS}	-1	35	35			G = 1	± nA max
Common-Mode Rejection	+CMRR ₁	-1	70	70			G = 1, V _{IN} = 0V to +10V	dB min
Common-Mode Rejection	-CMRR ₁	-1	70	70			G = 1, V _{IN} = 0V to -10V	dB min
Common-Mode Rejection	+CMRR ₁₀₀	-1	100	100			G = 100, V _{IN} = 0V to +10V	dB min
Common-Mode Rejection	-CMRR ₁₀₀	-1	100	100			G = 100, V _{IN} = 0V to -10V	dB min
Common-Mode Rejection	+CMRR ₂₀₀	-1	100	100			G = 200, V _{IN} = 0V to +10V	dB min
Common-Mode Rejection	-CMRR ₂₀₀	-1	100	100			G = 200, V _{IN} = 0V to -10V	dB min
Common-Mode Rejection	+CMRR ₅₀₀	-1	110	110			G = 500, V _{IN} = 0V to +10V	dB min
Common-Mode Rejection	-CMRR ₅₀₀	-1	110	110			G = 500, V _{IN} = 0V to -10V	dB min
Power Supply Current	I _{CC}	-1	5	5			G = 1	mA max
Power Supply Rejection	PSRR ₁	-1	75	75			G = 1, V _S = ±12V, ±15V	dB min
Power Supply Rejection	PSRR ₁₀₀	-1	105	105			G = 100, V _S = ±12V, ±15V	dB min
Power Supply Rejection	PSRR ₂₀₀	-1	105	105			G = 200, V _S = ±12V, ±15V	dB min
Power Supply Rejection	PSRR ₅₀₀	-1	110	110			G = 500, V _S = ±12V, ±15V	dB min

NOTE

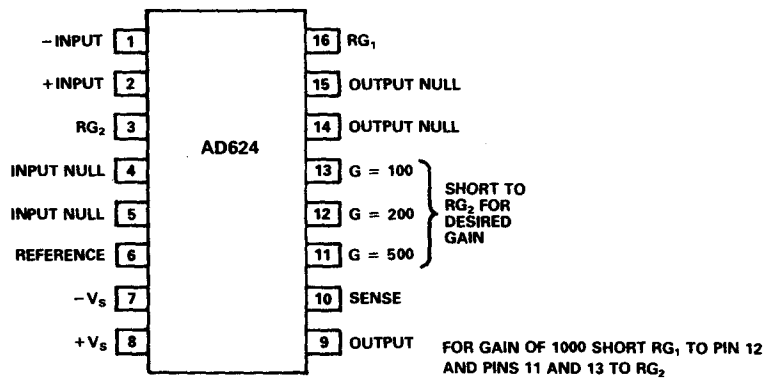
¹V_S = ±15V, R_L = 2kΩ unless otherwise specified.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



Pin Assignments



3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

