Dual 1.3GHz to 2.3GHz High Dynamic Range Downconverting Mixer

FEATURES

- **Conversion Gain: 8.5dB at 1950MHz**
- **IIP3: 26.2dBm at 1950MHz**
- **Noise Figure: 9.9dB at 1950MHz**
- **15.5dB NF Under 5dBm Blocking**
- **High Input P1dB**
- **47dB Channel-to-Channel Isolation**
- **1.25W Power Consumption at 3.3V**
- **Low Power Mode: <800mW Consumption**
- **Independent Channel Shutdown Control**
- **50Ω Single-Ended RF and LO Inputs**
- **LO Input Matched In All Modes**
- **0dBm LO Drive Level**
- **Small Package and Solution Size**
- **–40°C to 105°C Operation**

APPLICATIONS

- 3G/4G Wireless Infrastructure Diversity Receivers (LTE, W-CDMA, TD-SCDMA, UMTS, GSM1800)
- Remote Radio Unit
- MIMO Multichannel Receivers

DESCRIPTION

The LTC®5591 is part of a family of dual-channel high dynamic range, high gain downconverting mixers covering the 600MHz to 4.5GHz RF frequency range. **The LTC5591 is optimized for 1.3GHz to 2.3GHz RF applications. The LO frequency must fall within the 1.4GHz to 2.1GHz range for optimum performance.** A typical application is a LTE or W-CDMA multichannel or diversity receiver with a 1.7GHz to 2.2GHz RF input and low side LO.

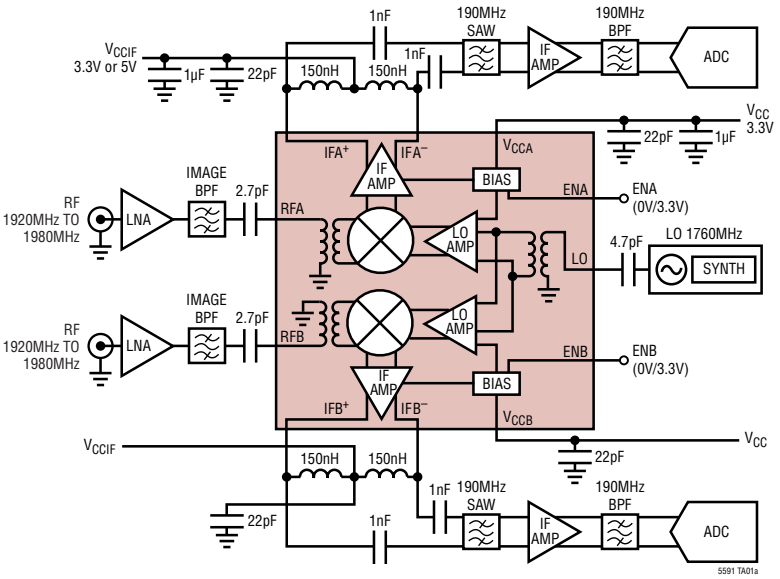
The LTC5591's high conversion gain and high dynamic range enable the use of lossy IF filters in high selectivity receiver designs, while minimizing the total solution cost, board space and system-level variation. A low current mode is provided for additional power savings and each of the mixer channels has independent shutdown control.

High Dynamic Range Dual Downconverting Mixer Family

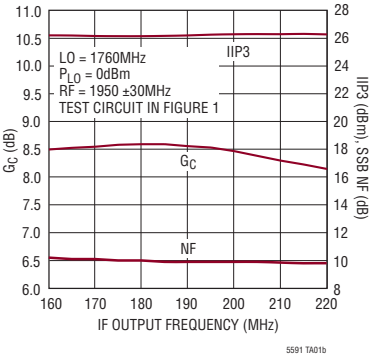
PART NUMBER	RF RANGE	LO RANGE
LTC5590	600MHz to 1.7GHz	700MHz to 1.5GHz
LTC5591	**1.3GHz to 2.3GHz**	**1.4GHz to 2.1GHz**
LTC5592	1.6GHz to 2.7GHz	1.7GHz to 2.5GHz
LTC5593	2.3GHz to 4.5GHz	2.1GHz to 4.2GHz

TYPICAL APPLICATION

Wideband Receiver



Wideband Conversion Gain, IIP3 and NF vs IF Frequency
(Mixer Only, Measured on Evaluation Board)

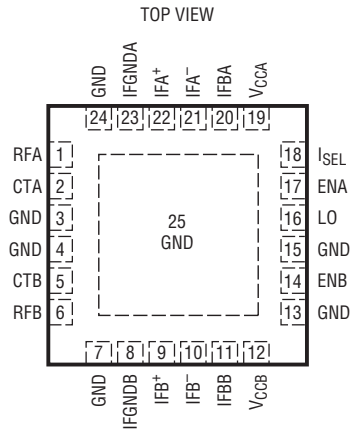


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 4.0V
IF Supply Voltage (V_{CCIF}) 5.5V
Enable Voltage (ENA, ENB) ..... –0.3V to V_{CC} + 0.3V
Bias Adjust Voltage (IFBA, IFBB) ..... –0.3V to V_{CC} + 0.3V
Power Select Voltage (I_{SEL}) ..... –0.3V to V_{CC} + 0.3V
LO Input Power (1GHz to 3GHz) 9dBm
LO Input DC Voltage ..... ±0.1V
RFA, RFB Input Power (1GHz to 3GHz) 15dBm
RFA, RFB Input DC Voltage ..... ±0.1V
Operating Temperature Range (T_C) ..... –40°C to 105°C
Storage Temperature Range ..... –65°C to 150°C
Junction Temperature (T_J) ..... 150°C

PIN CONFIGURATION



UH PACKAGE
24-LEAD (5mm × 5mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JC} = 7°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC5591IUH#PBF	LTC5591IUH#TRPBF	5591	24-Lead (5mm × 5mm) Plastic QFN	–40°C to 105°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, V_{CCIF} = 3.3V, ENA = ENB = High, I_{SEL} = Low, T_C = 25°C, unless otherwise noted. Test circuit shown in Figure 1. (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Requirements (V_{CCA}, V_{CCB}, V_{CCIFA}, V_{CCIFB})					
V_{CCA}, V_{CCB} Supply Voltage (Pins 12, 19)		3.1	3.3	3.5	V
V_{CCIFA}, V_{CCIFB} Supply Voltage (Pins 9, 10, 21, 22)		3.1	3.3	5.3	V
Mixer Supply Current (Pins 12, 19)	Both Channels Enabled		182	218	mA
IF Amplifier Supply Current (Pins 9, 10, 21, 22)	Both Channels Enabled		200	240	mA
Total Supply Current (Pins 9, 10, 12, 19, 21, 22)	Both Channels Enabled		382	458	mA
Total Supply Current – Shutdown	ENA = ENB = Low			500	µA
Enable Logic Input (ENA, ENB) High = On, Low = Off					
ENA, ENB Input High Voltage (On)		2.5			V
ENA, ENB Input Low Voltage (Off)				0.3	V
ENA, ENB Input Current	–0.3V to V_{CC} + 0.3V	–20		30	µA
Turn On Time			0.9		µs
Turn Off Time			1		µs

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, V_{CCIF} = 3.3V, ENA = ENB = High, I_{SEL} = Low, T_C = 25°C, unless otherwise noted. Test circuit shown in Figure 1. (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Low Current Mode Logic Input (I_{SEL}) High = Low Power, Low = Normal Power Mode					
I_{SEL} Input High Voltage		2.5			V
I_{SEL} Input Low Voltage				0.3	V
I_{SEL} Input Current	–0.3V to V_{CC} + 0.3V	–20		30	µA
Low Current Mode Current Consumption (I_{SEL} = High)					
Mixer Supply Current (Pins 12, 19)	Both Channels Enabled		119	143	mA
IF Amplifier Supply Current (Pins 9, 10, 21, 22)	Both Channels Enabled		120	144	mA
Total Supply Current (Pins 9, 10, 12, 19, 21, 22)	Both Channels Enabled		239	287	mA

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, V_{CCIF} = 3.3V, ENA = ENB = High, I_{SEL} = Low, T_C = 25°C, P_{LO} = 0dBm, P_{RF} = –3dBm (Δf = 2MHz for two tone IIP3 tests), unless otherwise noted. Test circuit shown in Figure 1. (Notes 2, 3, 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LO Input Frequency Range			1400 to 2100		MHz
RF Input Frequency Range	Low Side LO High Side LO		1600 to 2300 1300 to 1800		MHz MHz
IF Output Frequency Range	Requires External Matching		5 to 500		MHz
RF Input Return Loss	Z_O = 50Ω, 1300MHz to 2300MHz		>12		dB
LO Input Return Loss	Z_O = 50Ω, 1400MHz to 2100MHz		>12		dB
IF Output Impedance	Differential at 190MHz		300Ω||2.3pF		R||C
LO Input Power	f_{LO} = 1400MHz to 2100MHz	–4	0	6	dBm
LO to RF Leakage	f_{LO} = 1400MHz to 2100MHz		<–30		dBm
LO to IF Leakage	f_{LO} = 1400MHz to 2100MHz		<–30		dBm
RF to LO Isolation	f_{RF} = 1300MHz to 2300MHz		>45		dB
RF to IF Isolation	f_{RF} = 1300MHz to 2300MHz		>30		dB
Channel-to-Channel Isolation	f_{RF} = 1750MHz to 2150MHz		>47		dB

Low Side LO Downmixer Application: I_{SEL} = Low, RF = 1700MHz to 2300MHz, IF = 190MHz, $f_{LO} = f_{RF} – f_{IF}$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Conversion Gain	RF = 1750MHz RF = 1950MHz RF = 2150MHz	7.0	8.7 8.5 8.0		dB dB dB
Conversion Gain Flatness	RF = 1950 ±30MHz, LO = 1760MHz, IF = 190 ±30MHz		±0.25		dB
Conversion Gain vs Temperature	T_C = –40°C to 105°C, RF = 1950MHz		–0.006		dB/°C
Input 3rd Order Intercept	RF = 1750MHz RF = 1950MHz RF = 2150MHz	24.0	26.9 26.2 26.2		dBm dBm dBm
SSB Noise Figure	RF = 1750MHz RF = 1950MHz RF = 2150MHz		9.4 9.9 10.8		dB dB dB

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, V_{CCIF} = 3.3V, ENA = ENB = High, T_C = 25°C, P_{LO} = 0dBm, P_{RF} = –3dBm (Δf = 2MHz for two tone IIP3 tests), unless otherwise noted. Test circuit shown in Figure 1. (Notes 2, 3)

Low Side LO Downmixer Application: I_{SEL} = Low, RF = 1700MHz to 2300MHz, IF = 190MHz, $f_{LO} = f_{RF} – f_{IF}$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SSB Noise Figure Under Blocking	f_{RF} =1950MHz, f_{LO} = 1760MHz, f_{BLOCK} = 2050MHz, P_{BLOCK} = 5dBm P_{BLOCK} = 10dBm		 15.5 20.2		 dB dB
2RF-2LO Output Spurious Product ($f_{RF} = f_{LO} + f_{IF}/2$)	f_{RF} = 1855MHz at –10dBm, f_{LO} = 1760MHz, f_{IF} = 190MHz		–69		dBc
3RF-3LO Output Spurious Product ($f_{RF} = f_{LO} + f_{IF}/3$)	f_{RF} = 1823.33MHz at –10dBm, f_{LO} = 1760MHz, f_{IF} = 190MHz		–74		dBc
Input 1dB Compression	f_{RF} = 1950MHz, V_{CCIF} = 3.3V f_{RF} = 1950MHz, V_{CCIF} = 5V		10.7 13.9		dBm dBm

Low Power Mode, Low Side LO Downmixer Application: I_{SEL} = High, RF = 1700MHz to 2300MHz, IF = 190MHz, $f_{LO} = f_{RF} – f_{IF}$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Conversion Gain	RF = 1950MHz		7.2		dB
Input 3rd Order Intercept	RF = 1950MHz		21.4		dBm
SSB Noise Figure	RF = 1950MHz		10.3		dB
Input 1dB Compression	RF = 1950MHz, V_{CCIF} = 3.3V RF = 1950MHz, V_{CCIF} = 5V		10.7 11.7		dBm dBm

High Side LO Downmixer Application: I_{SEL} = Low, RF = 1300MHz to 1800MHz, IF = 190MHz, $f_{LO} = f_{RF} + f_{IF}$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Conversion Gain	RF = 1450MHz RF = 1600MHz RF = 1750MHz		8.9 8.6 8.4		dB dB dB
Conversion Gain Flatness	RF = 1600 ±30MHz, LO = 1790MHz, IF = 190 ±30MHz		±0.1		dB
Conversion Gain vs Temperature	T_C = –40°C to 105°C, RF = 1600MHz		–0.007		dB/°C
Input 3rd Order Intercept	RF = 1450MHz RF = 1600MHz RF = 1750MHz		25.0 24.6 24.3		dBm dBm dBm
SSB Noise Figure	RF = 1450MHz RF = 1600MHz RF = 1750MHz		10.0 10.1 10.1		dB dB dB
SSB Noise Figure Under Blocking	f_{RF} = 1600MHz, f_{LO} = 1790MHz, f_{BLOCK} = 1500MHz, P_{BLOCK} = 5dBm P_{BLOCK} = 10dBm		 16.4 21.2		 dB dB
2LO-2RF Output Spurious Product ($f_{RF} = f_{LO} – f_{IF}/2$)	f_{RF} = 1695MHz at –10dBm, f_{LO} = 1790MHz, f_{IF} = 190MHz		–64		dBc
3LO-3RF Output Spurious Product ($f_{RF} = f_{LO} – f_{IF}/3$)	f_{RF} = 1726.67MHz at –10dBm, f_{LO} = 1790MHz, f_{IF} = 190MHz		–75		dBc
Input 1dB Compression	RF = 1600MHz, V_{CCIF} = 3.3V RF = 1600MHz, V_{CCIF} = 5V		10.2 13.6		dBm dBm

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC5591 is guaranteed functional over the case operating temperature range of –40°C to 105°C. (θ_{JC} = 7°C/W)

Note 3: SSB Noise Figure measured with a small-signal noise source, bandpass filter and 6dB matching pad on RF input, bandpass filter and 6dB matching pad on the LO input, and no other RF signals applied.

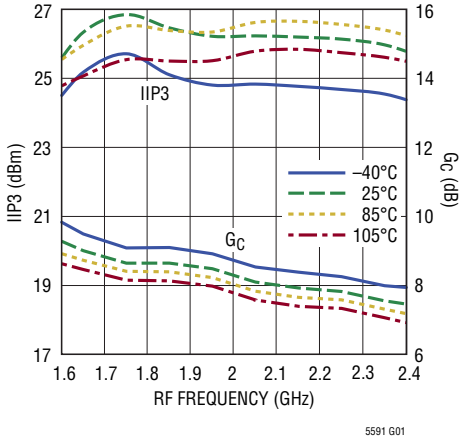
Note 4: Channel A to channel B isolation is measured as the relative IF output power of channel B to channel A, with the RF input signal applied to channel A. The RF input of channel B is 50Ω terminated and both mixers are enabled.

TYPICAL AC PERFORMANCE CHARACTERISTICS

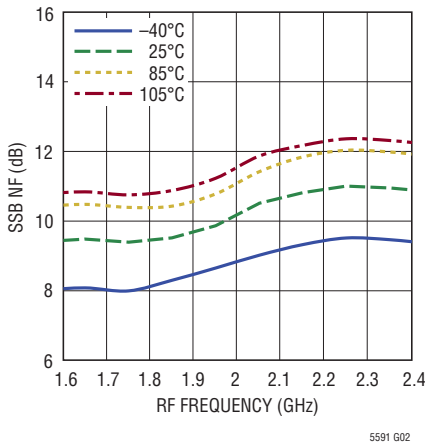
Low Side LO

V_{CC} = 3.3V, V_{CCIF} = 3.3V, ENA = ENB = High, I_{SEL} = Low, T_C = 25°C, P_{LO} = 0dBm, P_{RF} = –3dBm (–3dBm/tone for two-tone IIP3 tests, Δf = 2MHz), IF = 190MHz, unless otherwise noted. Test circuit shown in Figure 1.

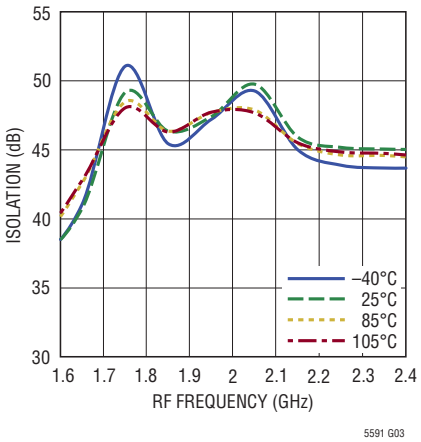
Conversion Gain and IIP3 vs RF Frequency



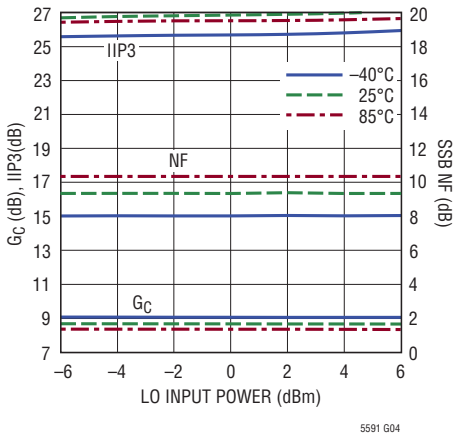
SSB NF vs RF Frequency



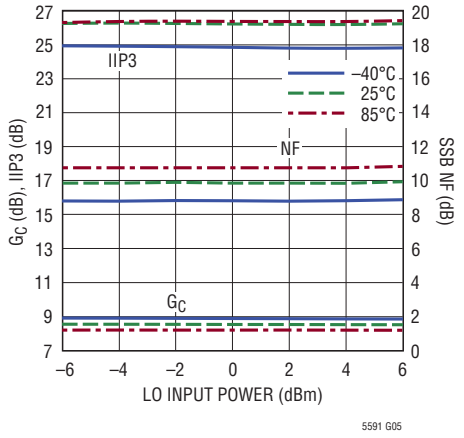
Channel Isolation vs RF Frequency



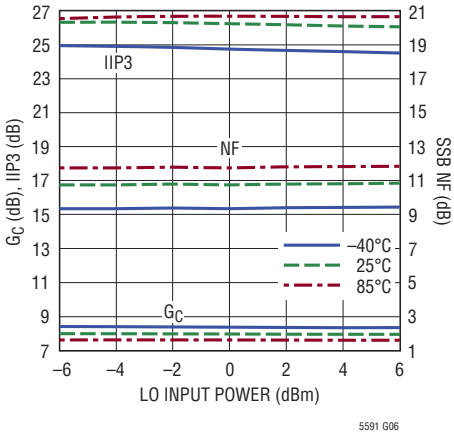
1750MHz Conversion Gain, IIP3 and NF vs LO Power



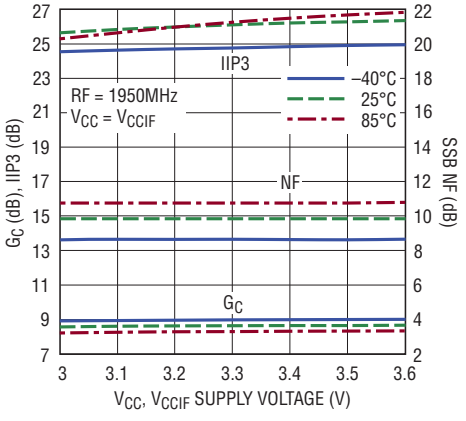
1950MHz Conversion Gain, IIP3 and NF vs LO Power



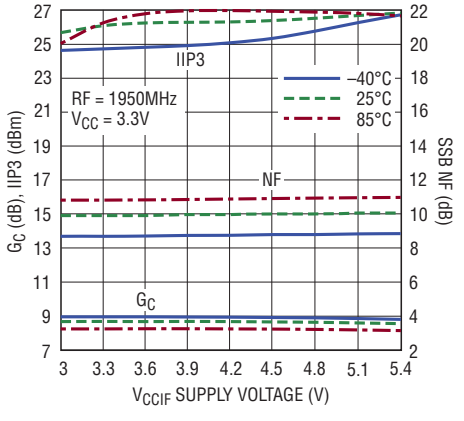
2150MHz Conversion Gain, IIP3 and NF vs LO Power



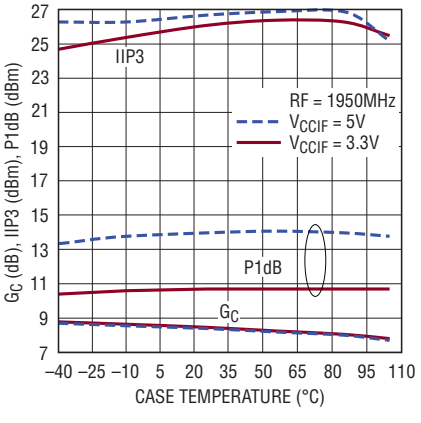
Conversion Gain, IIP3 and NF vs Supply Voltage (Single Supply)



Conversion Gain, IIP3 and NF vs IF Supply Voltage (Dual Supply)



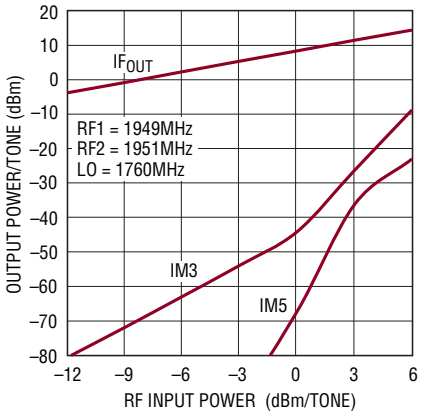
Conversion Gain, IIP3 and RF Input P1dB vs Temperature



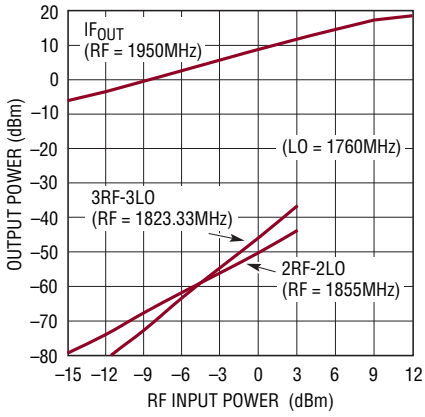
TYPICAL AC PERFORMANCE CHARACTERISTICS Low Side LO (continued)

V_{CC} = 3.3V, V_{CCIF} = 3.3V, ENA = ENB = High, I_{SEL} = Low, T_C = 25°C, P_{LO} = 0dBm, P_{RF} = –3dBm (–3dBm/tone for two-tone IIP3 tests, Δf = 2MHz), IF = 190MHz, unless otherwise noted. Test circuit shown in Figure 1.

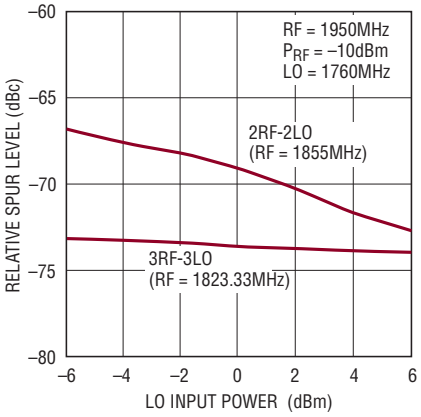
2-Tone IF Output Power, IM3 and IM5 vs RF Input Power



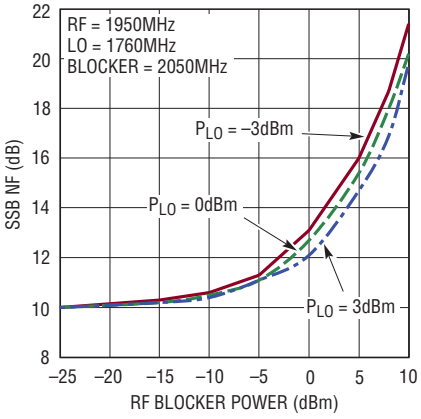
Single-Tone IF Output Power, 2 × 2 and 3 × 3 Spurs vs RF Input Power



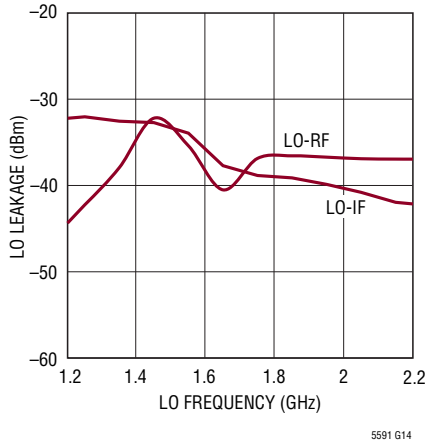
2 × 2 and 3 × 3 Spurs vs LO Power



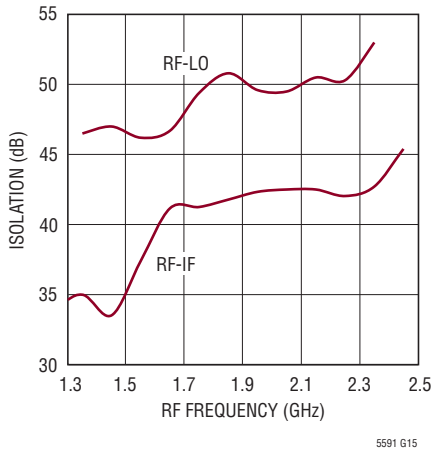
SSB Noise Figure vs RF Blocker Power



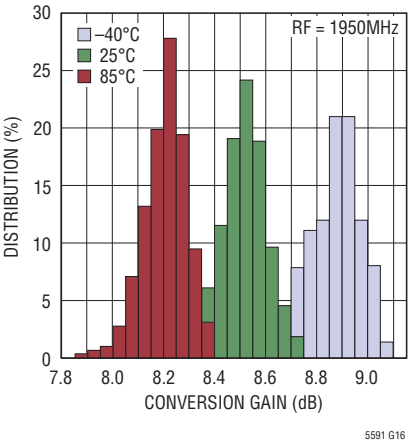
LO Leakage vs LO Frequency



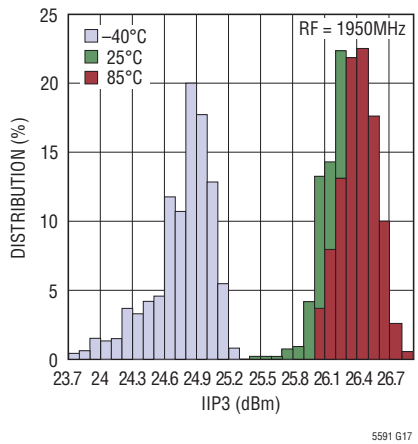
RF Isolation vs RF Frequency



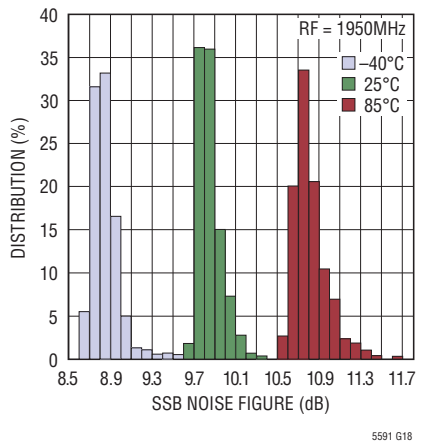
Conversion Gain Distribution



IIP3 Distribution



SSB Noise Figure Distribution

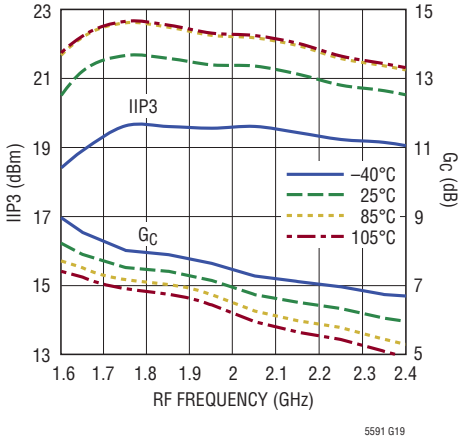


TYPICAL AC PERFORMANCE CHARACTERISTICS

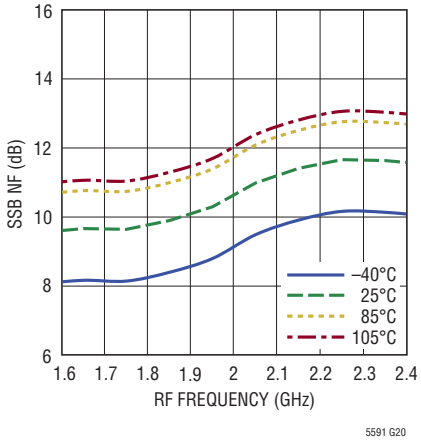
Low Power Mode, Low Side LO

V_{CC} = 3.3V, V_{CCIF} = 3.3V, ENA = ENB = High, I_{SEL} = High, T_C = 25°C, P_{LO} = 0dBm, P_{RF} = –3dBm (–3dBm/tone for two-tone IIP3 tests, Δf = 2MHz), IF = 190MHz, unless otherwise noted. Test circuit shown in Figure 1.

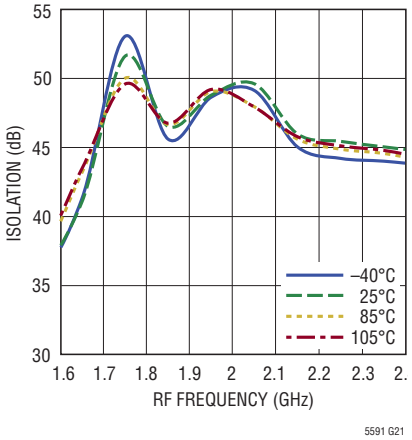
Conversion Gain and IIP3 vs RF Frequency



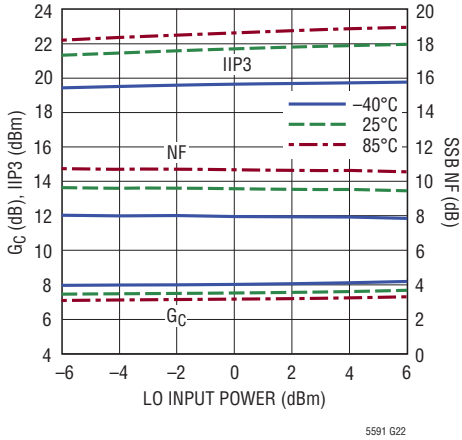
SSB NF vs RF Frequency



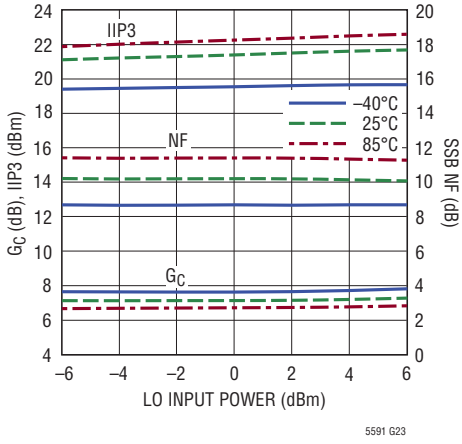
Channel Isolation vs RF Frequency



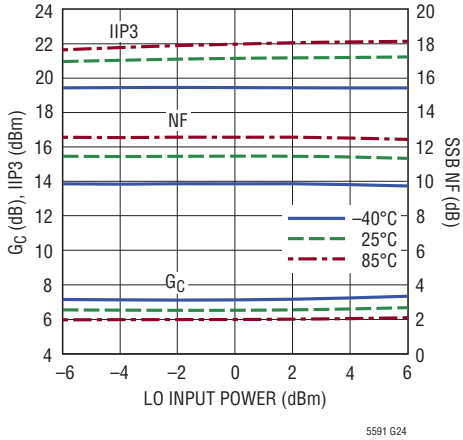
1750MHz Conversion Gain, IIP3 and NF vs LO Power



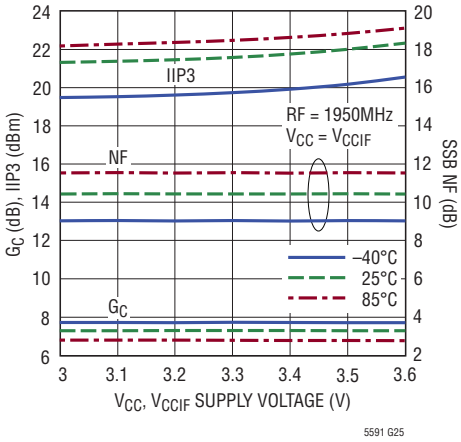
1950MHz Conversion Gain, IIP3 and NF vs LO Power



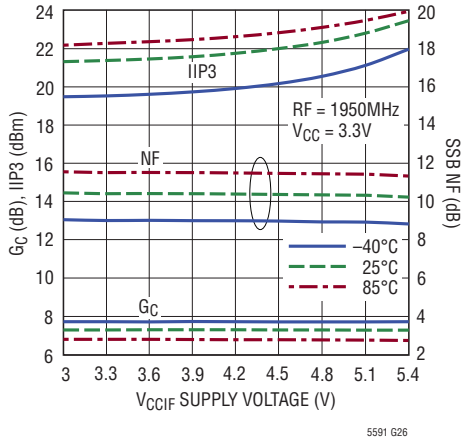
2150MHz Conversion Gain, IIP3 and NF vs LO Power



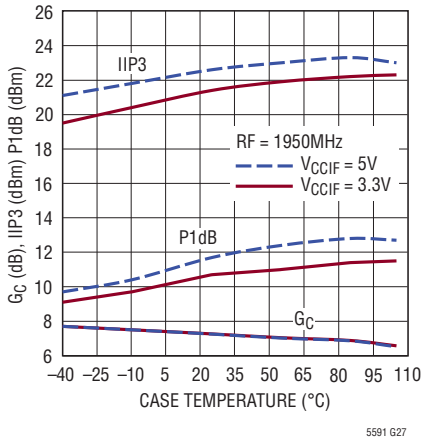
Conversion Gain, IIP3 and NF vs Supply Voltage (Single Supply)



Conversion Gain, IIP3 and NF vs IF Supply Voltage (Dual Supply)



Conversion Gain, IIP3 and RF Input P1dB vs Temperature

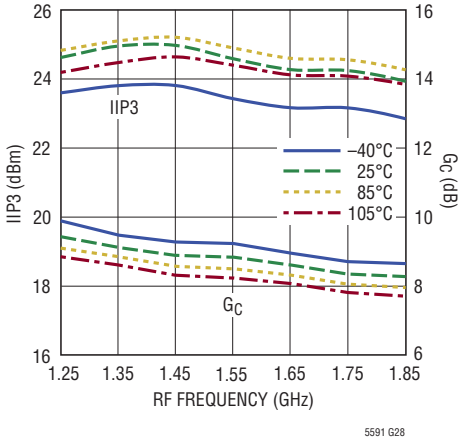


TYPICAL AC PERFORMANCE CHARACTERISTICS

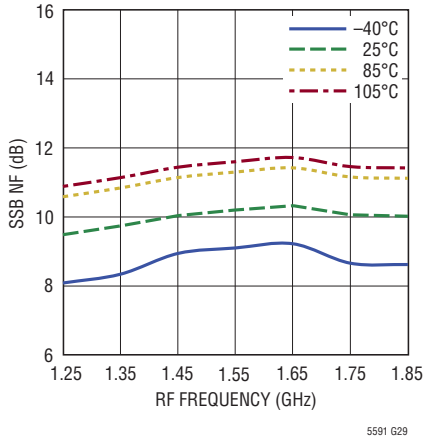
High Side LO

V_{CC} = 3.3V, V_{CCIF} = 3.3V, ENA = ENB = High, I_{SEL} = Low, T_C = 25°C, P_{LO} = 0dBm, P_{RF} = –3dBm (–3dBm/tone for two-tone IIP3 tests, Δf = 2MHz), IF = 190MHz, unless otherwise noted. Test circuit shown in Figure 1.

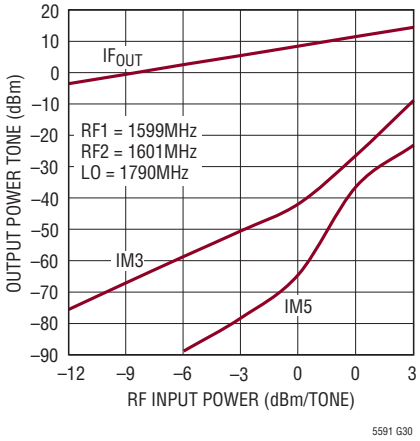
Conversion Gain and IIP3 vs RF Frequency



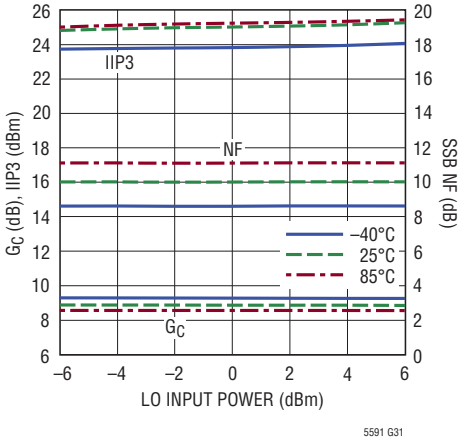
SSB NF vs RF Frequency



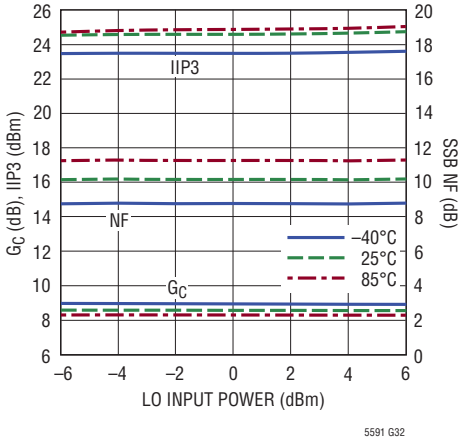
2-Tone IF Output Power, IM3 and IM5 vs RF Input Power



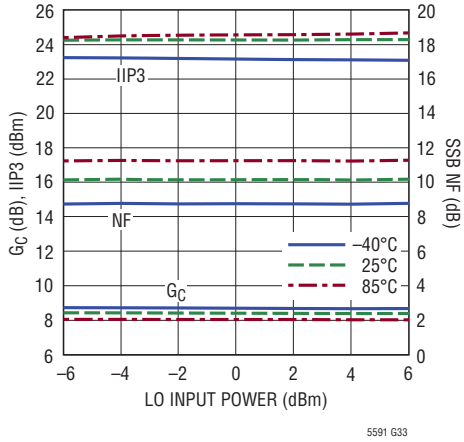
1450MHz Conversion Gain, IIP3 and NF vs LO Power



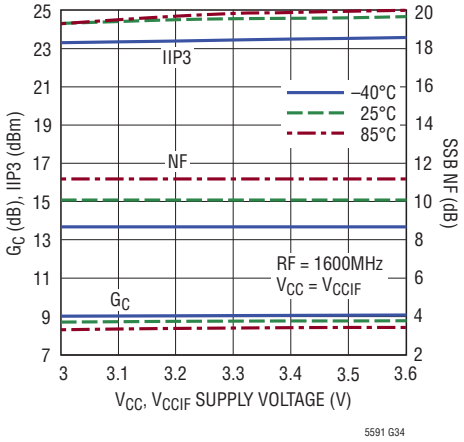
1600MHz Conversion Gain, IIP3 and NF vs LO Power



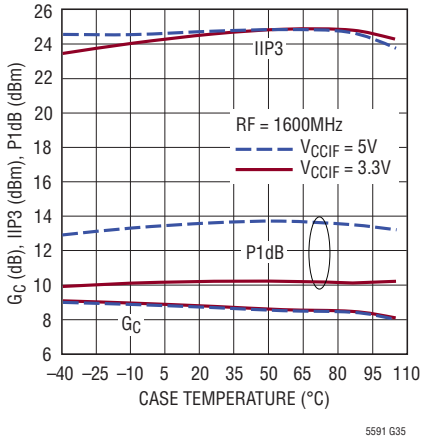
1750MHz Conversion Gain, IIP3 and NF vs LO Power



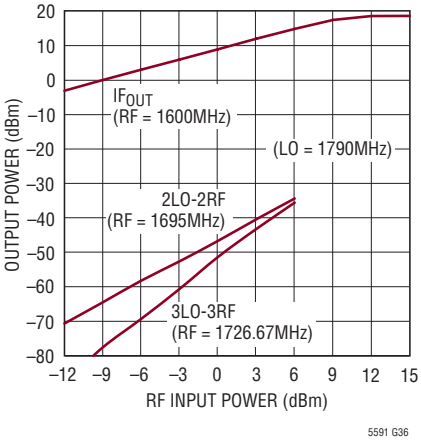
Conversion Gain, IIP3 and NF vs Supply Voltage (Single Supply)



Conversion Gain, IIP3 and RF Input P1dB vs Temperature



Single-Tone IF Output Power, 2 × 2 and 3 × 3 Spurs vs RF Input Power

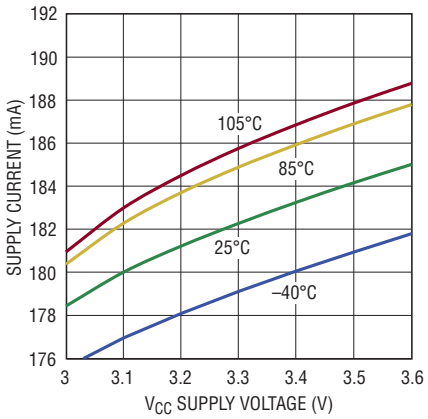


TYPICAL DC PERFORMANCE CHARACTERISTICS

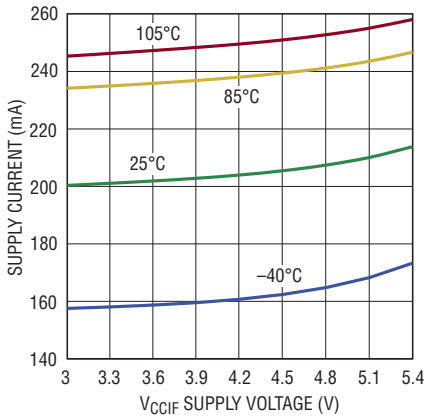
ENA = ENB = High, test circuit shown in Figure 1.

I_{SEL} = Low

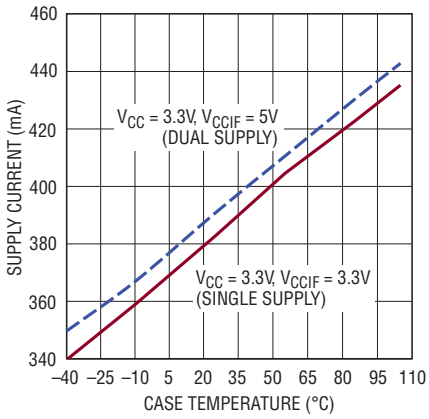
V_{CC} Supply Current vs Supply Voltage (Mixer and LO Amplifier)



V_{CCIF} Supply Current vs Supply Voltage (IF Amplifier)

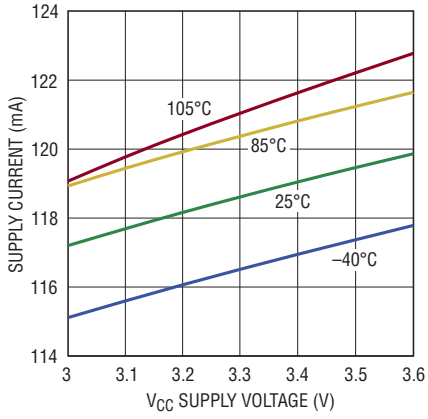


Total Supply Current vs Temperature (V_{CC} + V_{CCIF})

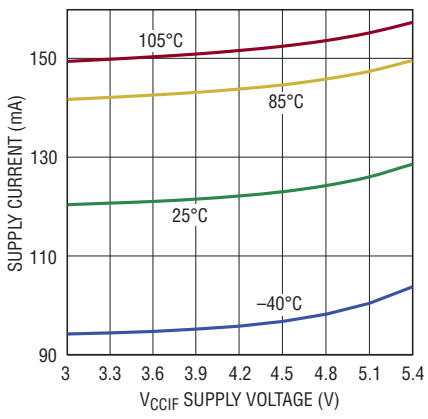


I_{SEL} = High

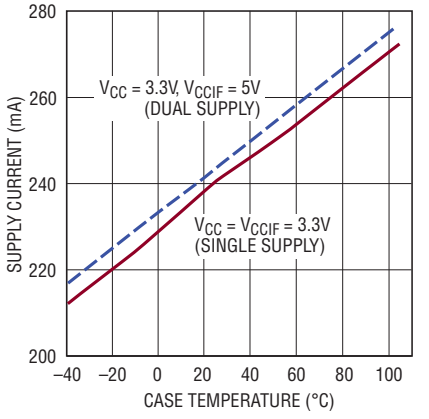
V_{CC} Supply Current vs Supply Voltage (Mixer and LO Amplifier)



V_{CCIF} Supply Current vs Supply Voltage (IF Amplifier)



Total Supply Current vs Temperature (V_{CC} + V_{CCIF})



PIN FUNCTIONS

RFA, RFB (Pins 1, 6): Single-Ended RF Inputs for Channels A and B. These pins are internally connected to the primary sides of the RF input transformers, which have low DC resistance to ground. **Series DC-blocking capacitors should be used to avoid damage to the integrated transformer when DC voltage is present at the RF inputs.** The RF inputs are impedance matched when the LO input is driven with a 0±6dBm source between 1.4GHz and 2.1GHz and the channels are enabled.

CTA, CTB (Pins 2, 5): RF Transformer Secondary Center-Tap on Channels A and B. These pins may require bypass capacitors to ground to optimize IIP3 performance. Each pin has an internally generated bias voltage of 1.2V and must be DC-isolated from ground and V_{CC}.

GND (Pins 3, 4, 7, 13, 15, 24, Exposed Pad Pin 25): Ground. These pins must be soldered to the RF ground plane on the circuit board. The exposed pad metal of the package provides both electrical contact to ground and good thermal contact to the printed circuit board.

IFGNDB, IFGNDA (Pins 8, 23): DC Ground Returns for the IF Amplifiers. These pins must be connected to ground to complete the DC current paths for the IF amplifiers. Chip inductors may be used to tune LO-IF and RF-IF leakage. Typical DC current is 100mA for each pin.

IFB^+, IFB^-, IFA^-, IFA^+ (Pins 9, 10, 21, 22): Open-Collector Differential Outputs for the IF Amplifiers of Channels B and A. These pins must be connected to a DC supply through impedance matching inductors, or transformer center-taps. Typical DC current consumption is 50mA into each pin.

IFBB, IFBA (Pins 11, 20): Bias Adjust Pins for the IF Amplifiers. These pins allow independent adjustment of the internal IF buffer currents for channels B and A, respectively. The typical DC voltage on these pins is 2.2V. If not used, these pins must be DC isolated from ground and V_{CC}.

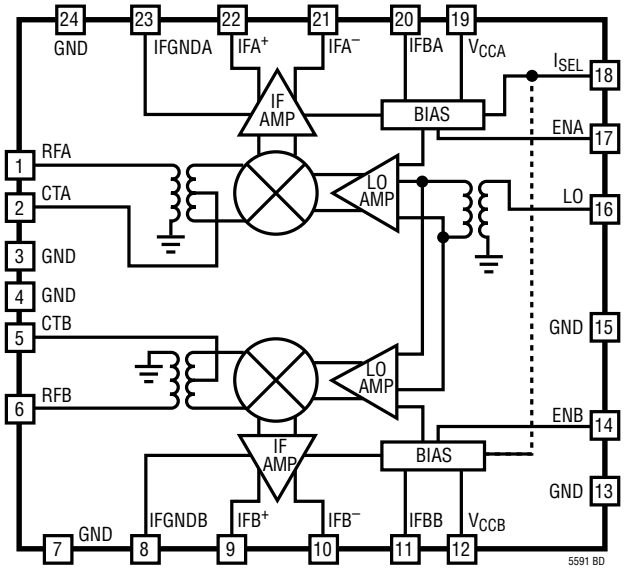
V_{CCB} and V_{CCA} (Pins 12, 19): Power Supply Pins for the LO Buffers and Bias Circuits. These pins must be connected to a regulated 3.3V supply with bypass capacitors located close to the pins. Typical current consumption is 91mA per pin.

ENB, ENA (Pins 14, 17): Enable Pins. These pins allow Channels B and A, respectively, to be independently enabled. An applied voltage of greater than 2.5V activates the associated channel while a voltage of less than 0.3V disables the channel. Typical input current is less than 10µA. These pins must not be allowed to float.

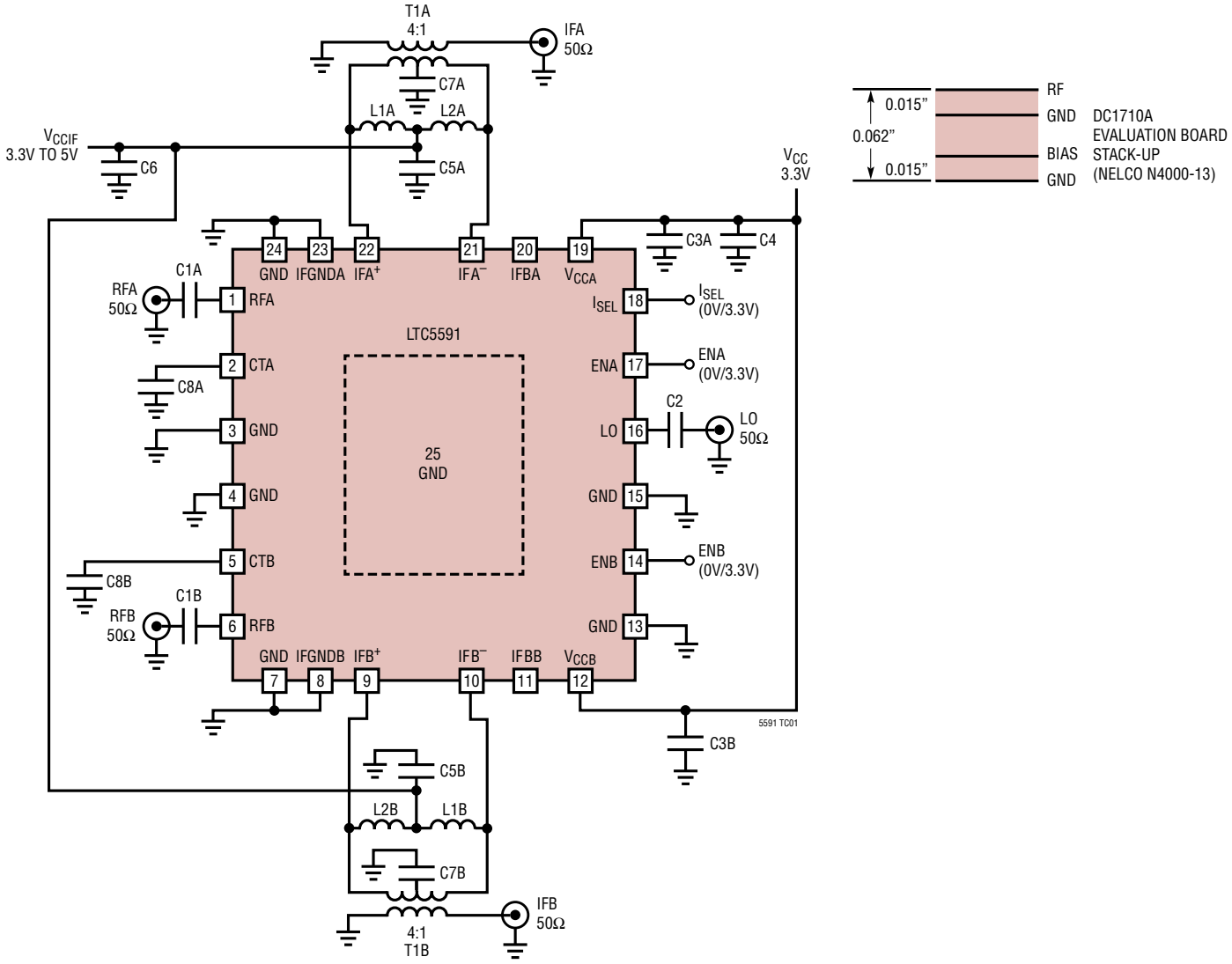
LO (Pin 16): Single-Ended Local Oscillator Input. This pin is internally connected to the primary side of the LO input transformer and has a low DC resistance to ground. **Series DC-blocking capacitors should be used to avoid damage to the integrated transformer when DC voltage is present at the LO input.** The LO input is internally matched to 50Ω for all states of ENA and ENB.

I_{SEL} (Pin 18): Low Current Select Pin. When this pin is pulled low (<0.3V), both mixer channels are biased at the normal current level for best RF performance. When greater than 2.5V is applied, both channels operate at reduced current, which provides reasonable performance at lower power consumption. This pin must not be allowed to float.

BLOCK DIAGRAM



TEST CIRCUIT



L1, L2 vs IF FREQUENCIES	
IF (MHz)	L1, L2 (nH)
140	270
190	150
240	100
300	56
380	33

REF DES	VALUE	SIZE	VENDOR
C1A, C1B, C8A, C8B	2.7pF	0402	AVX
C2	4.7pF	0402	AVX
C3A, C3B C5A, C5B	22pF	0402	AVX
C4, C6	1µF	0603	AVX
C7A, C7B	1000pF	0402	AVX
L1, L2	150nH	0603	Coilcraft
T1A, T1B	TC1-1W-7ALN+		Mini-Circuits

Figure 1. Standard Test Circuit Schematic (190MHz IF)

APPLICATIONS INFORMATION

Introduction

The LTC5591 consists of two identical mixer channels driven by a common LO input signal. Each high linearity mixer consists of a passive double-balanced mixer core, IF buffer amplifier, LO buffer amplifier and bias/enable circuits. See the Pin Functions and Block Diagram sections for a description of each pin. Each of the mixers can be shutdown independently to reduce power consumption and low current mode can be selected that allows a trade-off between performance and power consumption. The RF and LO inputs are single-ended and are internally matched to 50Ω. Low side or high side LO injection can be used. The IF outputs are differential. The evaluation circuit, shown in Figure 1, utilizes bandpass IF output matching and an IF transformer to realize a 50Ω single-ended IF output. The evaluation board layout is shown in Figure 2.

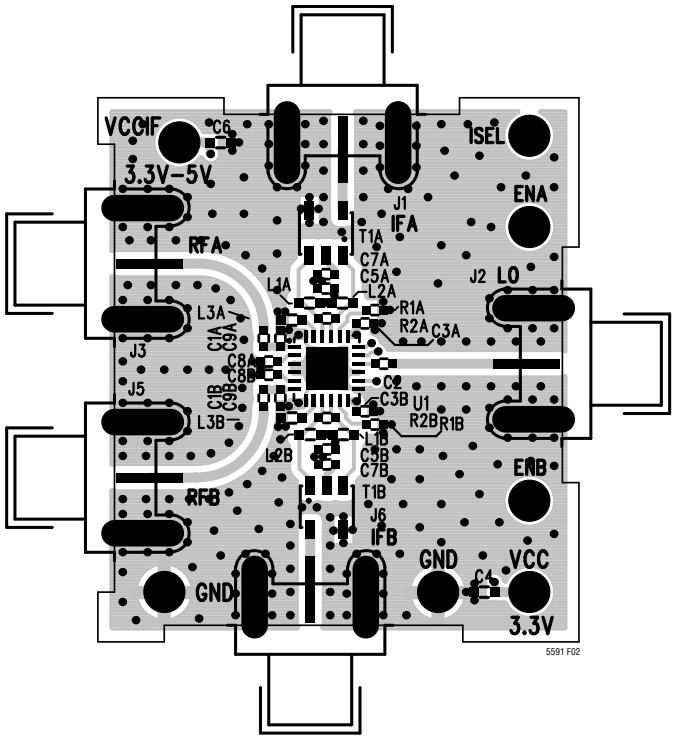


Figure 2. Evaluation Board Layout

RF Inputs

The RF inputs of channels A and B are identical. The RF input of channel A, shown in Figure 3, is connected to the primary winding of an integrated transformer. A 50Ω match is realized when a series external capacitor, C1A, is connected to the RF input. C1A is also needed for DC blocking if the source has DC voltage present, since the primary side of the RF transformer is internally DC-grounded. The DC resistance of the primary is approximately 3.6Ω.

The secondary winding of the RF transformer is internally connected to the channel A passive mixer core. The center-tap of the transformer secondary is connected to Pin 2 (CTA) to allow the connection of bypass capacitor, C8A. The value of C8A can be adjusted to improve the channel-to-channel isolation at specific RF operation frequency with minor impact to conversion gain, linearity and noise performance. The channel-to-channel isolation performance with different values of C8A is given in Figure 4. When used, it should be located within 2mm of Pin 2 for proper high frequency decoupling. The nominal DC voltage on the CTA pin is 1.2V.

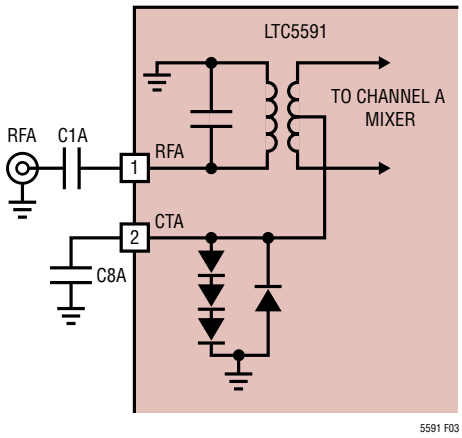


Figure 3. Channel A RF Input Schematic

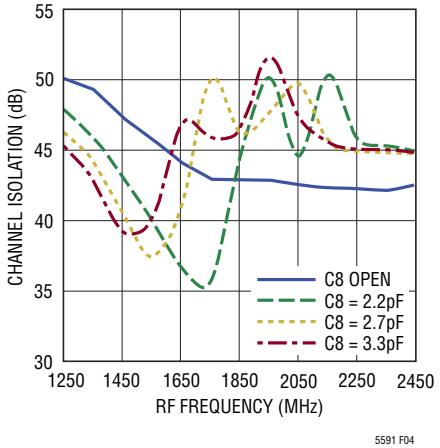


Figure 4. Channel-to-Channel Isolation vs C8 Values

APPLICATIONS INFORMATION

For the RF inputs to be properly matched, the appropriate LO signal must be applied to the LO input. A broadband input match is realized with C1A = 2.2pF. The measured input return loss is shown in Figure 4 for LO frequencies of 1.4GHz, 1.75GHz and 2GHz. These LO frequencies correspond to lower, middle and upper values in the LO range. As shown in Figure 5, the RF input impedance is dependent on LO frequency, although a single value of C1A is adequate to cover the 1.3GHz to 2.3GHz RF band.

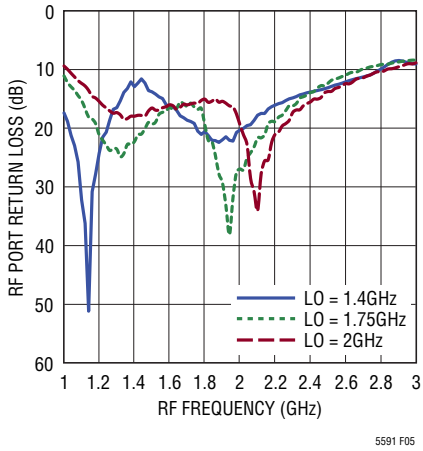


Figure 5. RF Port Return Loss

The RF input impedance and input reflection coefficient, versus RF frequency, are listed in Table 1. The reference plane for this data is pin 1 of the IC, with no external matching, and the LO is driven at 1.75GHz.

Table 1. RF Input Impedance and S11 (at Pin 1, No External Matching, f_{LO} = 1.75GHz)

FREQUENCY (GHz)	RF INPUT IMPEDANCE	S11	
		MAG	ANGLE
1.0	25.3 + j34.6	0.51	100.8
1.2	33.7 + j38.7	0.46	88.1
1.4	43.8 + j38.6	0.39	76.8
1.6	56.0 + j33.5	0.31	62.3
1.8	48.1 + j9.1	0.09	96.4
2.0	38.5 + j21.4	0.27	104.6
2.2	40.1 + j28.3	0.32	91.8
2.4	44.0 + j34.7	0.35	79.6
2.6	52.1 + j40.7	0.37	65.3
2.8	64.1 + j44.1	0.38	51.2
3.0	78.8 + j42.0	0.38	37.5

LO Input

The LO input, shown in Figure 6, is connected to the primary winding of an integrated transformer. A 50Ω impedance match is realized at the LO port by adding an external series capacitor, C2. This capacitor is also needed for DC blocking if the LO source has DC voltage present, since the primary side of the LO transformer is DC-grounded internally. The DC resistance of the primary is approximately 4.1Ω.

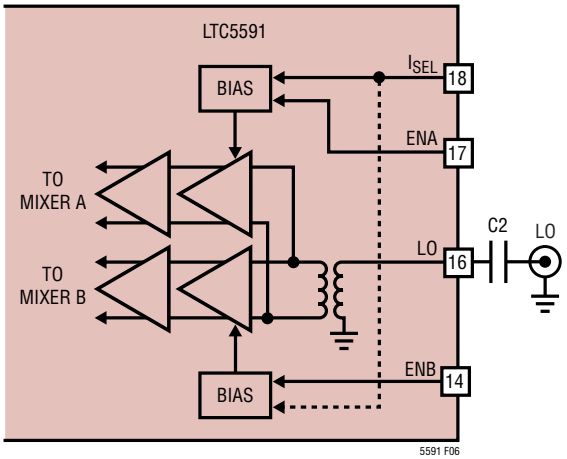


Figure 6. LO Input Schematic

The secondary of the transformer drives a pair of high speed limiting differential amplifiers for channels A and B. The LTC5591's LO amplifiers are optimized for the 1.4GHz to 2.1GHz LO frequency range; however, LO frequencies outside this frequency range may be used with degraded performance.

The LO port is always 50Ω matched when V_{CC} is applied, even when one or both of the channels is disabled. This helps to reduce frequency pulling of the LO source when

APPLICATIONS INFORMATION

the mixer is switched between different operating states. Figure 7 illustrates the LO port return loss for the different operating modes.

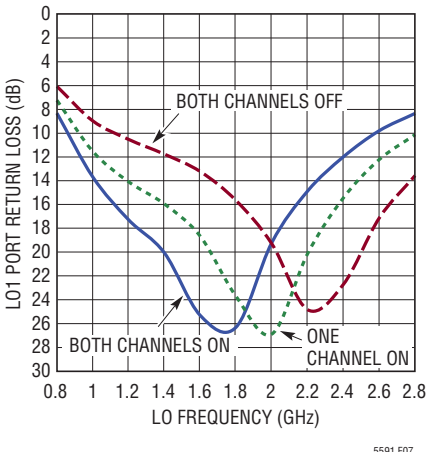


Figure 7. LO Input Return Loss

The nominal LO input level is 0dBm, though the limiting amplifiers will deliver excellent performance over a ±6dBm input power range. Table 2 lists the LO input impedance and input reflection coefficient versus frequency.

Table 2. LO Input Impedance vs Frequency (at Pin 16, No External Matching, ENA = ENB = High)

FREQUENCY (GHz)	INPUT IMPEDANCE	S11	
		MAG	ANGLE
1.0	39.4 + j46.4	0.47	75.5
1.2	55.3 + j40.8	0.36	61.4
1.4	61.9 + j26.8	0.25	52.6
1.6	56.5 + j16.1	0.16	59.5
1.8	47.6 + j14.0	0.14	91.6
2.0	41.6 + j18.0	0.21	103.9
2.2	38.4 + j23.5	0.29	101.5
2.4	37.1 + j30.7	0.36	93.3
2.6	38.4 + j38.3	0.42	83.3
2.8	42.0 + j47.6	0.47	72.2
3.0	48.6 + j56.1	0.49	61.8

IF Outputs

The IF amplifiers in channels A and B are identical. The IF amplifier for channel A, shown in Figure 8, has differential open collector outputs (IFA^+ and IFA^-), a DC ground return pin (IFGNDA), and a pin for adjusting the internal bias (IFBA). The IF outputs must be biased at the supply voltage (V_{CCIFA}), which is applied through matching inductors L1A and L2A. Alternatively, the IF outputs can be biased through the center tap of a transformer (T1A). The common node of L1A and L2A can be connected to the center tap of the transformer. Each IF output pin draws approximately 50mA of DC supply current (100mA total). An external load resistor, R2A, can be used to improve impedance matching if desired.

IFGNDA (Pin 23) must be grounded or the amplifier will not draw DC current. Inductor L3A may improve LO-IF and RF-IF leakage performance in some applications, but is otherwise not necessary. Inductors should have small resistance for DC. High DC resistance in L3A will reduce the IF amplifier supply current, which will degrade RF performance.

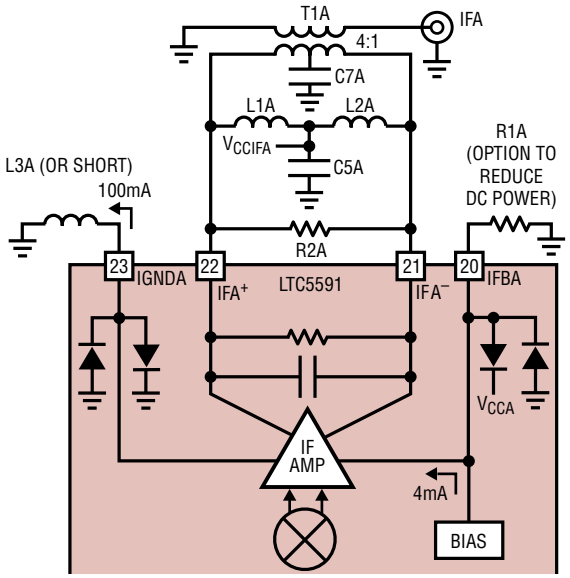


Figure 8. IF Amplifier Schematic with Bandpass Match

For optimum single-ended performance, the differential IF output must be combined through an external IF transformer or a discrete IF balun circuit. The evaluation board (see Figures 1 and 2) uses a 4:1 IF transformer for impedance transformation and differential to single-ended conversion. It is also possible to eliminate the IF transformer and drive differential filters or amplifiers directly.

APPLICATIONS INFORMATION

At IF frequencies, the IF output impedance can be modeled as 300Ω in parallel with 2.3pF. The equivalent small-signal model, including bondwire inductance, is shown in Figure 9. Frequency-dependent differential IF output impedance is listed in Table 3. This data is referenced to the package pins (with no external components) and includes the effects of IC and package parasitics.

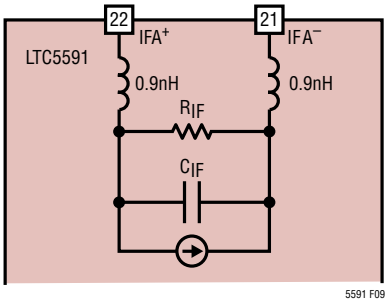


Figure 9. IF Output Small-Signal Model

Bandpass IF Matching

The bandpass IF matching configuration, shown in Figures 1 and 8, is best suited for IF frequencies in the 90MHz to 500MHz range. Resistor R2A may be used to reduce the IF output resistance for greater bandwidth and inductors L1A and L2A resonate with the internal IF output capacitance at the desired IF frequency. The value of L1A, L2A can be estimated as follows:

$$L1A = L2A = \frac{1}{\left[\left(2\pi f_{IF}\right)^2 \bullet 2 \bullet C_{IF}\right]}$$

where C_{IF} is the internal IF capacitance (listed in Table 3).

Table 3. IF Output Impedance vs Frequency

FREQUENCY (MHz)	DIFFERENTIAL OUTPUT IMPEDANCE (R_{IF} || X_{IF} (C_{IF}))
90	321 || –j769 (2.3pF)
140	307 || –j494 (2.3pF)
190	300 || –j364 (2.3pF)
240	292 || –j286 (2.3pF)
300	285 || –j225 (2.4pF)
380	276 || –j177 (2.4pF)
500	264 || –j122 (2.6pF)

Values of L1A and L2A are tabulated in Figure 1 for various IF frequencies. The measured IF output return loss for bandpass IF matching is plotted in Figure 10.

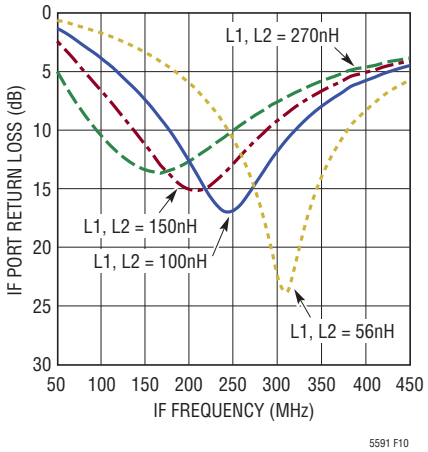


Figure 10. IF Output Return Loss with Bandpass Matching

Lowpass IF Matching

For IF frequencies below 90MHz, the inductance values become unreasonably high and the lowpass topology shown in Figure 11 is preferred. This topology also can provide improved RF to IF and LO to IF isolation. V_{CCIFA} is supplied through the center tap of the 4:1 transformer. A lowpass impedance transformation is realized by shunt elements R2A and C9A (in parallel with the internal RIF and CIF), and series inductors L1A and L2A. Resistor R2A is used to reduce the IF output resistance for greater bandwidth, or it can be deleted for the highest conversion gain. The final impedance transformation to 50Ω is realized by transformer T1A. The measured IF output return loss for

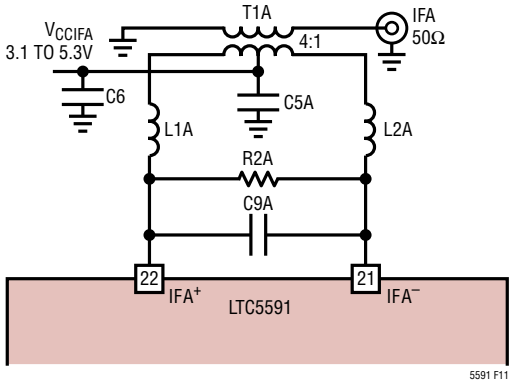


Figure 11. IF Output with Lowpass Matching

APPLICATIONS INFORMATION

lowpass IF matching with R2A and C9A open is plotted in Figure 12. The LTC5591 demo board (see Figure 2) has been laid out to accommodate this matching topology with only minor modifications.

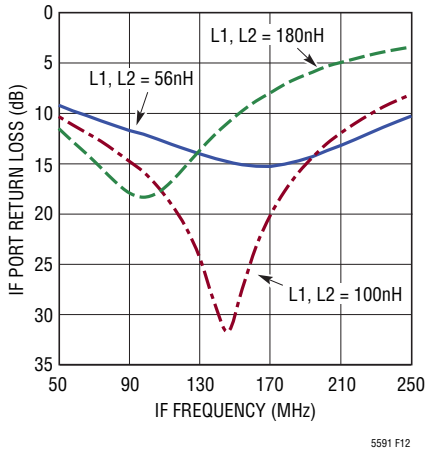


Figure 12. IF Output Return Loss with Lowpass Matching

IF Amplifier Bias

The IF amplifier delivers excellent performance with V_{CCIF} = 3.3V, which allows a single supply to be used for V_{CC} and V_{CCIF}. At V_{CCIF} = 3.3V, the RF input P1dB of the mixer is limited by the output voltage swing. For higher P1dB, in this case, resistor R2A (Figure 7) can be used to reduce the output impedance and thus the voltage swing, thus improving P1dB. The trade-off for improved P1dB will be lower conversion gain.

With V_{CCIF} increased to 5V the P1dB increases by over 3dB, at the expense of higher power consumption. Mixer P1dB performance at 1950MHz is tabulated in Table 4 for V_{CCIF} values of 3.3V and 5V. For the highest conversion gain, high-Q wire-wound chip inductors are recommended for L1A and L2A, especially when using V_{CCIF} = 3.3V. Low cost multilayer chip inductors may be substituted, with a slight reduction in conversion gain.

Table 4. Performance Comparison with V_{CCIF} = 3.3V and 5V (RF = 1950MHz, Low Side LO, IF = 190MHz, ENA = ENB = High)

V_{CCIF} (V)	R2A (Ω)	I_{CCIF} (mA)	G_C (dB)	P1dB (dBm)	IIP3 (dBm)	NF (dB)
3.3	Open	200	8.5	10.7	26.2	9.9
	1k	200	7.4	11.5	26.5	9.9
5	Open	207	8.4	13.9	26.7	10.1

The IFBA pin (Pin 20) is available for reducing the DC current consumption of the IF amplifier, at the expense of IIP3. The nominal DC voltage at Pin 20 is 2.1V, and this pin should be left open-circuited for optimum performance. The internal bias circuit produces a 4mA reference for the IF amplifier, which causes the amplifier to draw approximately 100mA. If resistor R1A is connected to Pin 20 as shown in Figure 8, a portion of the reference current can be shunted to ground, resulting in reduced IF amplifier current. For example, R1A = 470Ω will shunt away 1.4mA from Pin 20 and the IF amplifier current will be reduced by 35% to approximately 65mA. Table 5 summarizes RF performance versus total IF amplifier current when both channels are enabled.

Table 5. Mixer Performance with Reduced IF Amplifier Current

RF = 1950MHz, Low Side LO, IF = 190MHz, V_{CC} = V_{CCIF} = 3.3V

R1A, R1B	I_{CCIF} (mA)	G_C (dB)	IIP3 (dBm)	P1dB (dBm)	NF (dB)
Open	200	8.5	26.2	10.7	9.9
3.3kΩ	176	8.4	25.7	10.8	9.9
1.0kΩ	151	8.1	24.7	10.9	9.9
470Ω	130	7.9	23.7	10.9	9.9

RF = 1600MHz, High Side LO, IF = 190MHz, V_{CC} = V_{CCIF} = 3.3V

R1A, R1B	I_{CCIF} (mA)	G_C (dB)	IIP3 (dBm)	P1dB (dBm)	NF (dB)
Open	200	8.6	24.6	10.2	10.2
3.3kΩ	176	8.4	24.3	10.4	10.3
1.0kΩ	151	8.1	23.5	10.6	10.3
470Ω	130	7.9	22.7	10.5	10.3

APPLICATIONS INFORMATION

Low Current Mode

Both mixer channels can be set to low current mode using the I_{SEL} pin. This allows flexibility to choose a reduced current mode of operation when lower RF performance is acceptable. Figure 13 shows a simplified schematic of the I_{SEL} pin interface. When I_{SEL} is set low (<0.3V), both channels operate at nominal DC current. When I_{SEL} is set high (>2.5V), the DC currents in both channels are reduced, thus reducing power consumption. The performance in low power mode and normal power mode are compared in Table 6.

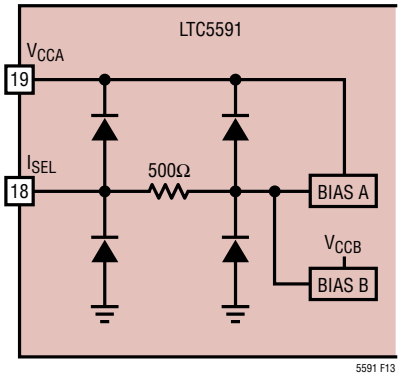


Figure 13. I_{SEL} Interface Schematic

Table 6. Performance Comparison Between Different Power Modes RF = 1950MHz, Low Side LO, IF = 190MHz, ENA = ENB = High

I_{SEL}	I_{TOTAL} (mA)	G_C (dB)	IIP3 (dBm)	P1dB (dBm)	NF (dB)
Low	382	8.5	26.2	10.7	9.9
High	239	7.2	21.4	10.7	10.3

Enable Interface

Figure 14 shows a simplified schematic of the ENA pin interface (ENB is identical). To enable channel A, the ENA voltage must be greater than 2.5V. If the enable function is not required, the enable pin can be connected directly to V_{CC}. The voltage at the enable pin should never exceed the power supply voltage (V_{CC}) by more than 0.3V. If this should occur, the supply current could be sourced through the ESD diode, potentially damaging the IC.

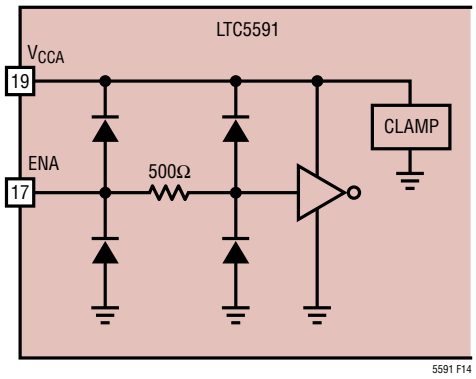


Figure 14. ENA Interface Schematic

The Enable pins must be pulled high or low. If left floating, the on/off state of the IC will be indeterminate. If a three-state condition can exist at the enable pins, then a pull-up or pull-down resistor must be used.

Supply Voltage Ramping

Fast ramping of the supply voltage can cause a current glitch in the internal ESD protection circuits. Depending on the supply inductance, this could result in a supply voltage transient that exceeds the maximum rating. A supply voltage ramp time of greater than 1ms is recommended.

Spurious Output Levels

Mixer spurious output levels versus harmonics of the RF and LO are tabulated in Table 7. The spur levels were measured on a standard evalution board using the test circuit shown in Figure 1. The spur frequencies can be calculated using the following equation:

$$f_{SPUR} = (M \bullet f_{RF}) - (N \bullet f_{LO})$$

Table 7. IF Output Spur Levels (dBc)

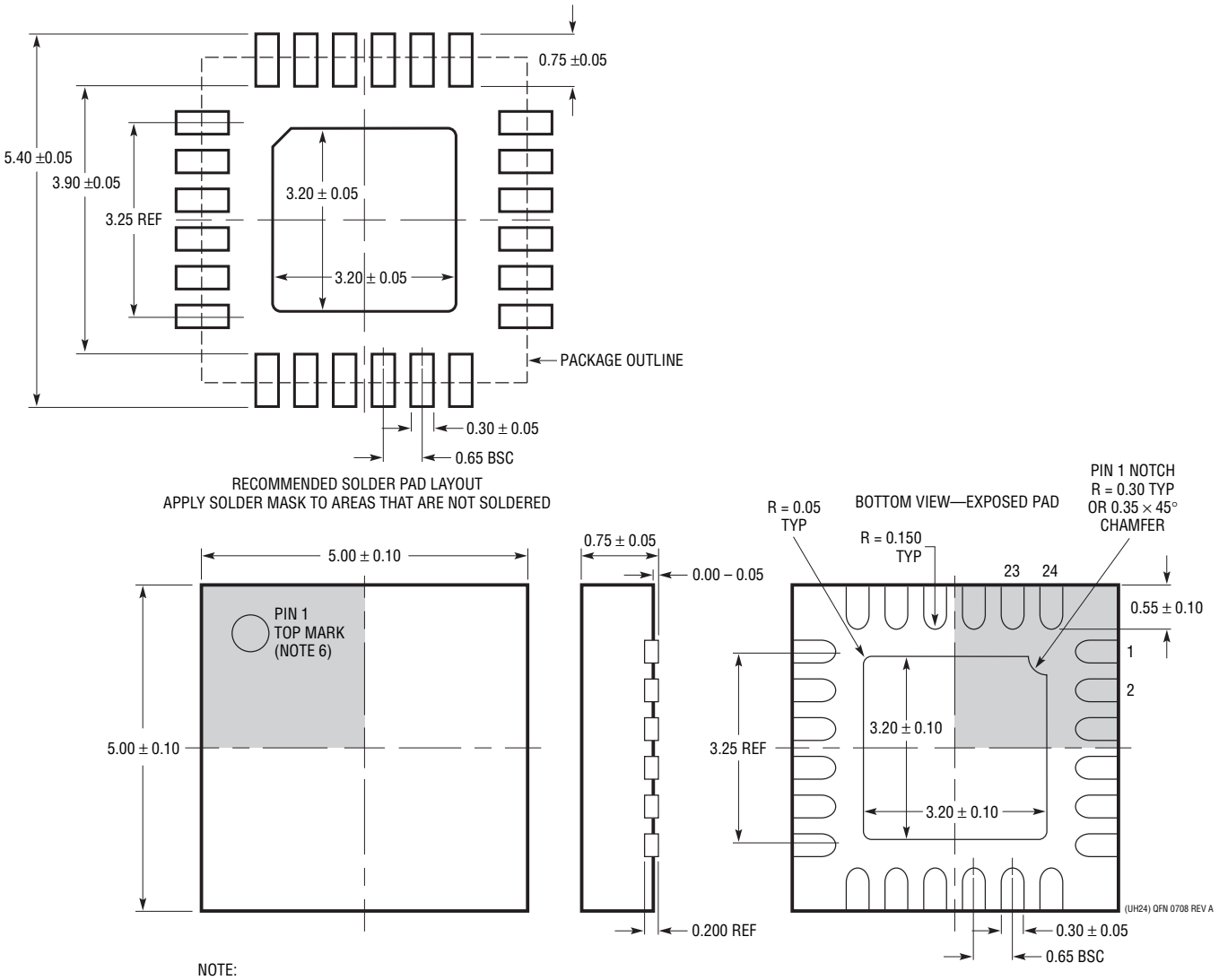
RF = 1950MHz, P_{RF} = –3dBm, P_{LO} = 0dBm, P_{IF} 190MHz, Low Side LO, V_{CC} = 3.3V, V_{CCIF} = 3.3V, ENA = ENB = High, I_{SEL} = Low, T_C = 25°C

		N									
		0	1	2	3	4	5	6	7	8	9
M	0		–41	–54	–64	–84	–66	–74	–75	–81	–84
	1	–49	0	–56	–42	–68	–77	–75	–70	*	–92
	2	–82	–83	–70	–77	*	*	*	*	*	*
	3	*	–88	*	–71	*	*	*	*	*	*
	4	*	*	*	*	*	*	*	*	*	*
	5	*	*	*	*	*	*	*	*	*	*
	6		*	*	*	*	*	*	*	*	*
	7			*	*	*	*	*	*	–84	*

*Less than –100dBc

PACKAGE DESCRIPTION

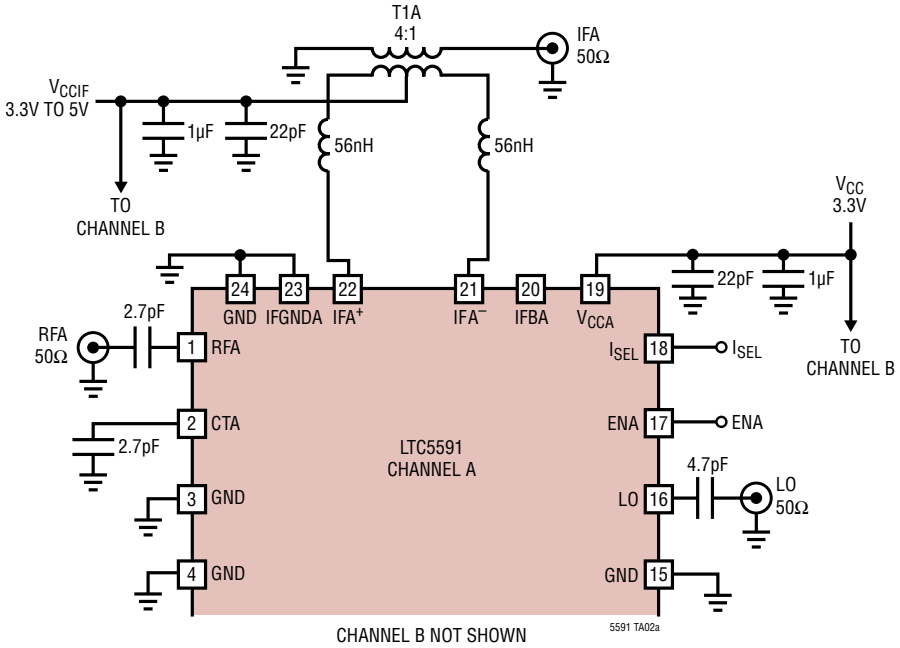
UH Package
24-Lead Plastic QFN (5mm × 5mm)
(Reference LTC DWG # 05-08-1747 Rev A)



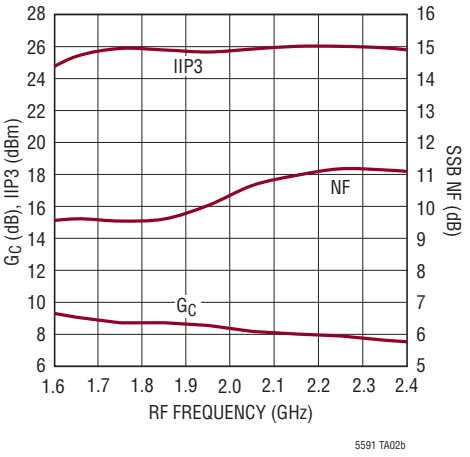
NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

Lowpass IF Matching, Low Side LO, V_{CC} = 3.3V, V_{CCIF} = 3.3V, ENA = ENB = High, I_{SEL} = Low, T_C = 25°C, P_{LO} = 0dBm, P_{RF} = –3dBm (–3dBm/Tone for Two-Tone IIP3 Tests, Δf = 2MHz), IF = 190MHz



Conversion Gain, IIP3 and SSB NF vs RF Frequency



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Infrastructure		
LT5527	400MHz to 3.7GHz, 5V Downconverting Mixer	2.3dB Gain, 23.5dBm IIP3 and 12.5dB NF at 1900MHz, 5V/78mA Supply
LT5557	400MHz to 3.8GHz, 3.3V Downconverting Mixer	2.9dB Gain, 24.7dBm IIP3 and 11.7dB NF at 1950MHz, 3.3V/82mA Supply
LTC6416	2GHz 16-Bit ADC Buffer	40.25dBm OIP3 to 300MHz, Programmable Fast Recovery Output Clamping
LTC6412	31dB Linear Analog VGA	35dBm OIP3 at 240MHz, Continuous Gain Range –14dB to 17dB
LTC5540/LTC5541/ LTC5542/LTC5543	600MHz to 4GHz Downconverting Mixer Family	8dB Gain, >25dBm IIP3, 10dB NF, 3.3V/200mA Supply
LT5554	Ultralow Distort IF Digital VGA	48dBm OIP3 at 200MHz, 2dB to 18dB Gain Range, 0.125dB Gain Steps
LT5578	400MHz to 2.7GHz Upconverting Mixer	27dBm OIP3 at 900MHz, 24.2dBm at 1.95GHz, Integrated RF Transformer
LT5579	1.5GHz to 3.8GHz Upconverting Mixer	27.3dBm OIP3 at 2.14GHz, NF = 9.9dB, 3.3V Supply, Single-Ended LO and RF Ports
RF Power Detectors		
LT5534	50MHz to 3GHz Log RF Power Detector with 60dB Dynamic Range	±1dB Output Variation over Temperature, 38ns Response Time, Log Linear Response
LT5581	6GHz Low Power RMS Detector	40dB Dynamic Range, ±1dB Accuracy Over Temperature, 1.5mA Supply Current
LTC5583	Dual 6GHz RMS Power Detector Measures VSWR	40MHz to 6GHz, Up to 60dB Dynamic Range, >40dB Channel-to-Channel Isolation, Difference Output for VSWR Measurement
ADCs		
LTC2285	14-Bit, 125Msps Dual ADC	72.4dB SNR, >88dB SFDR, 790mW Power Consumption
LTC2185	16-Bit, 125Msps Dual ADC Ultralow Power	76.8dB SNR, 185mW/Channel Power Consumption
LTC2242-12	12-Bit, 250Msps ADC	65.4dB SNR, 78dB SFDR, 740mW Power Consumption

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