



Soldering Considerations for Exposed-Pad Packages

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Introduction

This Engineer-to-Engineer Note is comprised of two main sections. The first section discusses general soldering guidelines for Analog Devices Inc. (ADI) DSP and processor boards, while the second section discusses specifically some commonly asked questions regarding Exposed pad (or EPAD) packages, requiring special considerations for soldering onto Printed Circuit Boards (PCBs). Special attention needs to be paid in order to ensure that electrical and thermal requirements are satisfied. This will ensure optimum performance of the device.

Determining the Temperature Profile for Boards

The process of determining the temperature profile for soldering components onto a custom board is determined by several factors, such as thickness and form factor of the board, the number and type of components, as well as the type of solder paste that is used (aero/mil or commercial/industrial). Solder paste vendors typically provide a reference document containing useful information, such as the recommended temperature profile for their paste. Based on this recommended profile for the type of solder paste used, it is advisable to populate a bare custom board with sufficient number of thermocouples, then pass it through the oven, and ensure that the appropriate temperature zones and times are reached.

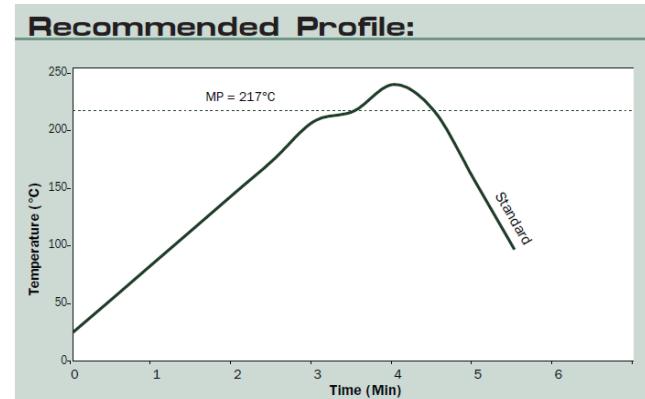


Figure 1 Recommended Heating Profile from Solder Paste vendor

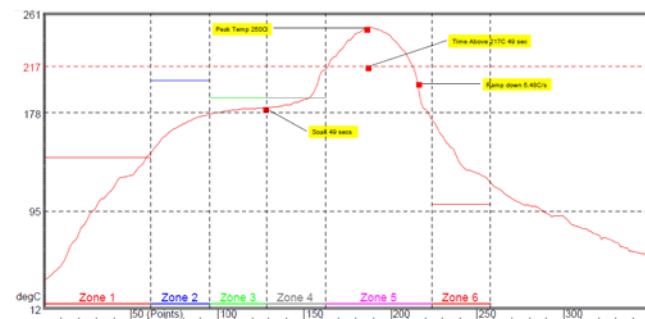


Figure 2 Heating Profile for typical ADI EZ-Kits

As a reference, Figure 1 and Figure 2 show the recommended temperature profile from the solder paste vendor, and the temperature profile followed in the oven for our EZ-KIT® boards.

The attachment accompanying this EE-Note contains the datasheet from the solder paste vendor, as well as the temperature profile information used for most Analog Devices, Inc. EZ-KIT boards.

It is important to note that this document is provided strictly as a reference, and a standard temperature profile may not work for boards that are very thick, and/or if multiple power planes are used and the board increases in density and thickness, or conversely, if the board is very light in density.

Component types can also require the profile to be changed, as in the case of large metal BGA's with incorporated heat sinks. It is important for customers with different components on their boards to require a different profile. How the raw boards are specified, and how they are populated will need to be taken into consideration. The information provided for the EZ-KIT boards can be used as a starting point, but it will likely need to be modified for the end user in some fashion.

While this EE-Note focuses on an example of a DSP with such an EPAD (namely, the 100-lead ADSP-21489 SHARC processor) for illustration purposes, the concepts discussed throughout this document should also apply to other DSPs with an EPAD, such as the ADSP-BF592 and the ADSP-BF506F EZ-KIT boards.

Commonly Asked Questions & Answers for Soldering EPAD Packages

Q1. Is there a generic temperature profile that can be used?

The temperature profile is unique to the part, the board, as well as the characteristics of solder paste used. For this reason, the temperature profile that would work for the ADSP-21489 100-pin LQFP-EP device will not necessarily work for a custom board with different characteristics.

Q2. There are twenty-five 0.012" via holes under the heat-sink area of the ADSP-21489 processor in the EZ-KIT reference design. Is

this really needed? And what if the custom board also contains via holes in its layout, but they are limited to the outside perimeter?

The optimum number of vias is determined by the amount of heat that needs to be dissipated into the ground plane. Typically, only one is needed for electrical connection.

This needs to be evaluated by the end user of the device to determine heat dissipation requirements. It is also important to note that the more vias used, the more solder will migrate into them starving the pad area for a good connection. Therefore, there is a trade-off to be kept in mind when deciding the number of vias.

One possibility is to increase the size of the pad on the board by 0.040" in X & Y, but maintain the solder mask at the size of the tab on the device. This will provide a frame of 0.020" around the perimeter of the pad on the board.

The perimeter of the pad on the board can be loaded with vias, but also keep them under the solder mask. This design will prevent the solder from going into the vias, but still give a thermal connection to ground by way of the barrels in the vias. With this approach, it will not dissipate as much heat as filled vias, but more vias can be used without starving the solder connection.

Q3. What is the recommended paste thickness to be applied under the heat-sink area?

This is determined by the other PCB components. Too much thickness will cause bridging on fine pitch components, and solder sticking in very small apertures on the stencil. Solder paste will reflow into solder,

reducing its volume to half the volume of the paste deposit. Therefore, it will never be able to avoid voids on the ground connection.

Typically a solder connection of 50% or greater is acceptable. [Figure 3](#) shows x-ray images of the 100-lead ADSP-21489 package on the EZ-KIT board. The lighter areas correspond to the regions of solder void.

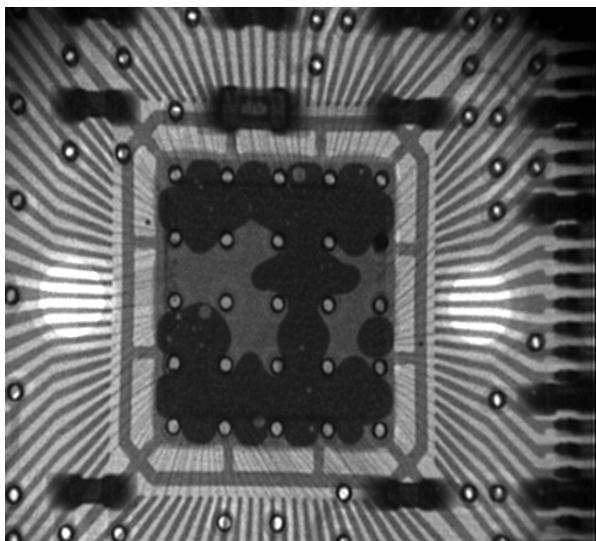
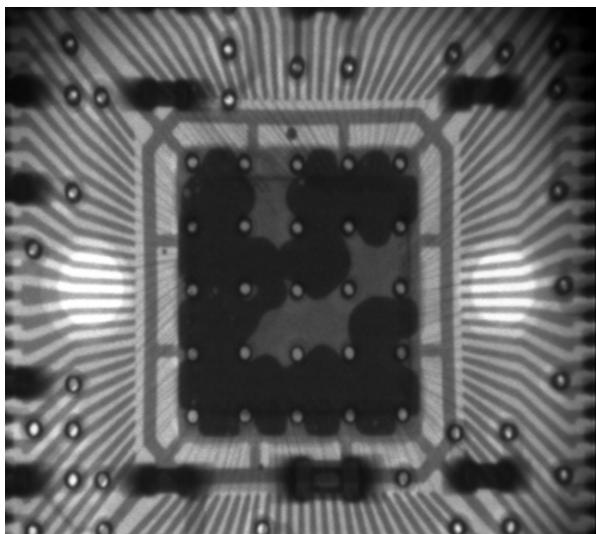


Figure 3. X-Ray Images of 100-lead ADSP-21489 package from two different EZ-KIT boards

Q4. Is there a specific stencil opening design that should be used?

The usual procedure for the EZ-KIT boards is to use 0.005" thick stencils with the aperture for the ground cut 1:1 for leaded devices, and about a 50% reduction for leadless devices (so the part does not float on the solder causing opens on the leadless connections). However, this is just a starting point; all stencil designs are very dependent on several unique characteristics of the overall design of the board.

Q5. Is there a temperature profile that customers can use?

Temperature profile is dependent on the thermal design of the board. The more you try to dissipate heat, and the denser the board is internally, the harder it will be to bring the pad temperature up to the proper point for good wetting. Too much heat will reduce the ability of the flux to do its job cleaning the surfaces and it will cause other defects. Again, keeping the heat dissipation requirement and board density to a minimum is the best approach.

Q6. What is the maximum percentage of area under the EPAD that could be solder voids? And are there any limits on the size of individual voids themselves?

In order to ensure a robust ground and thermal connection, the total void area must be less than 50% of the EPAD *AND* no more than 50% of the vias to the GND plane should be in a void. Additionally, the largest single void should not exceed 30% of the EPAD area.

That said, it is very difficult to quantify the impact of voids on the reliability of the EPAD connection without performing stress testing.

The appropriate PCB-level qualification stress tests (such as temperature-cycle) should be run on parts with known (Time-zero) voiding to confirm EPAD solder joint reliability.

Q7. Is there a concern of localized hot spots on the package where there might be a void under the EPAD?

No. As long as the limits specified under the previous answer are adhered to, the EPAD functions as a heat-spreader, and any localized rise in temperature is uniformly distributed across the entire EPAD, and subsequently dissipated at the contacts of the EPAD.

Q8. We are having a difficult time deciding on the amount of solder paste to apply. Increasing the amount of solder paste seems to reduce the area and number of solder voids, but also causes problems of “solder beading” or “solder balling” due to excessive solder paste. Can ADI help with providing tighter package bounds to alleviate this problem?

The answer is very dependent on the manufacturing equipment, temperature conditions, board design, stencil and solder paste, via wicking prevention strategy and material set, including PCB.

Typically, it is not possible to offer expert advice without full knowledge of all manufacturing and product design details. ADI recommends that customers work with

their PCB assembly house to conduct a DOA (Design of Experiments) procedure to optimize the manufacturing parameters specific to the assembly conditions and equipment.

Q9. We plan to model our future board design to incorporate the ADI recommendations of at least a 3x3 matrix of vias under the EPAD (not just 8 along the perimeters), and also change the number of panes accordingly, to at least 3x3 instead of the 2x2 that they have. In the interim, it would be great if ADI can provide some insight as to how a customer may alleviate some of the solder void issue on their current board by using the “Via packing” method.

ADI recommends a 5x5 array of vias to connect the PCB pad to the ground plane (at least, an additional 3x3 array added to the existing design). This is required in order to ensure a good thermal pathway and also to ensure a robust ground electrical connection. A uniform array of vias combined with a “via wicking” prevention strategy can also help reduce the formation of voids.

Via wicking prevention is intended to reduce the amount of solder that flows into the vias and also to prevent the formation of solder “balls” on the underside of the PCB. Typical via wicking prevention strategies include “via tenting”, “via filling” and “via encroachment”.

Solder voids in thermal pad regions are a known issue when mounting silicon on PCBs. When limited in size, these voids are not expected to degrade the electrical or thermal performance. Common techniques used to control the formation of these voids

are available. **Figure 4** shows four commonly used techniques used in the industry to address this issue.

The first technique is referred to as “via tenting from the top”. This approach uses dry film solder mask applied to the top of the PCB. In this technique, it is recommended that the solder mask diameter be 100 microns larger than the diameter of the via.

The second technique is referred to as “via tenting from the bottom”. This approach differs from the tenting from the top technique only in that the dry film solder mask is applied to the bottom of the PCB.

The third technique shown is “via plugging”. This is performed by partially filling the via with liquid photo-imageable (LPI) solder mask from the bottom side of the PCB.

Lastly, **Figure 4** shows the “encroached via” technique. This approach is achieved by application of solder mask to the bottom of the PCB around the vias.

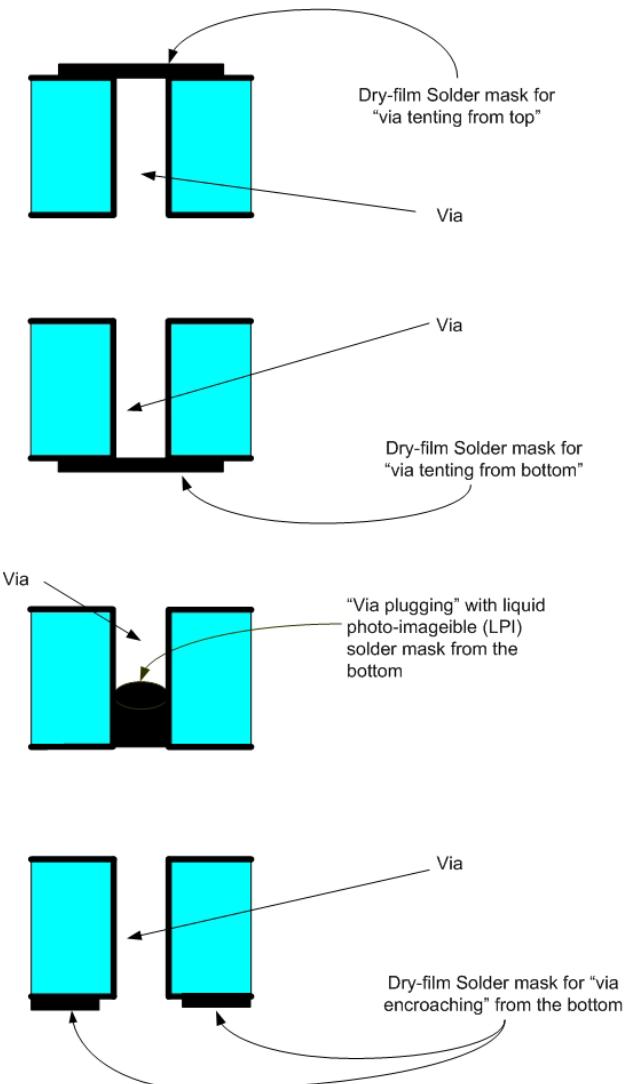


Figure 4 Via Wicking Prevention Strategies

References

- [1] *JESD No. 22-B102E Standard on Solderability*, JEDEC Solid State Technology Association, 2007.
- [2] *ADSP-21483/21487/21488/21489 SHARC Embedded Processor Data Sheet*. Rev A, April 2012. Analog Devices, Inc.
- [3] *ADSP-BF592 Blackfin Embedded Processor Data Sheet*. Rev A, August 2011. Analog Devices, Inc.

Document History

Revision	Description
<i>Rev 1 – May 17, 2012 by C. Patel and R. Chary</i>	Initial release.