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## Estimating Power for ADSP-BF534/BF536/BF537 Blackfin® Processors

Contributed by Joe B.

Rev. 3 – November 21, 2007

### Introduction

This EE-Note discusses the methodology for estimating total average power consumption of ADSP-BF534, ADSP-BF536, and ADSP-BF537 Blackfin® embedded processors. The ADSP-BF536 Blackfin processor is a low-power derivative of the ADSP-BF537 processor and is referred to as a “low-power processor” in this document. The ADSP-BF537 processors can run at faster internal clock speeds and are referred to as “high-performance processors” in this document. The ADSP-BF534 processor can be either low-power (400 MHz models) or high-performance (500 MHz models). The term *Blackfin* refers to all variations of processors addressed by this document.

Power estimates are based on characterization data measured over power supply voltage, core frequency ( $CCLK$ ), and junction temperature ( $T_j$ ). The intent of this document is to assist board designers in estimating their power budget for power supply design and thermal relief designs using Blackfin processors. These processors feature dynamic power management control, allowing the regulation of applied core voltage ( $V_{DDINT}$ ) from an external I/O source ( $V_{DDEXT}$ ). The ranges for these supplies differ depending on the part being used.

The total power consumption of the Blackfin processor is the sum of the power consumed for both of the power supply domains,  $V_{DDINT}$  and  $V_{DDEXT}$ .

Please consult the following sections of the *ADSP-BF534/ADSP-BF536/ADSP-BF537 Blackfin Embedded Processor Data Sheet*<sup>[1]</sup> for details specific to discussions throughout this EE-Note:

- See the *Recommended Operating Conditions* section for details regarding  $V_{DDINT}$  and  $V_{DDEXT}$  ranges.
- See the *Timing Specifications* section for details regarding required  $V_{DDINT}$  values to support the desired  $CCLK$ .
- See the *Ordering Guide* section for a comprehensive list of the various speed and temperature grade models available for ADSP-BF534, ADSP-BF536, and ADSP-BF537 Blackfin processors.

## Estimating Internal Power Consumption

The total power consumption due to internal circuitry (on the  $V_{DDINT}$  supply) is the sum of the static power component and dynamic power component of the processor's core logic. The dynamic portion of the internal power depends on the instruction execution sequence, the data operands involved, and the instruction rate. The static portion of the internal power is a function of temperature and voltage; it is not related to processor activity.

Analog Devices provides current consumption figures and scaling factors for discrete dynamic activity levels. System application code can be mapped to these discrete numbers to estimate the dynamic portion of the internal power consumption for Blackfin processors in a given application.

### Internal Power Vector Definitions

The following power vector definitions define the dynamic activity levels that apply to the internal power vectors shown in Table 1.

- $I_{DD-IDLE}$  -  $V_{DDINT}$  supply current for idle activity. Idle activity is the core executing the `IDLE` instruction only, with no core memory accesses, no DMA, and no interrupts.
- $I_{DD-NOP}$  -  $V_{DDINT}$  supply current for no-op activity. No-op activity is the core executing the `NOP` instruction only, with no core memory accesses, no DMA, and no interrupts. This is a useful measurement for software-implemented delay loops.
- $I_{DD-APP}$  -  $V_{DDINT}$  supply current for a specific application's activity. This activity is the core executing an application comprised of 30% dual-MAC instructions and 70% load-store and no-op instructions. All instructions and data are located in L1 SRAM, and peripherals are not enabled.
- $I_{DD-TYP}$  -  $V_{DDINT}$  supply current for typical activity. Typical activity is the core executing an application comprised of 75% dual-MAC instructions and 25% dual-ALU instructions. All instructions and data are located in L1 SRAM, and peripherals are not enabled. This is the test vector used for the dissipation numbers found in the data-sheet.
- $I_{DD-HIGH}$  -  $V_{DDINT}$  supply current for high activity. High activity is the core executing an application comprised entirely of dual-MAC instructions. All instructions and data are located in L1 SRAM, and peripherals are disabled.
- $I_{DD-PEAK}$  -  $V_{DDINT}$  supply current for peak activity. Peak activity is the core executing 100% dual-MAC instructions fetched from internal memory, with memory DMA moving a data pattern from L1 Data A memory to L1 Data B memory. The bit pattern toggles all bits in each access.



The test code used to measure  $I_{DD-PEAK}$  represents worst-case processor operation. This activity level is not sustainable under normal application conditions.

### Estimating $I_{DDINT}$ Dynamic Current, $I_{DD-DYN}$

There are two steps required to estimate dynamic power consumption due to internal circuitry (i.e., on the  $V_{DDINT}$  supply). The first step is to determine the dynamic baseline current, and the second step is to determine the percentage of activity for each discrete power vector with respect to the entire application.

*I<sub>DD</sub> Baseline Dynamic Current, I<sub>DD-BASELINE-DYN</sub>*

The graph for the Blackfin processors' baseline dynamic current ( $I_{DD-BASELINE-DYN}$ ) is shown in Figure 1. The  $I_{DD-BASELINE-DYN}$  value is derived using the  $I_{DD-TYP}$  dynamic activity level vs. core frequency. Each curve in the graph represents a baseline  $I_{DDINT}$  dynamic current for a specified power supply setting. Using the curve specific to the application,  $I_{DD-BASELINE-DYN}$  for the  $V_{DDINT}$  power supply domain can be estimated at the CCLK of the processor in the application. For example, with  $V_{DDINT}$  at 1.2 V and CCLK at 400 MHz, the corresponding  $I_{DD-BASELINE-DYN}$  for the  $V_{DDINT}$  power supply domain would be approximately 120 mA.

**ADSP-BF534/6/7**  
**I<sub>DD</sub> Dynamic Typical (I<sub>DD-BASELINE-DYN</sub>)**

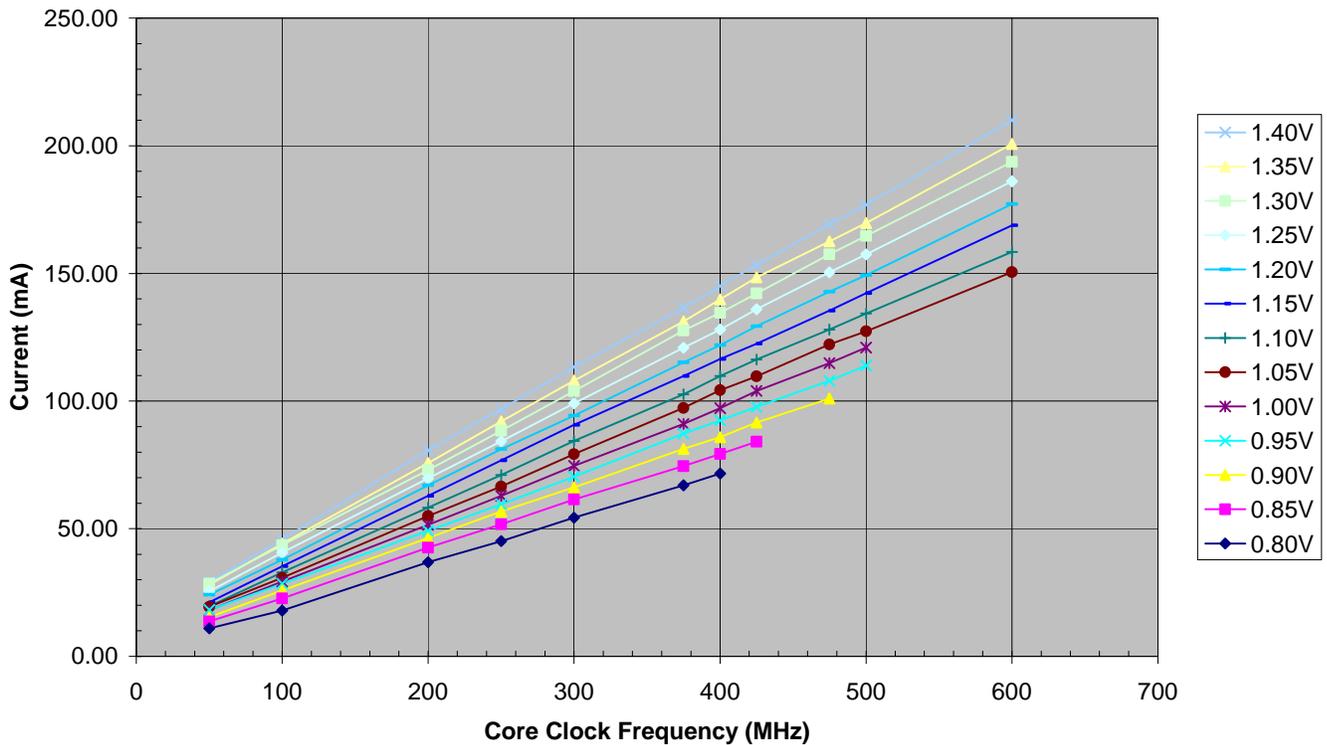


Figure 1. Baseline  $I_{DDINT}$  Dynamic Current

### *I<sub>DD</sub> Dynamic Current Running Your Application*

Table 1 lists the scaling factors for each activity level, which are used to estimate the dynamic current for each specific application. With knowledge of the program flow and an estimate of the percentage of time spent at each activity level, system developers can use  $I_{DD-BASELINE-DYN}$  values shown in Figure 1 and the corresponding activity scaling factors (ASF) from Table 1 to determine the dynamic portion of the internal current ( $I_{DD-DYN}$ ) for each Blackfin processor in a system.

Power Vector	Activity Scaling Factor (ASF)
$I_{DD-PEAK}$	1.33
$I_{DD-HIGH}$	1.29
$I_{DD-TYP}$	1.00
$I_{DD-APP}$	0.88
$I_{DD-NOP}$	0.72
$I_{DD-IDLE}$	0.43

Table 1. Internal Power Vectors and Dynamic Scaling Factors

The dynamic current consumption for a Blackfin processor in a specific application is calculated according to Equation 1, where “%” is the percentage of the overall time that the application spends in that state:

$$\begin{aligned}
 & (\% \text{ Peak activity level } \times I_{DD-PEAK} \text{ ASF } \times I_{DD-BASELINE-DYN}) \\
 & (\% \text{ High activity level } \times I_{DD-HIGH} \text{ ASF } \times I_{DD-BASELINE-DYN}) \\
 & (\% \text{ Typ. activity level } \times I_{DD-TYP} \text{ ASF } \times I_{DD-BASELINE-DYN}) \\
 & (\% \text{ App. activity level } \times I_{DD-APP} \text{ ASF } \times I_{DD-BASELINE-DYN}) \\
 & (\% \text{ NOP activity level } \times I_{DD-NOP} \text{ ASF } \times I_{DD-BASELINE-DYN}) \\
 & + (\% \text{ Idle activity level } \times I_{DD-IDLE} \text{ ASF } \times I_{DD-BASELINE-DYN}) \\
 & \hline
 & \text{Total Dynamic Current for } V_{DDINT} \text{ (} I_{DD-DYN} \text{)}
 \end{aligned}$$

Equation 1. Internal Dynamic Current ( $I_{DD-DYN}$ )

For example, after profiling the application code for a particular system, activity is determined to be proportioned as shown in Figure 2.

$$\begin{aligned}
 & (10\% \text{ Peak Activity Level}) \\
 & (20\% \text{ High Activity Level}) \\
 & (50\% \text{ Typ. Activity Level}) \\
 & (10\% \text{ App. Activity Level}) \\
 & (10\% \text{ NOP Activity Level}) \\
 & + (0\% \text{ Idle Activity Level}) \\
 & \hline
 & 100\% \text{ Activity}
 \end{aligned}$$

Figure 2. Internal System Activity Levels

Using the ASF provided for each activity level in [Table 1](#) (and with  $V_{DDINT}$  at 1.2 V and CCLK at 400 MHz), a value for the dynamic portion of the internal current consumption of a single processor can be estimated as follows:

$$\begin{aligned}
 & (10\% \times 1.33 \times 120) \\
 & (20\% \times 1.29 \times 120) \\
 & (50\% \times 1.00 \times 120) \\
 & (10\% \times 0.88 \times 120) \\
 & (10\% \times 0.72 \times 120) \\
 & + (0\% \times 0.43 \times 120) \\
 \hline
 I_{DD-DYN} &= 112.82 \text{ mA} \approx 113 \text{ mA}
 \end{aligned}$$

Figure 3. Internal Dynamic Current Estimation

The total estimated dynamic current on the  $V_{DDINT}$  supply in this example is ~113 mA.

### Estimating $I_{DDINT}$ Static Current, $I_{DD-DEEPSLEEP}$

Deep Sleep mode for Blackfin processors is when power is applied to the core and L1 memories, but all clocks are turned off. In this mode, the static current ( $I_{DD-DEEPSLEEP}$ ) measurement can be taken, which is the static component of overall average dissipation. Graphs for  $I_{DD-DEEPSLEEP}$  for the Blackfin processors are shown in [Figure 4](#) (high-performance processors) and in [Figure 5](#) (low-power processors). Static current on the  $V_{DDINT}$  power supply domain is a function of junction temperature ( $T_J$ ) and voltage, but it is *not* a function of frequency or activity level.

Therefore, unlike the dynamic portion of the internal current,  $I_{DD-DEEPSLEEP}$  need not be calculated for each discrete activity level or power vector. Using the  $I_{DD-DEEPSLEEP}$  curve corresponding to the application (i.e., at specific  $V_{DDINT}$ ),  $I_{DD-DEEPSLEEP}$  can be estimated vs.  $T_J$  of the Blackfin processor.



[Appendix A](#) discusses the methodology for estimating  $T_J$ . This process involves knowing the total power profile for the processor; therefore, this process will be iterative to arrive at a final calculation for expected power dissipation.

For example, in an application with  $V_{DDINT}$  at 1.2 V and a high-performance Blackfin processor at a  $T_J$  of +100°C, the corresponding  $I_{DD-DEEPSLEEP}$  for the  $V_{DDINT}$  power supply domain would be approximately 375 mA.

Similarly, in an application with  $V_{DDINT}$  at 1.2 V and a low-power Blackfin processor at a  $T_J$  of +100°C, the corresponding  $I_{DD-DEEPSLEEP}$  for the  $V_{DDINT}$  power supply domain would be approximately 100 mA.

The static power of the Blackfin processor is constant for a given voltage and temperature. Therefore, it is simply added to the total estimated dynamic current when calculating the total power consumption due to the internal circuitry of the Blackfin processor. Note that the  $I_{DD-DEEPSLEEP}$  currents shown in [Figure 4](#) and [Figure 5](#) represent the worst-case static current as measured across the wafer fabrication process for high-performance and low-power devices, respectively.

### ADSP-BF537/BF534\* Maximum Static Current

**( $I_{DD\_DEEPSLEEP}$ )**

\* For ADSP-BF534 processors, applies *only* to 500 MHz speed-grade models

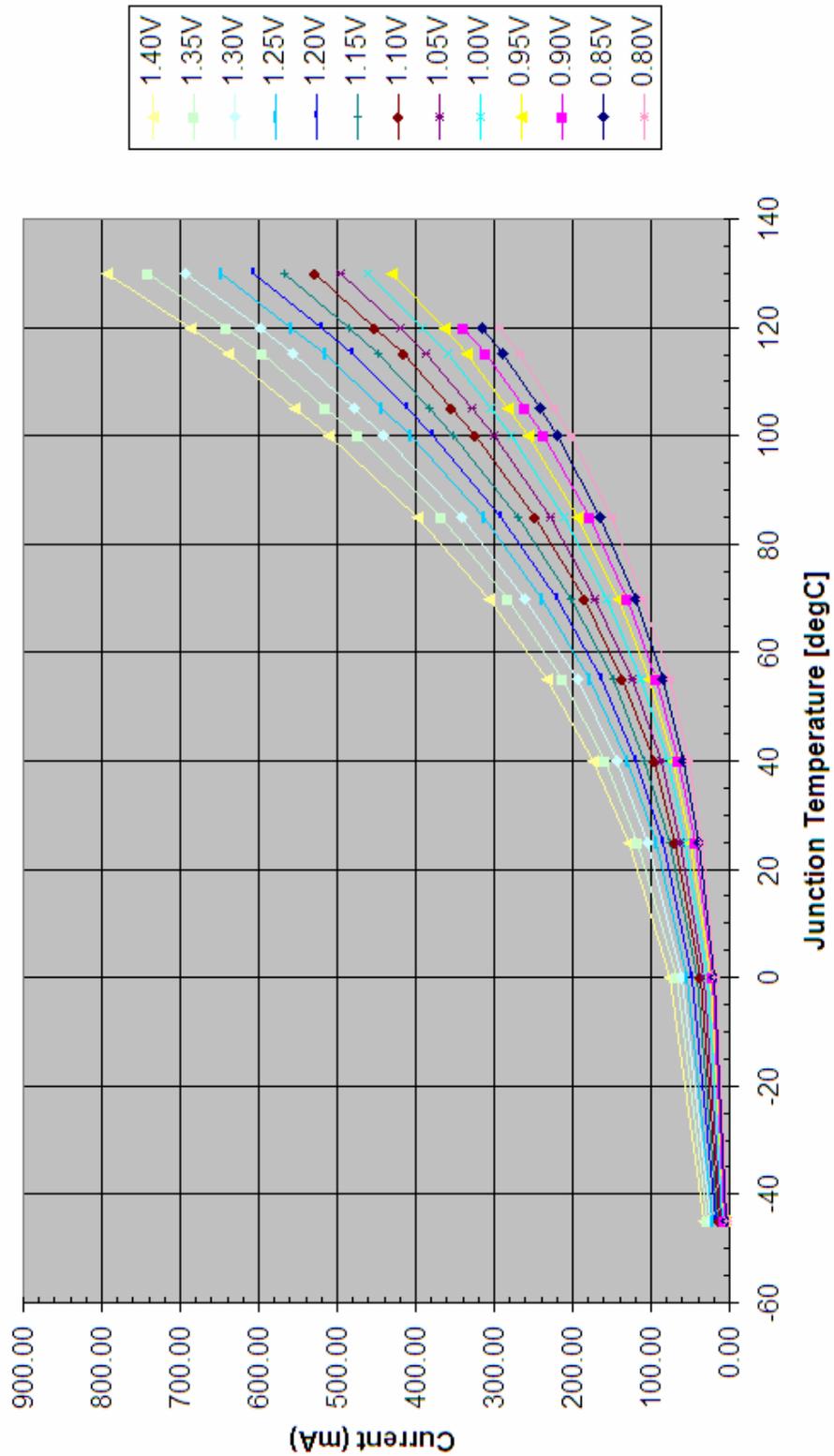


Figure 4. High-Performance  $I_{DD\_DEEPSLEEP}$  Static Current

### ADSP-BF536/BF534\* Maximum Static Current

( $I_{DD\_DEEPSLEEP}$ )

\* For ADSP-BF534 processors, applies *only* to 400 MHz speed-grade models

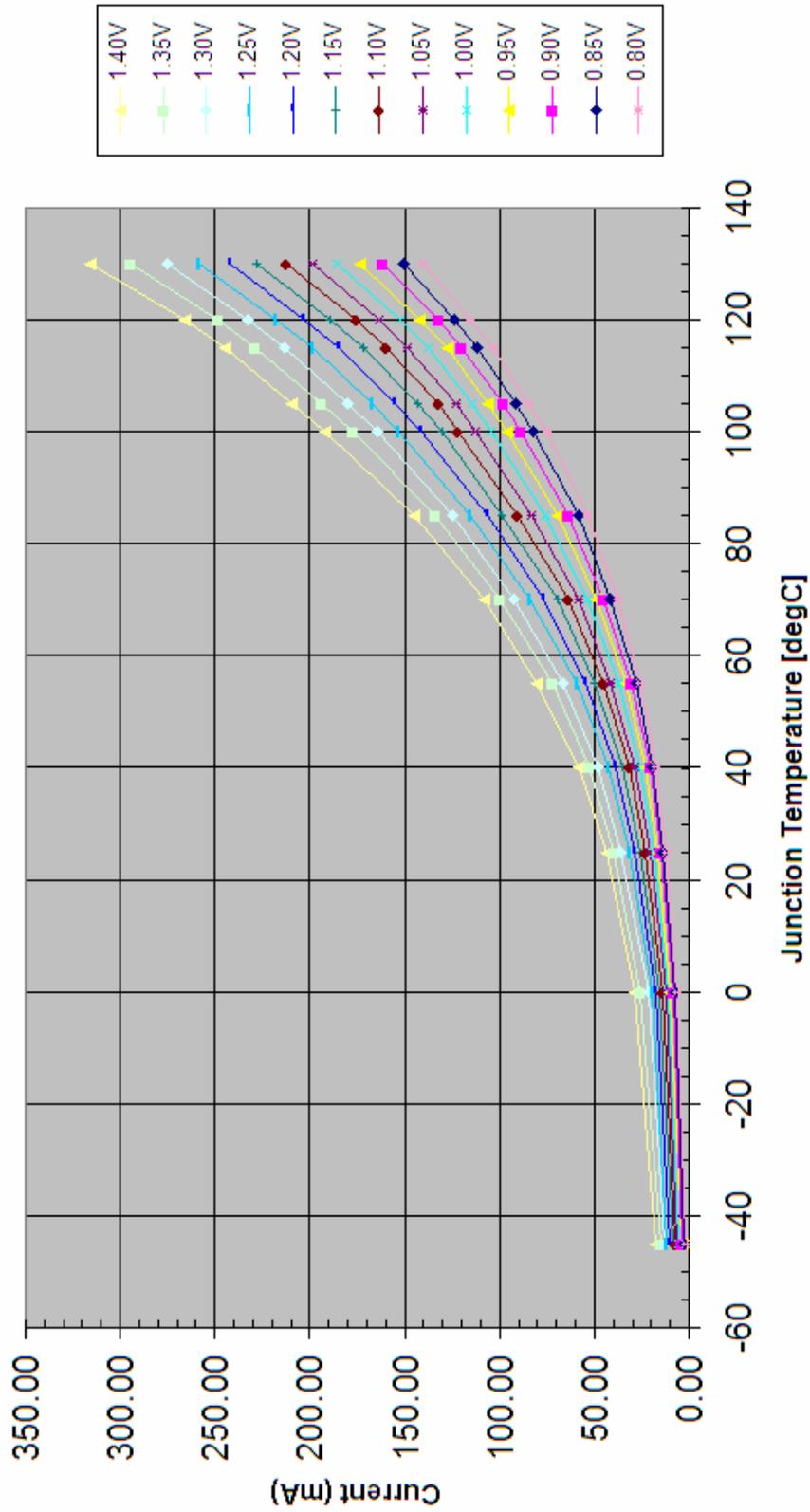


Figure 5. Low-Power  $I_{DD\_DEEPSLEEP}$  Static Current

## Estimating Total $I_{DDINT}$ Current

The total current consumption due to the internal core circuitry ( $I_{DDINT}$ ) is the sum of the dynamic current component and the static current component, as shown in [Equation 2](#).

$$I_{DDINT} = I_{DD-DYN} + I_{DD-DEEPSLEEP}$$

*Equation 2. Internal Core Current ( $I_{DDINT}$ ) Calculation*

Continuing with the example of the Blackfin processor operating at 1.2 V and 400 MHz (and with the code as profiled), assume that the resulting  $T_J$  is estimated to be +100°C. The total  $I_{DDINT}$  consumed by the high-performance processor core under these conditions would be:

$$I_{DDINT} = 113 + 379 = 492 \text{ mA}$$

*Equation 3.  $I_{DDINT}$  Estimation (High-Performance)*

The same estimate for the low-power processor core would be:

$$I_{DDINT} = 113 + 141 = 254 \text{ mA}$$

*Equation 4.  $I_{DDINT}$  Estimation (Low-Power)*

## Total Estimated Internal Power, $P_{DDINT}$

The resulting internal power consumption ( $P_{DDINT}$ ) is given by [Equation 5](#).

$$P_{DDINT} = V_{DDINT} \times I_{DDINT}$$

*Equation 5. Internal Power ( $P_{DDINT}$ ) Calculation*

Using [Equation 5](#), the total estimated internal power consumed by the high-performance processor in the application described in this example would be:

$$P_{DDINT} = 1.20V \times 492 \text{ mA} = 590 \text{ mW}$$

*Equation 6.  $P_{DDINT}$  Estimation (High-Performance)*

The same estimate for the low-power processor would be:

$$P_{DDINT} = 1.20V \times 254 \text{ mA} = 305 \text{ mW}$$

*Equation 7.  $P_{DDINT}$  Estimation (Low-Power)*

## Estimating External Power Consumption

External power consumption (on the  $V_{DDEXT}$  supply) is dependent on the enabled peripherals in a given system. Each unique group of peripheral pins contributes to a piece of the overall external power, based upon several parameters:

- $O$  - The number of output pins that switch during each cycle
- $f$  - The maximum frequency at which the output pins can switch
- $V_{DDEXT}$  - The voltage swing of the output pins
- $C_L$  - The load capacitance of the output pins
- $U$  - The utilization factor (the percentage of time that the peripheral is on and running)

In addition to the input capacitance of each device connected to an output, the total capacitance ( $C_L$ ) should include the capacitance of the processor pin itself ( $C_{OUT}$ ), which is driving the load.

Equation 8 shows how to calculate the average external current ( $I_{DDEXT}$ ) using the above parameters:

$$I_{DDEXT} = O \times f/2 \times V_{DDEXT} \times C_L \times U$$

*Equation 8. External Current ( $I_{DDEXT}$ ) Calculation*

The worst-case external pin power scenario occurs when the load capacitor charges and discharges continuously, requiring the pin to toggle each cycle. Since the state of the pin can change only once per cycle, the maximum toggling frequency is  $f/2$ . In terms of supply power, the worst-case  $V_{DDEXT}$  value is 3.6 V. Table 2 contains data for a realistic example of a PPI application, which runs several peripherals simultaneously. Actual results may vary, but again, the intent of this document is to help designers size the power supplies.

Estimated average external power consumption ( $P_{DDEXT}$ ) can be calculated as follows.

$$P_{DDEXT} = V_{DDEXT} \times I_{DDEXT}$$

*Equation 9. External Power ( $P_{DDEXT}$ ) Calculation*

Using the sample Blackfin system configuration in Figure 6, the external current and, therefore, the external power consumption can be estimated.

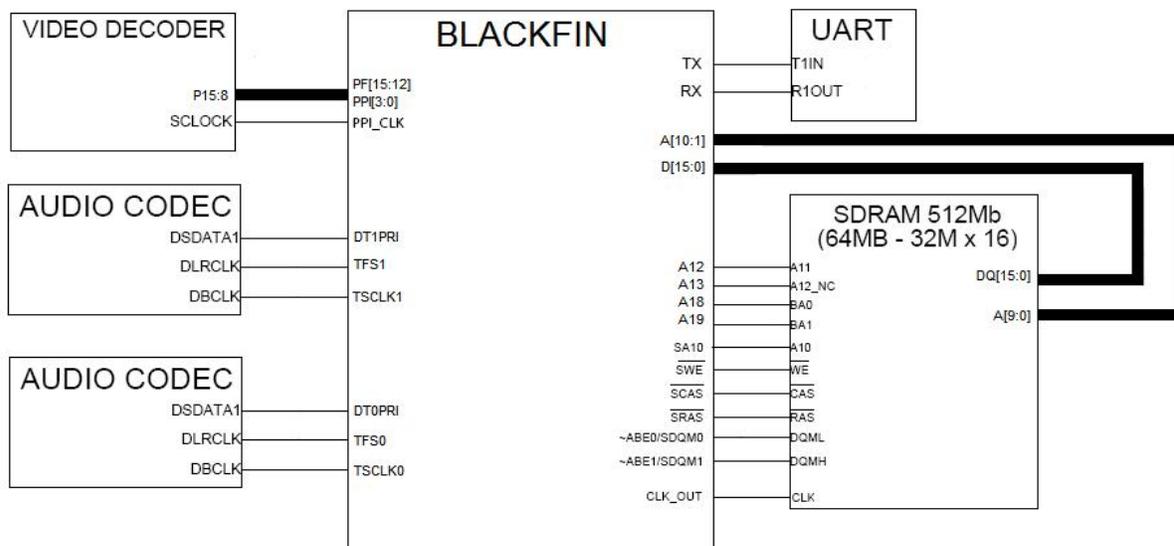


Figure 6. Blackfin System Sample Configuration

$I_{DDEXT}$  (Equation 8) can be calculated for each class of pins that can drive, as shown in Table 2.

Peripheral	Freq (Hz)	# of pins	C/pin (F)	Toggle Ratio	Util	Vddext (V)	Pout @ 3.6V (mW)
PPI	27.00E+06	9	30.00E-12	1	1.00	3.6	47.24
SPORT0	4.00E+06	2	30.00E-12	1	1.00	3.6	1.56
SPORT1	4.00E+06	2	30.00E-12	1	1.00	3.6	1.56
UART	115.00E+03	2	30.00E-12	1	0.25	3.6	0.01
SDRAM	133.33E+06	36	30.00E-12	0.25	0.50	3.6	116.35
Total External Power Dissipation @ 3.6 V (est. mW)							166.71

Table 2. Sample Calculation for Total Average External Power

In the above example, the total average external power consumption is estimated to be ~165 mW. This number was obtained with the parameters listed in Table 2 by applying Equation 10. The chosen operating frequencies are reasonable for each of the peripherals, including the maximum allowed SDRAM frequency of 133.33 MHz. This model assumes that each output pin changes state every clock cycle, which is a worst-case model, except in the case of the SDRAM (because the number of output pins transitioning each clock cycle will be less than the maximum number of output pins). Table 2 was taken from the *External Power Spreadsheet*<sup>[2]</sup>, which is associated with this EE-Note. It contains calculations for four sample systems. The reader can tailor this spreadsheet to the application, adding or deleting rows as necessary. Since the equation provides results in Watts (W), an additional multiplier of 1000 in the spreadsheet converts results into mW.

This equation is a more theoretically accurate version of the one used in the spreadsheet:

$$\overline{P}_{ext} = V_{DDext}^2 \cdot \sum_{All-Output-Pins} C_L \cdot \overline{f}$$

#### Equation 10. Alternate External Power ( $P_{DDEXT}$ ) Calculation

Rather than estimating average external power dissipated in each *peripheral*, the estimate applies to each *individual output pin*, based on the pin's load capacitance and average toggling frequency. The voltage swing is uniform across all output pins within the  $V_{DDEXT}$  supply domain, so it is multiplied by the summation of the dynamic charge changes on each output.

Using the PPI data in [Table 2](#), nine output pins change every cycle at an average frequency of 27 MHz. Since toggling between on-to-off and off-to-on requires two cycles,  $F_{AVG}$  (13.5 MHz) is half the PPI clock. Since each pin changes at the same rate and the pin capacitance is presumed to be the same, the summation is simply nine times the value of any one PPI pin. Applying [Equation 10](#):

$$\begin{aligned} P_{EXT\_AVG} &= V_{DDEXT}^2 * 9 \text{ pins} * (F_{AVG} * C_L) \\ &= (3.6)^2 * 9 * 13.5e6 * 30e-12 \\ &= 12.96 * 0.003645 \\ &= 0.047239W \\ &= 47.239mW \end{aligned}$$

As can be seen, the value derived using this equation is the same as the value estimated in [Table 2](#). This model obtains the same estimate on a per-pin basis rather than a per-peripheral basis.

In addition to the peripheral pins, there is one other output pin on Blackfin processors that will contribute to the  $V_{DDEXT}$  supply domain power profile if the system uses a crystal to provide the  $CLKIN$  signal to the processor. In this case, the processor drives the  $XTAL$  output pin when the PLL is active. The output drive frequency will be exactly the  $CLKIN$  rate, and the pin capacitance value can be obtained from the appropriate data-sheet. Note that the voltage swing will likely be less than  $V_{DDEXT}$  for most crystals, and using  $V_{DDEXT}$  in computations would be a worst-case model in terms of profiling power dissipation.

Finally, designers must be mindful of power supply efficiency when sizing the  $V_{DDEXT}$  supply. *Switching Regulator Design Considerations for ADSP-BF533 Blackfin Processors (EE-228)*<sup>[3]</sup> describes the internal voltage regulator.

### Real-Time Clock (RTC) Power Consumption

The final source of total power consumption comes from the optional third power domain, the Real-Time Clock (RTC) power domain ( $V_{DDRTC}$ ), which is a specified value. The RTC can be powered between 2.25 V and 3.6 V. For a worst-case analysis, a supply voltage of 3.6 V yields a current draw,  $I_{DDRTC}$ , of 30 to 50  $\mu$ A for a range of ambient temperature from 25 °C to 85 °C. For the sake of including this number in the final power consumption estimate, the power dissipated in the RTC domain,  $P_{DDRTC}$  is:

$$P_{DDRTC} = V_{DDRTC} \times I_{DDRTC}$$

#### Equation 11. Total Power ( $P_{DDRTC}$ ) Calculation

Knowing this value helps in selecting a battery as a potential power source for the RTC. The RTC can be used to take the Blackfin processor out of any low-power operating mode. Having a battery supply  $V_{DDRTC}$  allows the removal of the  $V_{DDINT}$  and  $V_{DDEXT}$  supplies, thus significantly reducing total average power consumption. As a worst-case example,  $P_{DDRTC}$  is 180  $\mu$ W, which is the product of the maximized  $V_{DDRTC}$  (3.6 V) and the high end of the  $I_{DDRTC}$  range (50  $\mu$ A) provided in the data sheet.

## Total Power Consumption

For a given system, total power consumption is the sum of its individual components - power consumed by internal circuitry, power consumed due to switching I/O pins, and power consumed by the RTC circuitry, as follows:

$$P_{TOTAL} = P_{DDINT} + P_{DDEXT} + P_{DDRTC}$$

Equation 12. Total Power ( $P_{TOTAL}$ ) Calculation

Where:

$P_{DDINT}$  = Internal power consumption as defined by Equation 5

$P_{DDEXT}$  = External power consumption as defined by Equation 9

$P_{DDRTC}$  = RTC power consumption as defined by Equation 11

For example, assuming that the processor in Figure 6 is operating under the conditions detailed in the example (the processor operating at 1.2 V, 400 MHz, and code as profiled in Figure 2), and also assuming that the resulting  $T_j$  has been estimated to be +100°C (see Appendix A for estimating  $T_j$ ), the total estimated power consumed for the high-performance processor would be:

$$P_{TOTAL} = 590 \text{ mW} + 166.71 \text{ mW} + 0.18 \text{ mW} = \sim 757 \text{ mW}$$

Figure 7. Total Power ( $P_{TOTAL}$ ) Calculation for Sample Shown in Figure 6 While Running Code Described in Equation 6 for High-Performance Processors

Similarly, the total estimated internal power consumed by the low-power processor under these same conditions would be:

$$P_{TOTAL} = 305 \text{ mW} + 166.71 \text{ mW} + 0.18 \text{ mW} = \sim 472 \text{ mW}$$

Figure 8. Total Power ( $P_{TOTAL}$ ) Calculation for Sample Shown in Figure 6 While Running Code Described in Equation 7 for Low-Power Processors

## Conclusion

Several variables affect the power requirements of an embedded system. Measurements published in the Blackfin processor data sheets are indicative of typical parts running under typical conditions. However, these numbers do not reflect the actual numbers that may occur for a given processor under non-typical conditions. In addition to the type of silicon that the customer could have, the ambient temperature, core and system frequencies, supply voltages, pin capacitances, power modes, application code, and peripheral utilization contribute to the average total power that may be dissipated.

The average power estimates obtained from methods described in this EE-Note indicate how much the Blackfin processor loads a power source over time. These estimates are useful in terms of expected power dissipation within a system, but designs must support worst-case conditions under which the application can be run. Do not use this calculation to size the power supply, as the power supply must support peak requirements.

## Appendix A

For Blackfin processors, the total power budget is limited by the maximum allowed junction temperature ( $T_J$ ) of the device. Please see the processor data sheet for the maximum  $T_J$  specification.

To guarantee correct operation, ensure that  $T_J$  does not exceed the maximum  $T_J$  specification. Use the following equation to determine  $T_J$  of the device while on the application's printed circuit board (PCB):

$$T_J = T_T + (P_{TOTAL} \times \psi_{JT})$$

Equation 13. Junction Temperature ( $T_J$ ) Calculation

Where:

$T_T$  = Package temperature ( $^{\circ}\text{C}$ ) measured at the top center of the package

$P_{TOTAL}$  = Total power consumption (W) as defined in [Equation 12](#)

$\psi_{JT}$  = Junction-to-top (of package) characterization parameter ( $^{\circ}\text{C}/\text{W}$ )

Under natural convection,  $\psi_{JT}$  for a thin plastic package is relatively low. This means that under natural convection conditions, the typical  $T_J$  is just a little higher than the temperature at the top-center of the package ( $T_T$ ). The die is physically separated from the surface of the package by only a thin region of plastic mold compound. Unless the top of the package is forcibly cooled by significant airflow, there will be very little difference between  $T_T$  and  $T_J$ . However, note that  $\psi_{JT}$  is affected by airflow and values for  $\psi_{JT}$  under various airflow conditions, and PCB design configurations are listed in the *Thermal Characteristics* section of the Blackfin processor data sheets for the 182-ball mini-BGA and the 208-ball sparse mini-BGA packages.

The *Thermal Characteristics* section of the respective data sheet also provides thermal resistance ( $\theta_{JA}$ ) values for all available packages. Data sheet values for  $\theta_{JA}$  are provided for package comparison and PCB design considerations only and are not recommended for verifying  $T_J$  on an actual application PCB.

Industrial applications of the mini-BGA package require thermal vias to an embedded ground plane on the PCB. Refer to JEDEC standard JESD51-9 for printed circuit board thermal ball land and thermal via design information.

## References

- [1] *ADSP-BF534/ADSP-BF536/ADSP-BF537 Blackfin Embedded Processor Data Sheet*. Rev. D, September 2007. Analog Devices, Inc.
- [2] *External Power Spreadsheet. Associated file with Estimating Power for ADSP-BF534/ADSP-BF536/ADSP-BF537 Blackfin Processors (EE-297)*. Rev 3, November 2007. Analog Devices, Inc.
- [3] *Switching Regulator Design Considerations for ADSP-BF533 Blackfin Processors (EE-228)*. Rev 1, February 2005. Analog Devices, Inc.

## Document History

Revision	Description
<i>Rev 3 – November 21, 2007 by Joe B.</i>	Clarified ADSP-BF534 processor offering as either low-power or high-performance
<i>Rev 2 – May 18, 2007 by Joe B.</i>	Updated to include full power characterization data
<i>Rev 1 – September 6, 2006 by Joe B.</i>	Initial Release