AN-873
APPLICATION NOTE

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Lock Detect on the ADF4xxx Family of PLL Synthesizers

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INTRODUCTION

This application note covers the ADF4xxx family of integer-N PLL synthesizers and the ADF4360-x family of integrated phase locked loop (PLL) synthesizers and voltage controlled oscillators (VCO). (See the Appendix for a full list of the ADF4xxx parts covered in the AN-873 application note.) There are two forms of lock detect available on each part: analog lock detect (ALD) and digital lock detect (DLD). Each has its advantages and disadvantages, depending on the application. The aim of this application note is to explain both options and allow the user to make an informed decision as to which form of lock detect to use.

Both ALD and DLD use the phase error at the phase frequency detector (PFD) inputs to decide whether the PLL is in lock. Figure 1 shows the PFD and charge pump block.

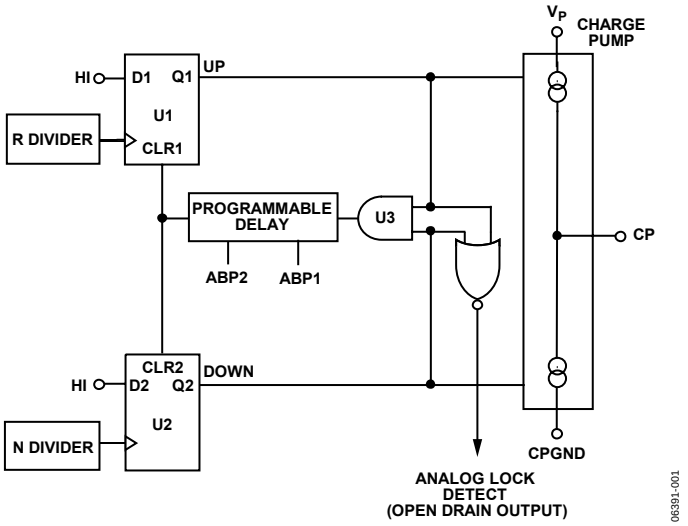

Figure 1. PFD and Charge Pump on the ADF4xxx Family of PLL Synthesizers

DIGITAL LOCK DETECT

Digital lock detect outputs either a CMOS logic high, indicating a locked PLL state, or a logic low, indicating an unlocked state. The state diagram for DLD is shown in Figure 2, and a simplified circuit diagram is shown in Figure 3. It works by measuring the phase error at the PFD inputs and using a window of 15 ns phase error to decide the lock status of the PLL.

When the phase error at the PFD inputs on five or more consecutive cycles is inside the 15 ns window, it considers the PLL to be in lock and outputs a logic high.

When the phase error drifts outside of the loss of lock threshold (30 ns) on any subsequent PFD cycle, it registers an out-of-lock condition, that is, a logic low. In some of the PLL parts, the windows are set by the R_{SET} resistor (see the Digital Lock Detect—Dependence on R_{SET} section). The 15 ns window and the 30 ns window are for an R_{SET} resistor of 4.7 kΩ.

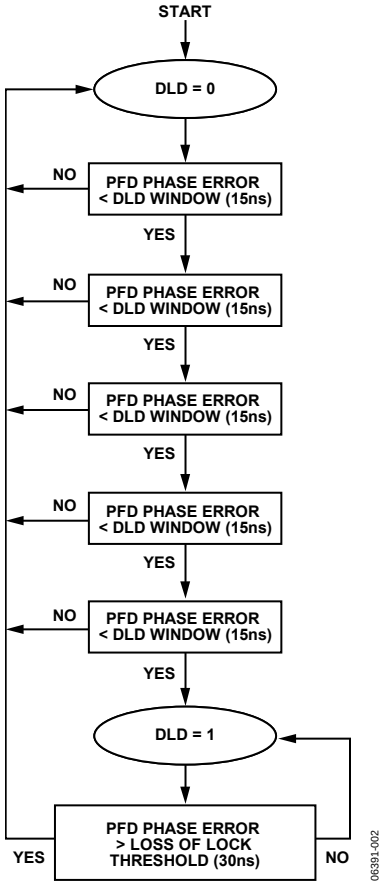

Figure 2. State Diagram for Digital Lock Detect (Lock Detect Precision (LDP) is 5 in This Case)

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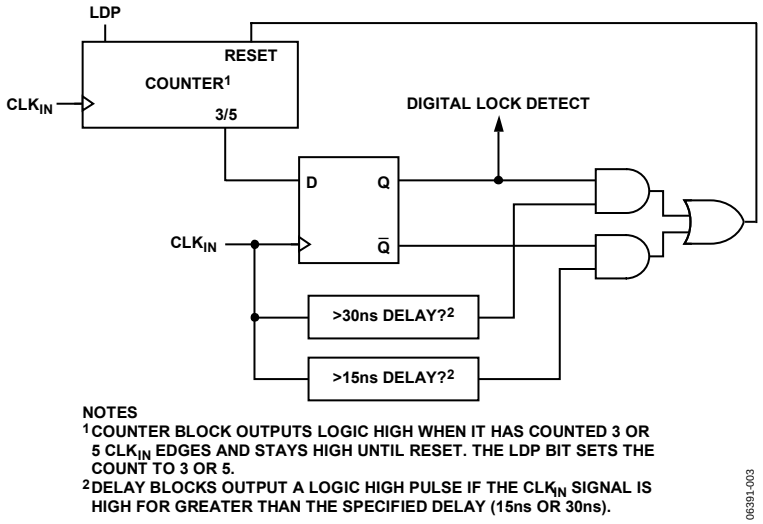

Figure 3. Simplified Circuit Diagram for Digital Lock Detect; CLK_{IN} is the Analog Lock Detect Signal

The lock detect precision (LDP) bit in the R-counter latch sets the number of cycles that are counted before lock is registered. There is a choice of three or five cycles.

ANALOG LOCK DETECT

Analog lock detect (ALD) is the NOR of the up and down signals going from the PFD to the charge pump (see Figure 1).

When the PLL is in lock, the edges at the PFD inputs are almost in phase, as shown in Figure 4. In this case, the PFD outputs consist of very short pulses of Q1 and Q2. The logical NOR of these produces a high signal with low-going pulses. The duration of the low-going pulse is equal to the duration of the antibacklash pulse width set in the R-counter latch. Figure 4 shows a timing diagram of a locked PLL and the corresponding output from ALD.

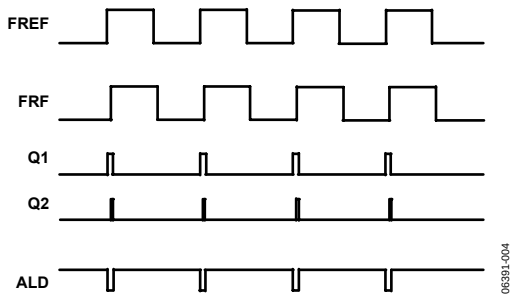

Figure 4. Timing Diagram of PLL in Lock Showing the Reference Signal, Divided RF Signal, Q1 and Q2 (the Up and Down Pulses Going from the PFD to the Charge Pump), and the ALD Signal, which is the NOR of Q1 and Q2

This signal needs to be filtered off-chip to remove the low going pulses. The filter is an analog dual-time constant filter, as shown in Figure 5. Analog lock detect is an open drain output.

When the NOR of Q1 and Q2 is high, Capacitor C1 charges through R2. When it is low, C1 discharges through R1. Through careful filter design, the lock detect output can give an accurate representation of the lock status of the PLL. ADIsimPLL™ aids the design of the filter (refer to www.analog.com/pll).

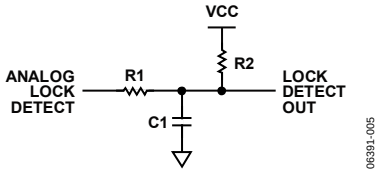

Figure 5. Analog Lock Detect Off-Chip Filtering by R1, R2, and C1; Analog Lock Detect is an Open Drain Output

GENERAL PERFORMANCE

Digital lock detect declares lock before the PLL has settled to final frequency and phase. This is because the phase error is <15 ns for more than five consecutive cycles before final frequency and phase are settled. Figure 6 shows a simulation of the frequency error for a 35 MHz frequency jump and the corresponding ALD (blue) and DLD (red) signals. The PLL is locked in less than 300 µs; DLD goes high about 150 µs before this. Analog lock detect, on the other hand, does not reach a steady high level until final frequency and phase have reached their settled values, due to the filtering on the output of ALD.

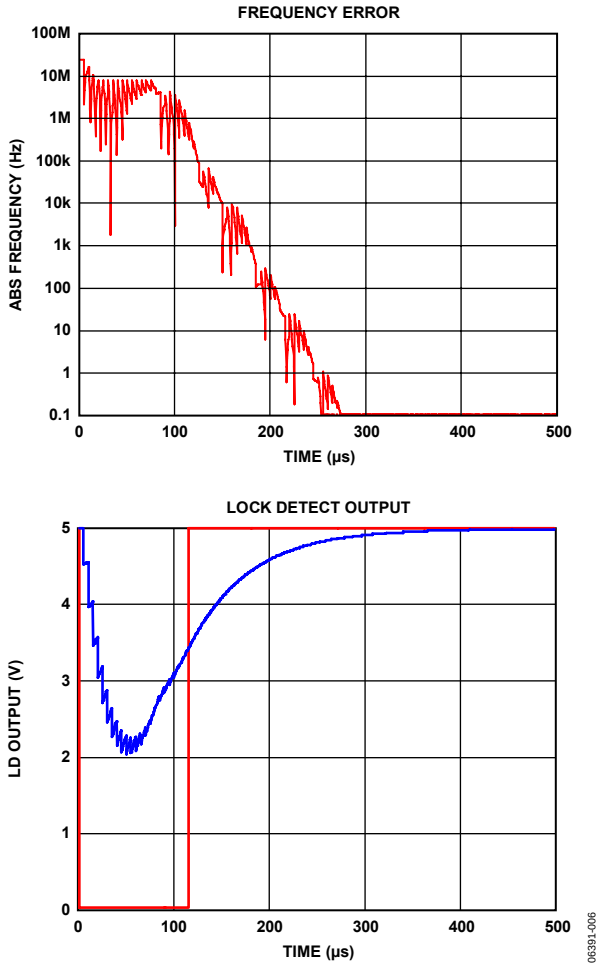

Figure 6. Frequency Error for a 35 MHz Frequency Jump and Corresponding ALD (Blue) and DLD (Red) Signals

Conversely, when an unlocked condition occurs, DLD goes low almost immediately; ALD may take some time to reduce to a low level.

PERFORMANCE VS. PFD FREQUENCY

Digital lock detect becomes less accurate at high PFD frequencies (>15 MHz). This is because the period of the PFD frequency begins to approach the 15 ns window used to check for lock. For example, a 25 MHz PFD frequency has a period of 40 ns. In such a case, the accuracy of digital lock detect is compromised. In an unlocked state, if the unlocked frequency is close to the desired frequency, the phase error at the PFD drifts in and out of the 15 ns window, causing the DLD signal to pulse high and low.

More seriously, sometimes if a voltage-controlled crystal oscillator (VCXO) is used, the unlocked signal may not differ enough in phase from the REFIN frequency. This is because VCXOs have such a narrow frequency range. For example, if a 50 MHz PFD is used, it has a 20 ns period. The PLL is in lock, and a locked signal activates a logic high.

Increasing the REFIN frequency causes the VCXO to track the frequency until it reaches the maximum frequency of the VCXO (for example, 50 MHz + 1 ppm) and cannot track the reference signal anymore. The PLL is no longer in lock. However, because the period of both signals is >20 ns, the digital lock detect never has a phase error of >30 ns, and digital lock detect continues to indicate logic high.

The accuracy of analog lock detect does not degrade to the same degree at higher PFD frequencies. However, the voltage level of the high signal may decrease slightly as the width of the low going pulse from ALD becomes a more significant portion of the whole PFD period. The duration of the low going pulse is equal to the duration of the antibacklash pulse width set in the R-counter latch. Thus, at higher PFD frequencies, the smaller pulse width is preferable.

Equally in the unlocked state, any high-going pulses become more significant and act to raise the unlocked voltage of the lock detect signal. The signal level should not be raised or lowered by enough to go outside CMOS high and low levels, however. For this reason, analog lock detect is a better option when the PFD frequency is >15 MHz.

At low PFD frequencies, leakage currents have more of an effect. Leakage currents and their effect on ALD and DLD performance are discussed next.

LEAKAGE CURRENTS

Leakage currents flowing from or into the loop filter may affect the performance of ALD and DLD. Leakage can have many sources, including leakage through the charge pump, VCO tuning port, loop filter capacitors, or biasing currents for active loop filters. The PFD and charge pump must act to replace the charge lost on each PFD cycle to keep the VCO tuning voltage constant and keep the PLL in lock. To achieve this, the PLL forces a phase error at the PFD inputs. This allows the charge pump to turn on for long enough to replace the charge lost on each PFD cycle. Leakage currents have more of an effect at lower PFD frequencies because the charge pump is in three-state for a longer period of time, allowing more current to leak.

The phase error at the PFD inputs in seconds, resulting from the leakage current, is approximately

$$Phase\ Error = \frac{Leakage\ Current}{I_{CP}} \times t_{PFD} \quad (1)$$

where:

I_{CP} is the charge pump current.

t_{PFD} is the period of the PFD frequency.

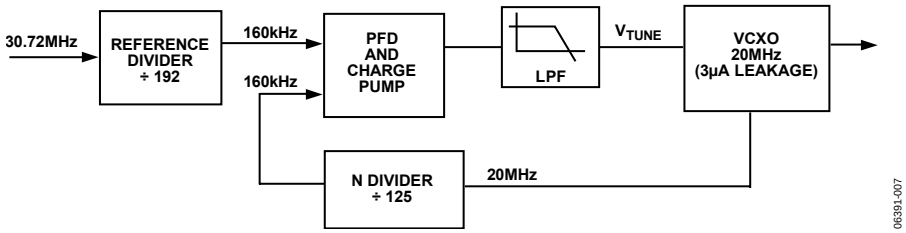

Figure 7. PLL with 20 MHz Derived from a 30.72 MHz Reference

Taking an example application where a 20 MHz clock is being derived from a 30.72 MHz reference: The 30.72 MHz is divided by 192 to 160 kHz, which is presented to the PFD. This is then multiplied by 125 to get the 20 MHz output frequency. A 20 MHz VCXO with a maximum leakage current of 3 µA is the tuneable oscillator. Figure 7 shows the block diagram of the PLL.

Calculating the phase error at the PFD inputs using Equation 1 gives the following:

$$Phase\ Error = \frac{3\,\mu A}{1\,mA} \times 6.25\,\mu s = 18.75\,ns$$

If digital lock detect is used in this application, the 18.75 ns phase error at the PFD inputs is outside the 15 ns window. Thus, DLD does not go high, even though the PLL is in lock. However, from Equation 1 we can see that increasing I_{CP} reduces phase error. So increasing I_{CP} by a factor of 4 brings the phase error down to 4.7 ns, back inside the DLD window; and DLD works again. Increasing charge pump current is not always an option, however, because it may make loop filter capacitor sizes unreasonable.

Analog lock detect is more robust in the presence of leakage. However, in the locked state, the low-going pulses are longer, due to the increased phase error at the PFD inputs caused by the leakage. These pulses need more aggressive filtering in order to keep the locked voltage level of ALD high. In the ALD filter (Figure 5), Resistor R1 should be increased to slow the discharge of Capacitor C1 during the low-going pulses. Equally, Resistor R2 can be decreased to speed the charging of C1 during the high pulses. The effect of changing these values, and their effect on the ALD voltage level in the presence of leakage, can be simulated in ADIsimPLL.

CYCLE SLIPPING

Cycle slipping occurs in PLLs when the phase error at the PFD inputs accumulates faster than the PLL can correct for. They can be recognized by characteristic kinks in the settling transient, where the charge pump momentarily drives the tuning voltage in the wrong direction (see Figure 8). Though more common in fractional-N synthesizers, cycle slips may also occur in integer-N synthesizers when the PFD frequency is much greater than the loop bandwidth. (PFD:loop bandwidth ratios of >100:1 usually result in cycle slips.)

Around a cycle slip, the error at the PFD inputs can drop below the lock detect window for a number of cycles, causing digital lock detect to be asserted. DLD stays high until the error at the PFD exceeds the loss of lock threshold. In a settling transient with many cycle slips, this may occur many times, causing DLD to pulse high and low until the frequency finally settles. In this case, DLD is reliable only as a loss-of-lock detector. With a carefully designed filter, analog lock detect can be more reliable as a lock indicator during the presence of cycle slips.

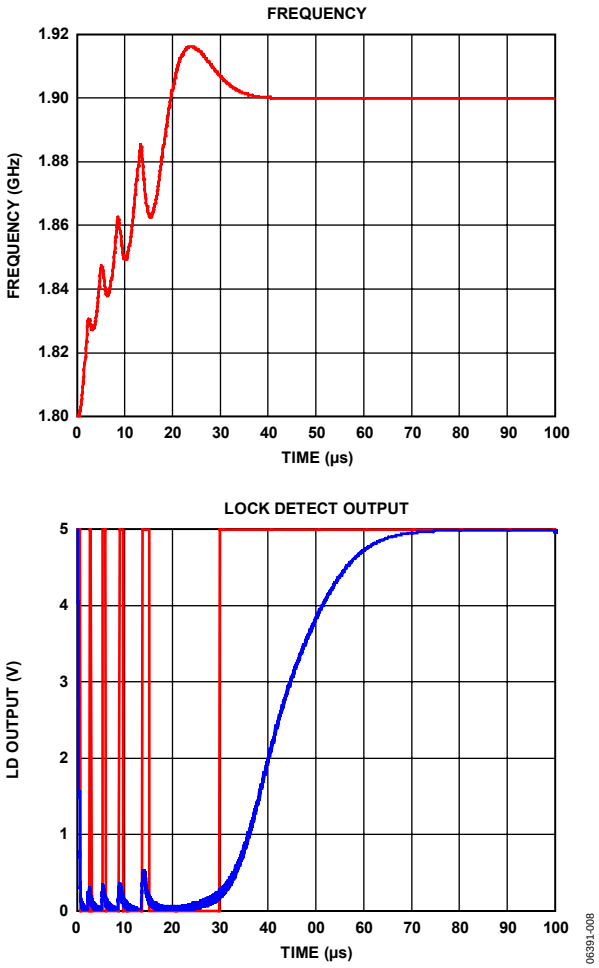

Figure 8. Cycle Slipping During a Settling Transient and the Corresponding DLD (Red) and ALD (Blue) Outputs; DLD Pulses High and Low During the Settling Transient

DIGITAL LOCK DETECT—DEPENDENCE ON R_{SET}

The timing window that digital lock detect uses to check for lock is nominally 15 ns. However, on the ADF41xx, the ADF42xx, and the ADF4001/ADF4002 synthesizers, this window is determined by the R_{SET} value. Figure 9 shows that the DLD window increases with the value of R_{SET}. The nominal value is 15 ns for an R_{SET} of 4.7 kΩ. The loss of lock threshold also increases with R_{SET} value. After DLD goes high, the phase error at the PFD must exceed the loss of lock threshold for one PFD cycle for DLD to go low. This is 30 ns, nominally, for an R_{SET} of 4.7 kΩ.

Figure 9. DLD Window and Loss of Lock Threshold vs. R_{SET} Value; the Allowable Range for R_{SET} is 2.7 kΩ to 10 kΩ. These windows can vary by 10% of the nominal value shown in the diagram.

The ability to control the digital lock detect window can be seen as an advantage in some applications. In the example shown in Figure 7 where leakage currents render digital lock detect unusable, changing R_{SET} from 4.7 kΩ to 10 kΩ increases the DLD window to ~28 ns. This brings the maximum phase error of 18.75 ns back inside the DLD window, and DLD works again. Note that changing R_{SET} also changes the charge pump current value. The charge pump current programmable setting should be changed to keep the charge pump current value constant when R_{SET} is changed. This ensures that the loop dynamics do not change.

In applications where a high PFD frequency is used, the value of R_{SET} can be reduced. This has the effect of decreasing the DLD window and making it a less significant portion of the whole PFD period, resulting in greater DLD accuracy.

On the ADF4360-x, the DLD window and loss-of-lock threshold are fixed at 15 ns and 30 ns, respectively, regardless of R_{SET} value.

DIGITAL LOCK DETECT—DEPENDENCE ON ANTIBACKLASH PULSE WIDTH

The antibacklash pulse width has a small effect on the operation of digital lock detect. This can be ignored in most applications, but it may need to be taken into account in extreme cases.

From Figure 3, DLD uses the analog lock detect signal to check for lock. Analog lock detect always has a low going pulse equal to the antibacklash pulse width. This pulse adds to any phase error present at the PFD inputs due to leakage. This should be taken into account when calculating PFD phase error as seen by the DLD circuitry.

For example, if there is a 10 ns phase error at the PFD inputs due to leakage and the ABPW is set to 1.3 ns, the total phase error seen by the DLD circuitry is 11.3 ns.

CONCLUSION

The AN-873 application note presents the advantages and disadvantages of ALD and DLD. By its digital nature, DLD has to make a definite yes-or-no decision as to whether or not a PLL is in lock. Under certain circumstances, as described in this application note, DLD is susceptible to inaccuracies. Through careful consideration of the PFD frequency and leakage currents flowing, it is possible to determine if DLD is accurate in a particular application.

After filtering, ALD can have more than just a 0 or 1 representation of a PLL lock status. The output voltage level can more accurately portray the lock status. However, the filter must be designed carefully, and the rise and fall times of the output voltage level can be an issue in some applications.

APPENDIX

A list of part numbers covered by this application note follows:

ADF40xx	**ADF41xx**	**ADF42xxx**	**ADF43xx-x**
ADF4001	ADF4106	ADF4206	ADF4360-x
ADF4002	ADF4107	ADF4207	
ADF4007	ADF4108	ADF4208	
	ADF4110	ADF4210	
	ADF4111	ADF4211	
	ADF4112	ADF4212	
	ADF4113	ADF4212L	
	ADF4116	ADF4213	
	ADF4117	ADF4216	
	ADF4118	ADF4217	
		ADF4218	
		ADF4218L	
		ADF4219L	

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