

## Generating Multiple Clock Outputs from the AD9540

by Ted Harris

In today's digital and mixed-signal electronic systems, clocking is an important consideration for overall system performance. The ability to generate clocks at specific rates with low jitter is vital to the proper functioning of analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). This is because uncertainty in the time domain, characterized as jitter, translates to uncertainty in amplitude, reducing the achievable noise floor and corresponding figures of merit, such as signal-to-noise ratio (SNR) and increasing the bit error rate (BER). For more information on how clock jitter can affect ADC or DAC performance, see Application Note AN-756. Other challenges faced in generating clocks include frequency accuracy, frequency resolution and the ability to introduce timing skew, and phase delay between different channels.

To meet these challenges, Analog Devices offers a family of clock generation and clock distribution products. One of ADI's first offerings, the AD9540, is a low jitter clock generation integrated circuit (IC). The AD9540 features a low jitter clock output from its current mode logic (CML)

driver capable of achieving rates of up to 655 MHz, suitable for clocking ADCs and DACs. Frequently, in a mixed-signal system, additional clocks are needed to clock digital hardware. While jitter is not as much of a concern in strictly digital systems, the ability to provide precise frequency resolution and to introduce controlled delays on the rising edges of the clock waveform are important. This application note discusses how to achieve a low jitter, high speed 622.08 MHz clock for OC-12 applications along with a lower rate clock with programmable skew, such as regeneration of the Frame SYNC reference. Both of these network clocks can be derived from a single AD9540 IC.

The block diagram is shown in Figure 1. An overview shows that all the necessary component blocks are present for generating both of the needed clocks. In generating low jitter clocks, it is almost always preferable to employ a phase-locked loop (PLL) circuit of some sort. Beyond providing frequency gain, PLL circuits offer great noise reduction capability because the loop filter will act as a tracking band-pass filter. Because in most clocking

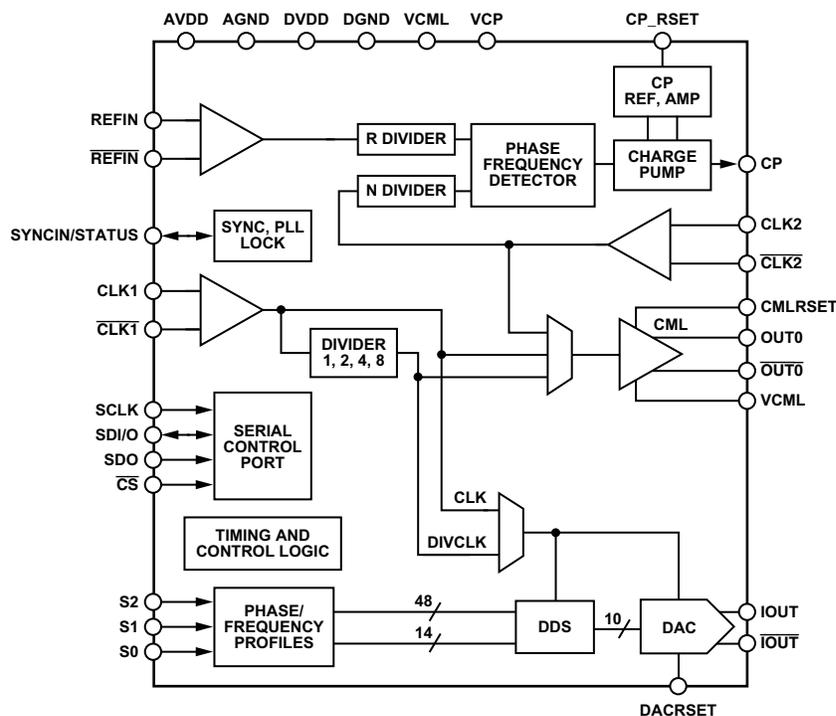


Figure 1. AD9540 Block Diagram

applications a single frequency is required, parameters such as acquisition time and tuning range are not of importance, so performance in these areas can be sacrificed to improve the noise performance of the loop. Specifically, a very narrow range VCO can be selected with a center frequency close to the desired clock rate. As the tuning range is reduced, the gain coefficient for the VCO ( $K_v$ ) is reduced, and the phase noise of the VCO itself is thereby reduced.

Also, the loop filter bandwidth is a concern for designers in that there is a trade-off associated with this parameter. Generally speaking, the wider the loop bandwidth, the faster the acquisition and lock time of a loop, but more noise from the reference and phase frequency detector itself gets fed through the loop. In the case of a clocking application, this trade-off can be made to achieve narrow loop bandwidths, sacrificing settling time in favor of noise suppression through the loop.

The digital clock requires precise frequency and adjustable phase that can be generated from the direct digital synthesizer (DDS) portion of the device. The DDS on the AD9540 offers 48-bit frequency tuning resolution ( $1.42 \mu\text{Hz}$ , given the maximum clock rate of 400 MHz) and 14-bit phase adjustment (0.022 degrees). The output

of a DDS is a reconstructed sine wave, so two additional external circuits are required. First, a band-pass filter at the desired clock rate needs to be applied to the reconstructed sine wave. This will remove most sampling artifacts from the output spectrum as well as remove broadband noise that has infected the DAC output signal. Second, in order to achieve the required slew rates for most clock circuits, an external comparator needs to be inserted into the clock signal path. One excellent choice, used for this example, is the ADCMP563.

A simplified block diagram for the resultant circuit is shown in Figure 2. Inputs  $\text{CLK1}/\overline{\text{CLK1}}$  are shorted to  $\text{CLK2}/\overline{\text{CLK2}}$ . The device is programmed such that the CML driver gets its input from the undivided input from CLK1, but the DDS is clocked by the divided output (622 MHz divided by 2 = 311 MHz). The drawing shows the crystal oscillator capability of the REF input of the PLL, demonstrating its use with a 38 MHz crystal. The two output clocks are shown at OUT0 (the low jitter 622 MHz clock) and OUT1 (the phase-programmable auxiliary clock). Edge skew (or time delay) in the auxiliary clock is accomplished by programming a phase offset into the DDS, which will change the relative point in time for the complementary input crossing at the comparator.

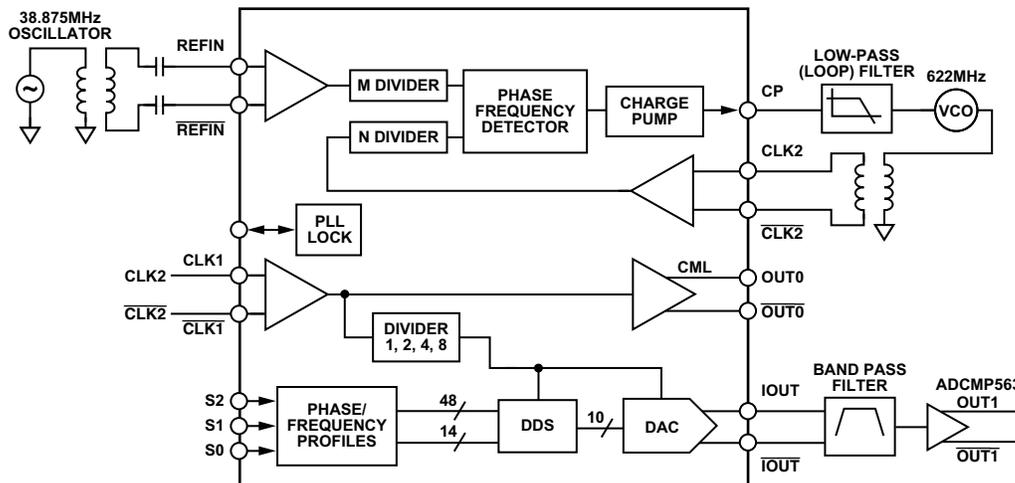


Figure 2. AD9540 Configured for Dual Clock Generation