

Sample-and-Hold Circuit Using the **ADG1211** Switch

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 is a sample-and-hold amplifier (SHA) function, which is basic to the data acquisition and analog-to-digital conversion process. In some programmable logic controller (PLC) output modules, a sample-and-hold circuit in each channel stores the output samples from a single high performance digital-to-analog converter (DAC). The sample-and-holds amplifier are often implemented using analog switches or multiplexers and buffers. The circuit shown in Figure 1 provides a precise, fast sample-and-hold circuit capable of processing industrial level signals of up to ± 10 V.

Switches and multiplexers are useful in data acquisition applications where instantaneous analog values must be captured. The input signal from the analog switch charges a hold capacitor that is connected to the input of an op amp. Ideally, the closed switch conveys nothing but the input signal to the capacitor. However, the switch also delivers a packet of charge when it switches, called charge injection. The **ADG1211** quad, single pole, single throw (SPST) switch has excellent charge injection performance of only 1 pC compared to typical solutions, which have 10 pC to 20 pC of charge injection. The **ADG1211** also has low capacitance and leakage current, making it an ideal choice for this circuit.

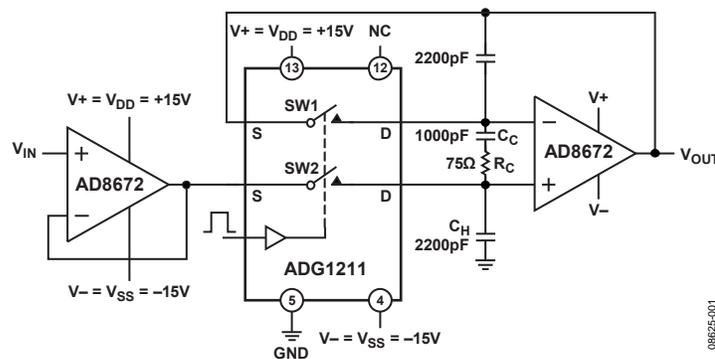


Figure 1. High Precision, Fast Sample-and-Hold Circuit (Simplified Schematic: Decoupling and All Connections Not Shown)

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REVISION HISTORY

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CIRCUIT DESCRIPTION

The circuit shown in Figure 1 is a precise, fast sample-and-hold circuit. During sample mode, SW2 is closed, and the output, V_{OUT} , follows the input signal, V_{IN} . In hold mode, SW2 is opened, and the signal is held by the hold capacitor, C_H .

Due to switch and capacitor leakage current, the voltage on the hold capacitor decays (droops) with time. The [ADG1211](#) minimizes this droop due to its low leakage specifications. The [ADG1211](#) has 20 pA leakage typically at 25°C and 100 pA maximum. The droop rate is further minimized by the use of a polystyrene hold capacitor.

A second switch, SW1, which operates in parallel with SW2, is included in this circuit to reduce pedestal error. Because both switches are at the same potential, they have similar transients, which act as a common-mode signal to the op amp, thereby minimizing charge injection effects. Pedestal error is also reduced by the compensation network, R_C and C_C . This compensation network also reduces the hold-time glitch and optimizes the acquisition time. The circuit in Figure 1 gives the following results: droop rate of 2 mV/ms, pedestal error of less than 0.5 mV, and acquisition time of 3 ms.

The circuit must be constructed on a multilayer printed circuit board with a large area ground plane. Proper layout, grounding, and decoupling techniques must be used to achieve optimum performance (see the [MT-031 Tutorial](#), [MT-088 Tutorial](#), [MT-090 Tutorial](#), and [MT-101 Tutorial](#)).