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Interfacing the ADL5373 I/Q Modulator to the AD9779A Dual Channel, 1 GSPS High Speed DAC

CIRCUIT FUNCTION AND BENEFITS

This circuit provides a simple, elegant interface between the ADL5373 I/Q modulator and the AD9779A high speed digital-to-analog converter (DAC). The ADL5373 and the AD9779A are well-matched devices because they have the same bias levels and similarly high signal-to-noise ratios (SNR). The matched bias levels of 500 mV allow for a glueless interface: there is no requirement for a level shifting network that adds noise and insertion loss along with extra components. The addition of the swing limiting resistors (RSLI, RSLQ) allows the DAC swing to be scaled appropriately without loss of resolution or of the 0.5 V bias level. The high SNR of each device preserves a high SNR through the circuit.
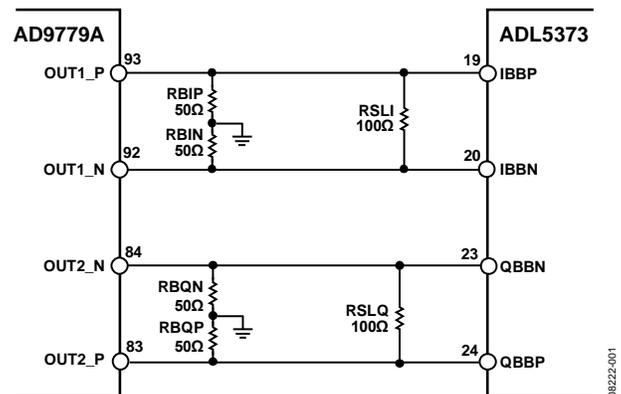

Figure 1. Interface Between the AD9779A and ADL5373 with 50 Ω Resistors to Ground to Establish the 500 mV DC Bias for the ADL5373 Baseband Inputs (Simplified Schematic)

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REVISION HISTORY

11/16—Rev. A to Rev. B
Changed Name from CN-0019 to AN-1423...................Universal

5/09—Rev. 0 to Rev. A
Updated Format..Universal

10/08—Revision 0: Initial Version

CIRCUIT DESCRIPTION

The ADL5373 is designed to interface with minimal components to members of Analog Devices family of TxDAC® converters. The baseband inputs of the ADL5373 require a dc common-mode bias voltage of 500 mV. With each AD9779A output swinging from 0 mA to 20 mA, a single 50 Ω resistor to ground from each of the DAC outputs provides the desired 500 mV dc bias. With just the four 50 Ω resistors in place, the voltage swing on each pin is 1 V p-p. This results in a differential voltage swing of 2 V p-p on each input pair.

By adding RSLI and RSLQ resistors to the interface, the output swing of the DAC can be reduced without any loss of DAC resolution. The resistor is placed as a shunt between each side of the differential pair, as shown in Figure 1, which reduces the ac swing without changing the dc bias already established by the 50 Ω resistors and the DAC output current.

The value of this ac swing limiting resistor is chosen based on the desired ac voltage swing. Figure 2 shows the relationship between the swing limiting resistor and the peak-to-peak ac swing that it produces when 50 Ω bias setting resistors are used. Note that all Analog Devices I/Q modulators present a relatively high input impedance on their baseband inputs (typically >1 kΩ), which results in the input impedance of the I/Q modulator having no effect on the scaling of the DAC output signal.
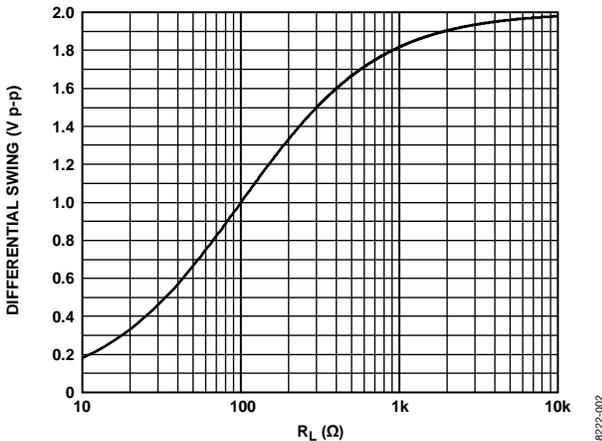
Figure 2. Relationship Between the AC Swing Limiting Resistor and the Peak-to-Peak Voltage Swing with 50 Ω Bias Setting Resistors

It is generally necessary to low-pass filter the DAC outputs to remove image frequencies when driving a modulator. The ADL5373 interface lends itself well to the introduction of such a filter. The filter can be inserted between the dc bias setting resistors and the ac swing limiting resistor. Doing so establishes the input and output impedances for the filter.

A simulated filter example is shown in Figure 3 with a third-order elliptical filter with a 3 dB frequency of 10 MHz. Matching input and output impedances makes the filter design easier, so the shunt resistor chosen is 100 Ω, producing an ac swing of 1 V p-p differential for a 0 mA to 20 mA DAC full-scale output current.
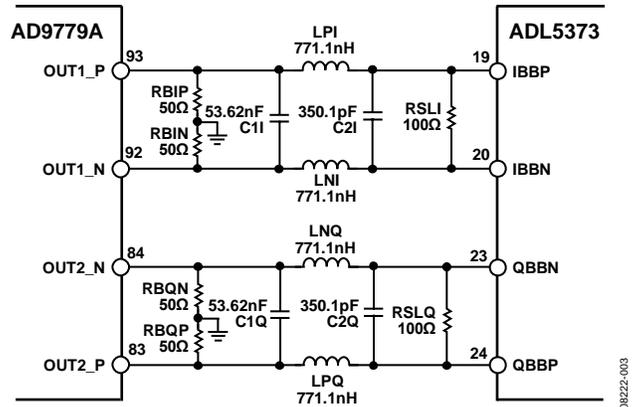
Figure 3. DAC Modulator Interface with 3 MHz Third-Order, Low-Pass Filter (Calculated Component Values)

The simulated frequency response of this filter is shown in Figure 4. In a practical application, the use of standard value components along with the input impedance of the I/Q modulator (2900 kΩ in parallel with a few picofarads of input capacitance), slightly changes the frequency response.
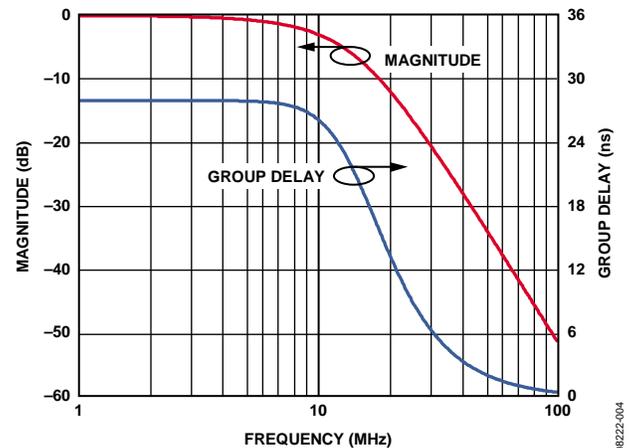
Figure 4. Simulated Frequency Response for DAC Modulator Interface with 10 MHz Third-Order Bessel Filter

All the power supply pins of the ADL5373 must be connected to the same 5 V source. Adjacent pins of the same name can be tied together and decoupled to a large area ground plane with a 0.1 μF capacitor. These capacitors must be located as close as possible to the device. The power supply can range between 4.75 V and 5.25 V.

The COM1 pin, COM2 pin, COM3 pin, and COM4 pin must be tied to the same ground plane through low impedance paths. The exposed paddle on the underside of the package must also be soldered to a low thermal and electrical impedance ground plane. If the ground plane spans multiple layers on the circuit board, the layers must be stitched together with nine vias under the exposed paddle. See the AN-772 Application Note for more detail.

COMMON VARIATIONS

The interface described in this application note can be used to interface any TxDAC® converter with ground referenced 0 mA to 20 mA output currents to any I/Q modulator with a 0.5 V input bias level. For zero-IF applications, the AD9783 dual DAC provides a low voltage differential signaling (LVDS) interface, while the complementary metal-oxide semiconductor (CMOS) driven AD9788 dual DAC can generate a fine resolution complex IF input to the I/Q modulator. The ADL5370/ADL5371/ADL5372/ADL5373 family of I/Q modulators provides narrow-band operation with high output 1 dB compression point and OIP3, whereas the ADL5375 provides broadband high performance operation from 400 MHz to 6GHz. The ADL5385 I/Q modulator uses a 2 × LO and operates from 50 MHz to 2.2 GHz.

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