

Impact of Adding a Neutral Attenuation Network in a 3P4W Wye System

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INTRODUCTION

In a 3-phase 4-wire (3P4W) wye configuration, there are three phase wires and one neutral wire. Each phase voltage is measured with respect to the neutral. The phase voltages are typically 220 V rms or 110 V rms in magnitude. Each phase voltage is 120° phase-shifted with respect to the other phase voltages. A common practice is to use attenuation networks on each of the 3-phase wires to step down the 220 V/110 V signals into signals small enough to enter the ADExxxx metering IC. (ADExxxx refers to Analog Devices, Inc., 3-phase AFEs such as the [ADE7854](#), [ADE7858](#), [ADE7868](#), [ADE7878](#), [ADE7854A](#), [ADE7858A](#),

[ADE7868A](#), [ADE7878A](#), [ADE7880](#), [ADE7758](#), [ADE7754](#), [ADE7762](#), and [ADE7752A](#).) The neutral wire is typically used as the ground reference for the ADExxxx IC. Figure 1 shows the typical 3P4W wye configuration voltage attenuation network setup.

However, in certain cases, the neutral cannot be treated as the ground reference. In such situations, an attenuation network is added to the neutral, thus forming a large resistance between neutral and ADExxxx ground, as shown in Figure 3. This application note analyses the performance impact of adding a neutral attenuation network in a 3P4W wye system.

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REVISION HISTORY

10/14—Revision 0: Initial Version

DESCRIPTION OF THE ISSUE

Figure 1 shows the standard 3P4W wye configuration setup. For simplicity, only the voltage channel connection is shown. There are attenuation networks connected to all three phase wires, and the neutral is considered to be the ground of the ADExxxx IC.

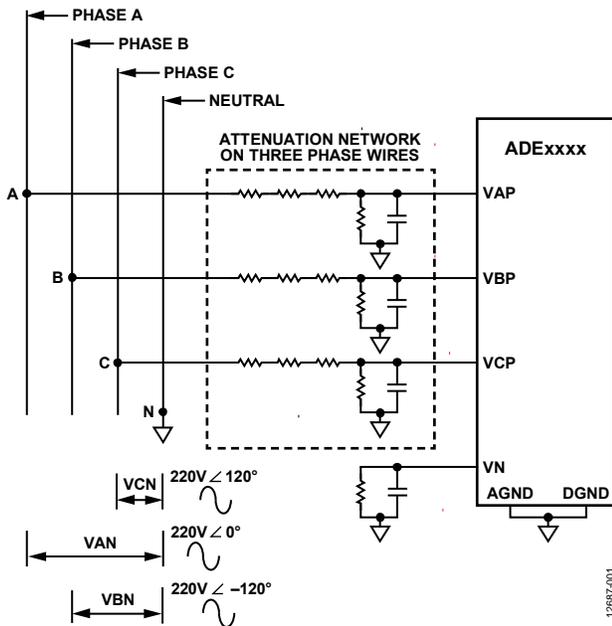


Figure 1. Standard 3P4W Wye Configuration Voltage Connection

In certain cases, the neutral cannot be treated as the ground reference. There can be multiple reasons for this requirement. Two of the main reasons are as follows:

1. Certain meters undergo a safety test during which one of the phase wires is swapped with the neutral. If Phase A is swapped with neutral, in Figure 1, the system ground reference is now 220 V. The system components, such as the power supply unit, are often not capable of handling this situation. Therefore, treating neutral as the ground reference is not a suitable option.
2. The communication module in a metering system is isolated from the high voltages for safety purposes. There are different types of isolation requirements based on application, meter design, standards, and so on. If only one level of functional isolation is required, it can be achieved by isolating the ground of the system from neutral alone. It is assumed that current sensors with isolation (such as current transformers) are used in the system. Figure 2 shows a typical metering system. The power supply is also isolated from neutral, in this case. There are also cases where two levels of isolation are required in the system: safety (galvanic) isolation and functional isolation. The safety isolation is typically achieved by implementing a sufficient amount of data and power isolation between the MCU and communication module. The functional isolation is achieved by separating neutral from the ground of the MCU.

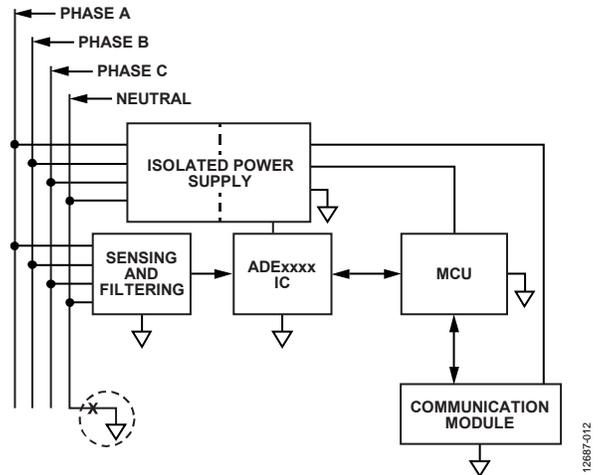


Figure 2. 3P4W Metering System Isolation Requirement

If these limitations cannot be overcome by means of any system level changes, the meter designers typically install an attenuation network on the neutral wire as well, which keeps the ground of the system at a different potential than the neutral wire.

The attenuation network resistors on the neutral wire create a large resistance between the neutral and the ground of the ADExxxx IC. This resistance is referred to as the neutral series resistance. Figure 3 shows the voltage connection in the system with the addition of neutral series resistance.

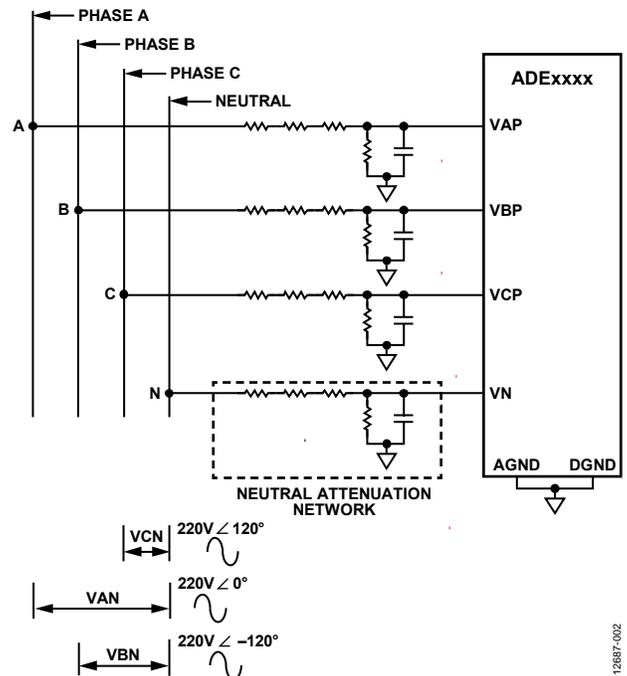


Figure 3. 3P4W Wye Configuration Voltage Connection with Attenuation Network on Neutral

Another common alternative to remain isolated from the high voltages is the use of voltage transformers; however, voltage transformers are less preferable because they make the meter design expensive and large.

VOLTAGE CHANNEL ADCs

Voltage signals are typically single-ended signals in metering applications. Therefore, the three voltage channel analog-to-digital converters (ADCs) within an ADExxxx IC have a common input terminal (the VN pin), as shown in Figure 4.

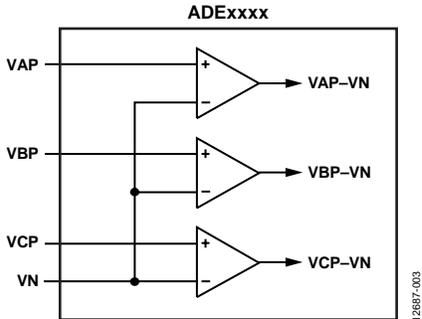


Figure 4. Voltage Channel ADC Configuration in 3-Phase ADExxxx IC

In Figure 4, VAP, VBP, VCP, and VN represent the ADExxxx IC input pins. The VAP, VBP, and VCP pins accept the stepped-down voltage signals from the phase wires, as shown in Figure 5 and Figure 6. The AGND and DGND pins of the ADExxxx IC, shown in Figure 5 and Figure 6, are tied to the ground potential of the system. If neutral is connected to ground, the VN pin of the ADExxxx IC also stays at that potential, as shown in Figure 5. If neutral is connected to an attenuation network, the stepped-down version of the neutral signal is available at the VN pin, as shown in Figure 6.

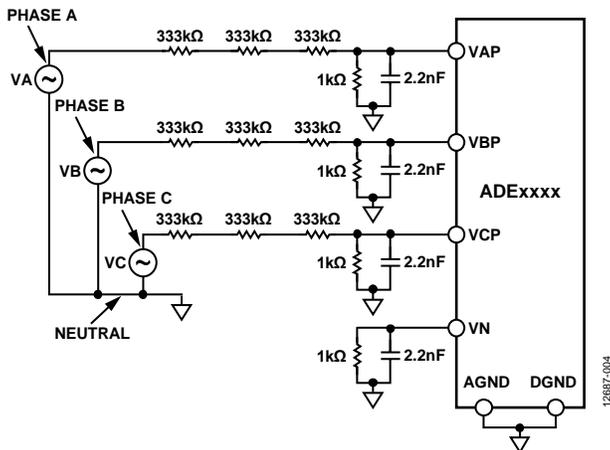


Figure 5. 3P4W Wye System: Neutral Connected to Ground

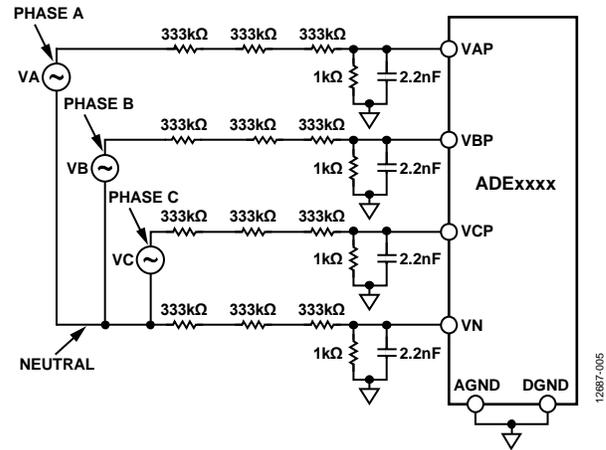


Figure 6. 3P4W Wye System: Neutral Series Resistance

To obtain valid results from the ADExxxx IC, it is important to understand the signal limitations at its input pins. The conditions to be met, with respect to the input voltage pins, are as follows:

1. The ac potential difference between VAP/VBP/VCP and VN must be no greater than ± 500 mV peak (353.55 mV rms).
2. The ac potential difference between VAP/VBP/VCP and AGND must be no greater than ± 500 mV peak (353.55 mV rms).
3. Similarly, the ac potential difference between VN and AGND must be no greater than ± 500 mV peak (353.55 mV rms). Although VN can be as large as ± 500 mV peak (353.55 mV rms) with respect to AGND, it is desirable to keep VN equal to AGND, because VN is common to all three voltage channel ADCs (see Figure 4).

The third condition in the previous list is the most relevant condition with respect to the use of neutral series resistance in a 3P4W system. In a configuration like the one shown in Figure 5, VN and AGND are at the same potential. However, when a neutral series resistance exists in the system, as shown in Figure 6, VN is not always equal to AGND. Any imbalance in the phase voltages causes the VN – AGND potential difference to be nonzero, thus leading to measurement errors.

SIMULATION TEST BENCH

To understand the impact of having a series resistance on the neutral, a simulation test bench was set up using the ADIsimPE software. The simulation test bench, corresponding to Figure 5, was set up as shown in Figure 7. The input impedance at the voltage channel input pins of the ADExxxx IC was also taken into consideration, as shown by the use of components R9 to R12 and C5 to C8. The ADE7880 IC is taken as an example, and its minimum input impedance is used for all simulations. VA, VB, and VC in Figure 7 are the Phase A, Phase B, and

Phase C voltages, respectively. The voltage input pins of the ADExxxx IC, VAP, VBP, VCP, and VN, are denoted as VAP_pin, VBP_pin, VCP_pin, and VN_pin, respectively. The ground of the ADExxxx IC is denoted as AGND_pin. The scopes that measure the VAP – VN, VBP – VN, and VCP – VN potential differences are denoted as VAN, VBN, and VCN, respectively. The VAG, VBG, VCG, and VNG scopes measure the voltage signals on the VAP, VBP, VCP, and VN pins, respectively, with respect to ground.

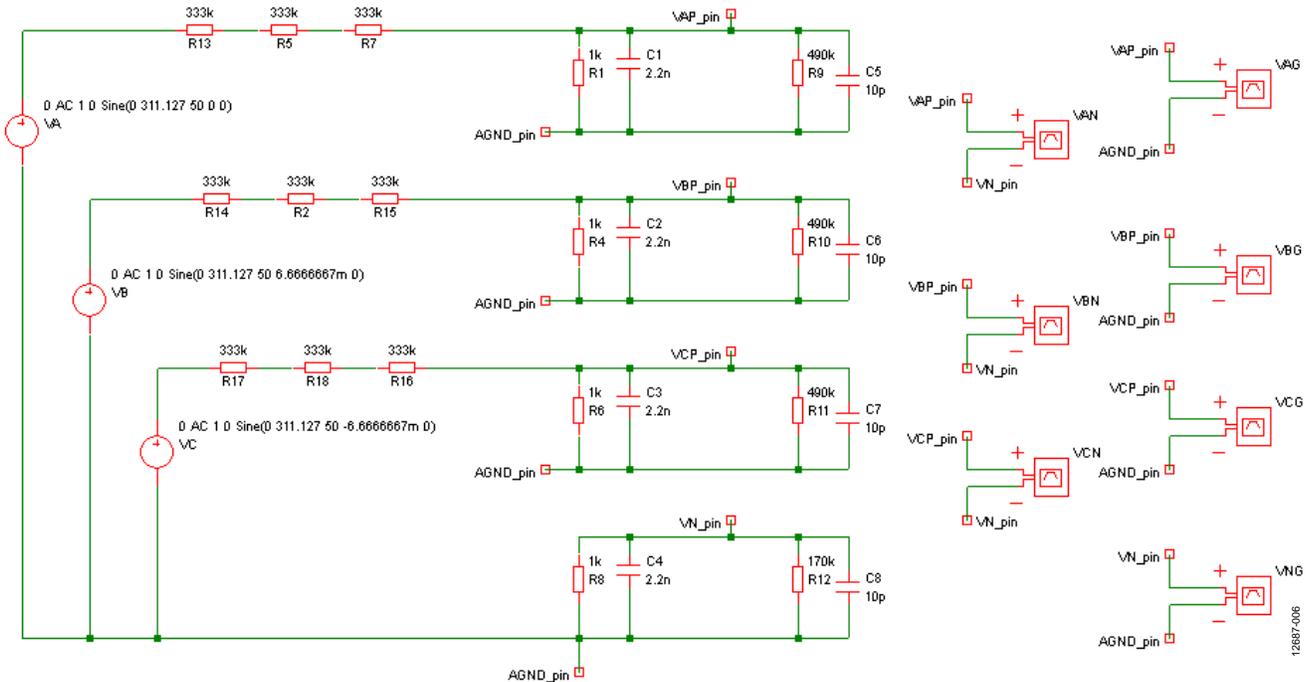


Figure 7. Simulation Test Bench: Standard 3P4W Wye Setup

VOLTAGE MAGNITUDE IMBALANCE

All three phase voltages, VA, VB, and VC, typically have the same magnitude and are exactly 120° phase-shifted with respect to each other (see Figure 8). In such a situation, the voltages are said to be balanced, and their vector sum is equal to zero. However, in reality, the loads are not balanced perfectly, thus causing imbalance in the phase voltages. The voltage imbalance can be due to difference in magnitude or phase or both. Voltage magnitude imbalance occurs when the magnitude of the three phase voltages are not equal to each other. Voltage phase imbalance occurs when the phase voltages are not exactly 120° phase-shifted with respect to each other. In this application note, only voltage magnitude imbalance is considered.

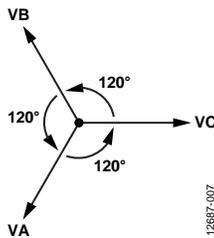


Figure 8. Phasor Diagram Showing Three Phase Voltages

There are several definitions available for voltage imbalance. For the purposes of this application note, two terms are defined: % magnitude imbalance and total magnitude imbalance.

The % magnitude imbalance is defined as the absolute maximum deviation from the average rms voltage as a percentage of the average rms voltage.

$$\% \text{ Magnitude Imbalance} = \frac{\text{Max} \left\{ |V_{MAX} - V_{AVG}|, |V_{MIN} - V_{AVG}| \right\}}{V_{AVG}} \times 100\%$$

where:

V_{MAX} is the maximum magnitude of the three phase voltage rms values VA, VB, and VC.

V_{MIN} is the minimum magnitude of the three phase voltage rms values VA, VB and VC.

V_{AVG} is the average magnitude of the three phase voltage rms values VA, VB and VC.

The total magnitude imbalance is defined as the sum of all absolute deviations from the average rms voltage, in volts.

$$\text{Total Magnitude Imbalance} = |VA - V_{AVG}| + |VB - V_{AVG}| + |VC - V_{AVG}| \text{ V}$$

For example, if $|VA| = 220 \text{ V}$, $|VB| = 165 \text{ V}$, and $|VC| = 275 \text{ V}$, the % magnitude imbalance is calculated as follows:

$$\% \text{ Magnitude Imbalance} = \frac{\text{Max} \left\{ |275 - 220|, |165 - 220| \right\}}{220} \times 100\%$$

$$\% \text{ Magnitude Imbalance} = (55/220) \times 100\%$$

$$\% \text{ Magnitude Imbalance} = 25\%$$

The total magnitude imbalance is calculated as follows:

$$\text{Total Magnitude Imbalance} = |220 - 220| + |165 - 220| + |275 - 220| \text{ V}$$

$$\text{Total Magnitude Imbalance} = 55 + 55 \text{ V}$$

$$\text{Total Magnitude Imbalance} = 110 \text{ V}$$

These two quantities are used hereafter in this application note when referring to the amount of voltage magnitude imbalance in the system.

STANDARD 3P4W CONFIGURATION

The standard 3P4W voltage channel configuration shown in Figure 5 was simulated, and the amplitude and phase of the voltage signals at the VAP, VBP, VCP, and VN pins were measured with respect to AGND. The amplitude and phase of the VAP, VBP, and VCP signals with respect to VN were also noted.

Each of the attenuation networks on the 3-phase wires is comprised of three 333 kΩ resistors and one 1 kΩ resistor. This arrangement, as shown in Figure 5, provides 1000:1 attenuation to the phase voltages. The three phase voltages provided were

$$|VA| = 220 \text{ V}; \angle VA = 0^\circ$$

$$|VB| = 220 \text{ V}; \angle VB = -120^\circ$$

$$|VC| = 220 \text{ V}; \angle VC = +120^\circ$$

These phase voltages are equal in magnitude and are 120° phase-shifted from the other voltages, which shows that the system is balanced. The common node of the three voltage sources VA, VB, and VC in Figure 5 represents the neutral wire in the 3P4W system.

The voltage signals at the input pins of the ADExxxx IC were

$$|VAP - VN| = 214.6 \text{ mV rms}; \angle(VAP - VN) = 0^\circ$$

$$|VBP - VN| = 214.6 \text{ mV rms}; \angle(VBP - VN) = -120^\circ$$

$$|VCP - VN| = 214.6 \text{ mV rms}; \angle(VCP - VN) = +120^\circ$$

The signals at the input pins with respect to AGND potential were

$$|VAP - AGND| = 214.6 \text{ mV rms}; \angle(VAP - AGND) = 0^\circ$$

$$|VBP - AGND| = 214.6 \text{ mV rms}; \angle(VBP - AGND) = -120^\circ$$

$$|VCP - AGND| = 214.6 \text{ mV rms}; \angle(VCP - AGND) = +120^\circ$$

$$|VN - AGND| = 0 \text{ V}; \angle(VN - AGND) = 0^\circ$$

3P4W CONFIGURATION WITH NEUTRAL SERIES RESISTANCE

The simulation test bench was modified to include the attenuation network on the neutral wire of the system, as shown in Figure 6.

The same balanced phase voltage inputs provided for the standard 3P4W case were provided for this setup as well. The observed voltage signals, VAP, VBP, and VCP with respect to VN and VAP, VBP, VCP, and VN with respect to AGND, were the same as the standard 3P4W case. This result shows that the addition of the neutral series resistance has no notable impact on the system performance when the system is balanced. To understand the impact of neutral series resistance in an unbalanced system, the following conditions were simulated:

1. Phase B and Phase C disconnected (floating)
2. Phase B and Phase C tied to neutral
3. $|V_A| = 220 \text{ V}$, $|V_B| = 240 \text{ V}$, $|V_C| = 240 \text{ V}$
4. $|V_A| = 220 \text{ V}$, $|V_B| = 20 \text{ V}$, $|V_C| = 20 \text{ V}$

Case 1: Phase B and Phase C Disconnected

When Phase B and Phase C were disconnected or floating, the simulation test bench was similar to the one shown in Figure 9.

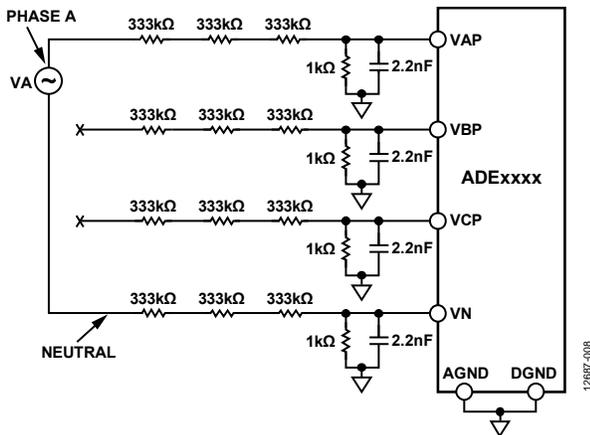


Figure 9. Phase B and Phase C Disconnected, Case 1

The voltage signal applied on Phase A was

$$|V_A| = 220 \text{ V}; \angle V_A = 0^\circ$$

The voltage signals at the input pins of the ADExxxx IC were

$$|V_{AP} - V_N| = 214.2 \text{ mV rms}; \angle(V_{AP} - V_N) = 0^\circ$$

$$|V_{BP} - V_N| = 106.9 \text{ mV rms}; \angle(V_{BP} - V_N) = 0^\circ$$

$$|V_{CP} - V_N| = 106.9 \text{ mV rms}; \angle(V_{CP} - V_N) = 0^\circ$$

The signals at the input pins with respect to AGND potential were

$$|V_{AP} - \text{AGND}| = 107.3 \text{ mV rms}; \angle(V_{AP} - \text{AGND}) = 0^\circ$$

$$|V_{BP} - \text{AGND}| = 0 \text{ V}; \angle(V_{BP} - \text{AGND}) = 0^\circ$$

$$|V_{CP} - \text{AGND}| = 0 \text{ V}; \angle(V_{CP} - \text{AGND}) = 0^\circ$$

$$|V_N - \text{AGND}| = 107.3 \text{ mV rms}; \angle(V_N - \text{AGND}) = 180^\circ$$

These results mean that the ADExxxx IC measures the voltage signals to be

- Phase A voltage: 219.6 V, $\angle 0^\circ$ (-0.2% gain error)
- Phase B voltage: 109.8 V, $\angle 0^\circ$ (expected: 0 V)
- Phase C voltage: 109.8 V, $\angle 0^\circ$ (expected: 0 V)

When only the Phase A voltage exists, the voltages present on the VAP and VN pins are differential, antiphase signals. Because of the configuration, a -0.2% gain error is observed in the Phase A voltage measurement. Because the VN pin is common to all phase voltages, the signal on the VN pin affects the Phase B and Phase C voltage measurements of the ADExxxx IC. In this case, VN is not equal to AGND, due to which the signal present on the VN pin is phase-shifted by 180° and appears on the Phase B and Phase C voltage measurements. In this case, the Phase B and Phase C voltages computed by the ADExxxx IC contain large errors because the signal on the VN pin consists of half of the voltage signal of Phase A.

To avoid getting invalid results on disconnected phases, monitor the phase angle of the voltages every time a measurement is taken to ensure that all the phase voltages are 120° phase-shifted with respect to each other. In this case, the Phase B and Phase C voltage signals were in-phase with the Phase A voltage signal, therefore indicating that the voltage related measurements from Phase B and Phase C must be discarded.

Case 2: Phase B and Phase C Tied to Neutral

When only Phase A was present, as shown in Case 1: Phase B and Phase C Disconnected, and Phase B and Phase C were tied to neutral instead of floating, most of the error observed in the measurements of Phase B and Phase C were eliminated. Figure 10 shows the setup diagram.

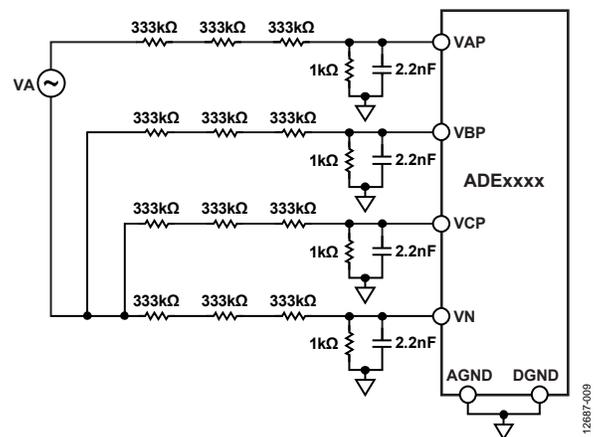


Figure 10. Phase B and Phase C Tied to Neutral, Case 2

The voltage signal applied on Phase A was

$$|V_A| = 220 \text{ V}; \angle V_A = 0^\circ$$

The voltage signals at the input pins of the ADExxxx IC were

$$|V_{AP} - V_N| = 214.3 \text{ mV rms}; \angle(V_{AP} - V_N) = 0^\circ$$

$$|V_{BP} - V_N| = 0.21 \text{ mV rms}; \angle(V_{BP} - V_N) = 180^\circ$$

$$|V_{CP} - V_N| = 0.21 \text{ mV rms}; \angle(V_{CP} - V_N) = 180^\circ$$

The signals at the input pins with respect to AGND potential were

$$|VAP - AGND| = 160.9 \text{ mV rms}; \angle(VAP - AGND) = 0^\circ$$

$$|VBP - AGND| = 53.6 \text{ mV rms}; \angle(VBP - AGND) = 180^\circ$$

$$|VCP - AGND| = 53.6 \text{ mV rms}; \angle(VCP - AGND) = 180^\circ$$

$$|VN - AGND| = 53.4 \text{ mV rms}; \angle(VN - AGND) = 180^\circ$$

These results mean that the ADExxxx IC measures the voltage signals to be

- Phase A voltage: 219.8 V, $\angle 0^\circ$ (–0.1% gain error)
- Phase B voltage: 0.22 V, $\angle 180^\circ$ (expected: 0 V)
- Phase C voltage: 0.22 V, $\angle 180^\circ$ (expected: 0 V)

Because the signals on Phase B, Phase C, and neutral have similar signal path in this configuration, the Phase B and Phase C voltage signals at the input pins of the ADExxxx IC were observed to be closer to reality. Instead of observing half of the Phase A voltage signal on Phase B and Phase C, like in the previous case, the Phase B and Phase C voltage measurements in this configuration represented a very small signal, that is, $\sim(VAP - VN)/1000$. The voltage signals on Phase B and Phase C were 180° out of phase with the Phase A voltage. Because the Phase B and C voltages are not 120° phase-shifted in comparison to the Phase A voltage, the phase angle of the Phase B and Phase C voltages can be used to indicate that these phase voltages have been tied to neutral, in the application. The gain error in the Phase A measurement was –0.1% in this case.

Case 3: $|VA| = 220 \text{ V}$, $|VB| = 240 \text{ V}$, $|VC| = 240 \text{ V}$

In Case 3, instead of removing the phase voltages completely, voltage magnitude imbalance was simulated by applying voltage signals of different amplitudes to VB and VC compared to VA. In this case, the applied voltage signals were

$$|VA| = 220 \text{ V}; \angle VA = 0^\circ$$

$$|VB| = 240 \text{ V}; \angle VB = -120^\circ$$

$$|VC| = 240 \text{ V}; \angle VC = +120^\circ$$

This condition represents a 9% voltage magnitude imbalance with a total magnitude imbalance of 40 V. The simulation test bench was set up based on the configuration shown in Figure 6.

The voltage signals at the input pins of the ADExxxx IC were

$$|VAP - VN| = 214.6 \text{ mV rms}; \angle(VAP - VN) = 0^\circ$$

$$|VBP - VN| = 234.1 \text{ mV rms}; \angle(VBP - VN) = -119.9^\circ$$

$$|VCP - VN| = 234.1 \text{ mV rms}; \angle(VCP - VN) = +120.1^\circ$$

The signals at the input pins with respect to AGND potential were

$$|VAP - AGND| = 219.5 \text{ mV rms}; \angle(VAP - AGND) = 0^\circ$$

$$|VBP - AGND| = 231.7 \text{ mV rms}; \angle(VBP - AGND) = -119^\circ$$

$$|VCP - AGND| = 231.7 \text{ mV rms}; \angle(VCP - AGND) = +121^\circ$$

$$|VN - AGND| = 4.86 \text{ mV rms}; \angle(VN - AGND) = -118^\circ$$

These results mean that the ADExxxx IC measures the voltage signals to be

- Phase A voltage: 220 V, $\angle 0^\circ$ (no error)
- Phase B voltage: 240 V, $\angle -119.9^\circ$ (+0.1° phase error)
- Phase C voltage: 240 V, $\angle +120.1^\circ$ (+0.1° phase error)

When an imbalance such as this was simulated, no notable gain error was observed on the Phase A, Phase B, and Phase C measurements; however, a minor phase error of 0.1° was observed in the Phase B and Phase C voltages.

Case 4: $|VA| = 220 \text{ V}$, $|VB| = 20 \text{ V}$, $|VC| = 20 \text{ V}$

In Case 4, a larger voltage magnitude imbalance was considered.

The applied voltage signals were

$$|VA| = 220 \text{ V}; \angle VA = 0^\circ$$

$$|VB| = 20 \text{ V}; \angle VB = -120^\circ$$

$$|VC| = 20 \text{ V}; \angle VC = +120^\circ$$

In this case, a 91% voltage magnitude imbalance was considered with a total magnitude imbalance of 400 V. Although this amount of imbalance is impractical, this case was simulated to understand the impact of a large voltage magnitude imbalance in the system. The simulation test bench was set up based on the configuration shown in Figure 6.

The voltage signals at the input pins of the ADExxxx IC were

$$|VAP - VN| = 214.4 \text{ mV rms}; \angle(VAP - VN) = 0^\circ$$

$$|VBP - VN| = 19.6 \text{ mV rms}; \angle(VBP - VN) = -120.6^\circ$$

$$|VCP - VN| = 19.6 \text{ mV rms}; \angle(VCP - VN) = +120.6^\circ$$

The signals at the input pins with respect to AGND potential were

$$|VAP - AGND| = 165.8 \text{ mV rms}; \angle(VAP - AGND) = 0^\circ$$

$$|VBP - AGND| = 60.9 \text{ mV rms}; \angle(VBP - AGND) = -164^\circ$$

$$|VCP - AGND| = 60.9 \text{ mV rms}; \angle(VCP - AGND) = +164^\circ$$

$$|VN - AGND| = 48.6 \text{ mV rms}; \angle(VN - AGND) = 180^\circ$$

These results mean that the ADExxxx IC measures the voltage signals to be

- Phase A voltage: 219.8 V, $\angle 0^\circ$ (–0.1% gain error)
- Phase B voltage: 20.1 V, $\angle -120.6^\circ$ (+0.5% gain error; –0.6° phase error)
- Phase C voltage: 20.1 V, $\angle +120.6^\circ$ (+0.5% gain error; +0.6° phase error)

When a large voltage magnitude imbalance such as this existed in the system, the gain error observed on the Phase B and Phase C voltages due to the configuration was 0.5%. These measurements also had a phase error of 0.6° . The Phase A voltage measurement had a gain error of –0.1%.

LAB TESTS

To verify the simulation results and to understand the impact of real components, lab tests were conducted using the ADE7880, a poly phase energy metering IC.

The ADE7880 evaluation board and a 3-phase Rotek accurate source were used to conduct the lab tests. Refer to the ADE7880 evaluation board user guide, UG-356, for details on the ADE7880 evaluation board. To introduce the neutral series resistance in the configuration, the following changes were made (see Figure 11):

- The 1 kΩ resistor, R25 in Figure 11, was removed and soldered on top of C25 on the evaluation board.
- In the place of the 1 kΩ R25 resistor, a 1 MΩ resistor was soldered.

The jumper status on the voltage channel connections of the ADE7880 evaluation board were

- JP7A, JP7B, JP7C, JP7N = open
- JP9A, JP9B, JP9C = closed
- JP8A, JP8B, JP8C = Pin 1 and Pin 2

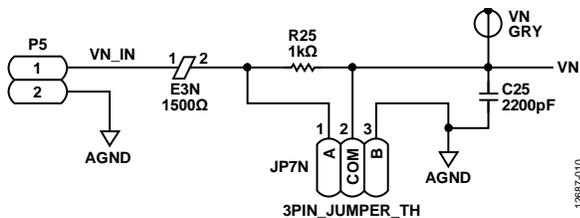


Figure 11. Neutral Voltage Connection, ADE7880 Evaluation Board

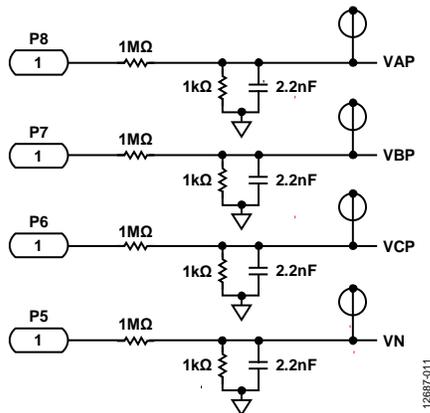


Figure 12. Final Representation of Voltage Channel Configuration

Pin 1 of the P8, P7, P6, and P5 connectors were connected to the Phase A, Phase B, Phase C, and neutral wires, respectively, as shown in Figure 12.

The voltage rms measurements from the ADE7880 IC were recorded in each case to quantify the gain error observed. Readings of 100 rms were recorded, and the results were averaged to acquire an rms value in each case.

The 1 MΩ and 1 kΩ resistors placed on the signal path of all phase and neutral wires were measured and found to be

- Phase A = 1.001 MΩ; 1.009 kΩ
- Phase B = 999 kΩ; 1.002 kΩ
- Phase C = 1.002 Ω; 0.997 kΩ
- Neutral = 950 kΩ; 1.01 kΩ

All the simulation cases were repeated by replacing the three 333 kΩ resistors in the signal path of each wire (see Figure 6), with a single resistor on the signal path of each wire. Instead of using 1 MΩ and 1 kΩ resistors in the schematic, resistors with the measured values were used. The use of actual resistor values is essential because the mismatch in the attenuation network ratios causes more error when voltage magnitude imbalance exists.

The lab and simulation test results are shown in Table 1. The balanced case measurements, with the neutral series resistance, were considered as the reference, to compute the gain errors in unbalanced cases.

The simulation and lab results match closely, as seen in Table 1. Observing the resistor values measured from the evaluation board, all the resistors were 1% tolerant resistors, except for the 1 MΩ resistor on the neutral wire (actually 950 kΩ), which was 5% tolerant. This resistor is the major part of neutral series resistance and is common to all phase voltage measurements. Therefore, the loose tolerance specification of this resistor adversely impacted the performance in all phases where voltage magnitude imbalance exists. If the 1 MΩ resistor of Phase A is 5% tolerant, whereas all other resistors are 1% tolerant, the impact due to the attenuation network mismatch is severe only on the Phase A results, when voltage magnitude imbalance exists.

Table 1. Lab and Simulation Results Comparison

Unbalanced Case	Gain Error in RMS Measurement					
	AVRMS		BVRMS		CVRMS	
	Lab	Simulation	Lab	Simulation	Lab	Simulation
Case 1: Phase B and Phase C Disconnected	+2.00%	+2.38%	N/A ¹	N/A ¹	N/A ¹	N/A ¹
Case 2: Phase B and Phase C Tied to Neutral	+0.96%	+1.21%	N/A ¹	N/A ¹	N/A ¹	N/A ¹
Case 3: VA = 220 V; VB = VC = 240 V	-0.10%	-0.14%	+0.15%	+0.04%	+0.15%	+0.25%
Case 4: VA = 220 V; VB = VC = 20 V	+1.17%	+1.12%	-7.37%	-5.17%	-9.61%	-5.42%

¹ N/A = not applicable. The expected Phase B and Phase C voltages are 0 V in Case 1 and Case 2. Therefore, error is not shown in this table. Refer to the sections on each individual case for details on erroneous Phase B and Phase C voltage signals in Case 1 and Case 2.

SIMULATION TEST: SPECIAL CASE

Because the simulation results closely matched the lab results, further simulations were conducted to better understand the errors observed in the 25% voltage magnitude imbalance condition. When a 25% voltage magnitude imbalance exists, with a total magnitude imbalance of 110 V, the gain and phase errors were simulated on three different scenarios, and the

results are provided in Table 2. Resistors with 1% tolerance were considered for these simulation cases. The resistors that formed the attenuation network were

- Phase A: Three 336.33 k Ω resistors and one 990 Ω resistor
- Phase B: Three 329.67 k Ω resistors and one 1.01 k Ω resistor
- Phase C: Three 333 k Ω resistors and one 1 k Ω resistor
- Neutral: Three 333 k Ω resistors and one 1 k Ω resistor

Table 2. Simulation Results: 25% Voltage Magnitude Imbalance with 1% Tolerant Resistors

Unbalanced Case	Phase A Voltage		Phase B Voltage		Phase C Voltage	
	Gain Error	Phase Error	Gain Error	Phase Error	Gain Error	Phase Error
$ V_A = 275 \text{ V}, V_B = 220 \text{ V}, V_C = 165 \text{ V}$	0.12%	0°	0.00%	-0.1°	0.03%	0°
$ V_A = 165 \text{ V}, V_B = 275 \text{ V}, V_C = 220 \text{ V}$	-0.14%	0°	-0.19%	-2.3°	0.00%	0°
$ V_A = 220 \text{ V}, V_B = 165 \text{ V}, V_C = 275 \text{ V}$	0.00%	0°	0.26%	0°	-0.02%	0°

CONCLUSION

The performance impact analysis of using a neutral series resistance in a 3P4W wye system, done with the help of simulation and lab test results, reveal the following:

1. When the phases are balanced, there is no performance degradation observed, in comparison to the standard 3P4W configuration (see Figure 5 for the standard configuration).
2. Calibrate the 3P4W wye meter setup by providing balanced test voltage signals on all phases, even when calibrating phases one by one.
3. When voltage magnitude imbalance exists, gain and phase errors may be observed, depending on the amount of imbalance and the attenuation network ratio mismatch.
4. When 25% voltage magnitude imbalance exists, a maximum gain error of 0.26% and a maximum phase error of -2.3° can be expected, while using 1% tolerant resistors. If a single voltage measurement has 0.26% gain error and -2.3° phase error, the active energy measurement has an error of 0.18% at PF of 1, -6.8% at PF of 0.5, and -20% at PF of 0.2.
5. Use resistors with tighter tolerance ratings for better performance in unbalanced conditions.
6. The errors provided in this application note, based on lab and simulation test results, do not take into account the performance degradation over temperature.
7. Voltage phase imbalance (a condition where the phase voltages are not exactly 120° phase-shifted with respect to each other) is not common. The impact of the neutral series resistance during such an imbalance is not considered in this application note.