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APPLICATION NOTE

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Enabling HDMI 2.0 Using ADV8005 and ADV7625/ADV7626/ADV7627

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INTRODUCTION

This application note outlines how to enable the new 4:2:0 feature of HDMI® 2.0 on the ADV8005 and ADV7625/ADV7626/ADV7627 series of parts. The implementation of the HDMI 4:2:0 feature allows receiving and transmitting ultra HD video with a 60 Hz refresh rate (4k × 2k at 60 Hz) using a 3 GHz bandwidth.

Prior to HDMI 2.0, digital video had been transmitted using a 4:4:4 or 4:2:2 format. The former could transmit either RGB or YCrCb without subsampling chroma. The latter can carry only chroma subsampled YCrCb data, which means that pixels contain only partial information about chroma. For more information, refer to the handbook on video demystification listed in the References section. The newly introduced 4:2:0 format reduces the chroma information for YCrCb even further than 4:2:2, but increases the luma bandwidth.

Table 1. Luma/Chroma Composition

Portion of Composition	4:4:4	4:2:2	4:2:0
Luma	33%	50%	66%
Chroma	66%	50%	33%

Transmitting ultra HD at 60 video frames per second in a 4:4:4 video format requires a bandwidth of 6 Gbps. In the 4:2:0 format, two luma samples are sent for one chroma sample. This reduces the number of video pixels sent per line of video. Transmitting ultra HD at 60 video frames per second in a 4:2:0 video format requires a bandwidth of only 3 Gbps.

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REVISION HISTORY

7/14—Revision 0: Initial Version

VSPS AND HDMI 2.0

The ADV8005 is a video signal processor (VSP) with serial and TTL video inputs that can deinterlace and scale input video. The ADV7625/ADV7626/ADV7627 parts are high performance HDMI transceiver parts with cross-point and splitter capabilities. The ADV8005 and ADV7625/ADV7626/ADV7627 series of products feature 3 Gbps HDMI transmitters (Tx).

All of these parts were originally designed to support HDMI specification 1.4; however, it is also possible to pass the 4:2:0 format of the HDMI specification 2.0 through these parts. It is not possible, however to perform color conversions in 4:2:0.

To enable the 4:2:0 functionality on these parts, two conditions must be met:

- 4:2:0 data must use a similar configuration to that used for 4:4:4 data.
- Appropriate InfoFrame content must be sent from the transmitters.

HDMI 2.0 only specifies use of the 4:2:0 format for video identification codes (VIC) 96, 97, 101, 102, 106, and 107 from CEA-861-F. These are all ultra HD formats with a 50 Hz or 60 Hz frame rate.

These settings depend on transmitter operation mode.

MODES OF TRANSMITTER OPERATIONS

There are two distinct modes of operation, pass through mode and non-pass through mode.

Pass Through Mode

The ADV7625 series of parts can operate in a pass through mode (known also as mux mode). In this mode, the transmitter is directly fed with a raw TMDS data stream from the HDMI receiver. In this case, the HDMI stream (TMDS stream) remains unaltered from the input to the output. Audio, video, and packet content is not reassembled in the transmitter.

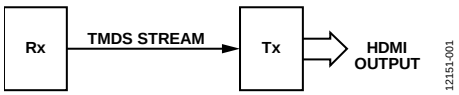

Figure 1. Block Diagram of Data Supplied to Tx in Pass Through Mode

This mode is enabled when data bypasses the CP core in the ADV7625.

In order to handle 4:2:0 mode, no additional configuration is required. The incoming 4:2:0 stream is passed straight to the output. All 4:2:0-relevant information received by the receiver remains unaltered and is output through the Tx into a downstream HDMI sink attached to the transmitter.

Non-Pass Through Mode

Non-pass through mode is enabled in the HDMI transmitter when the HDMI data stream is rebuilt, and InfoFrames are inserted. Normally, the pixel data is supplied through CP core which is capable of passing 4:2:0 stream using the standard 4:4:4 path.

One uses this mode

- when the ADV7625 is configured to enable CP core or perform audio insertion.
- for the ADV8005. The ADV8005 HDMI Tx receives video data from the TTL inputs or from the TMDS receiver.

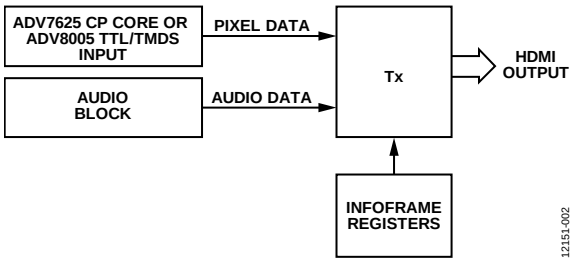

Figure 2. Block Diagram of Data Supplied to Tx in Non-Pass Through Mode

In non-pass through mode, the transmitter must be configured to embed auxilliary video information (AVI) InfoFrames that reflect the 4:2:0 stream.

SETTING AVI INFOFRAMES

The introduction of new video formats such as 3840 × 2160 P at 60 Hz (4k × 2k at 60 Hz) has led to an expansion of the video identification codes from 64 up to 128 in the AVI InfoFrame. The standard AVI InfoFrame in the ADV8005 and ADV7625/ ADV7626/ ADV7627 HDMI transmitters uses 6 bits to support the VIC. However, the flexible transmitter design allows users to enable a spare HDMI packet as the AVI InfoFrame and disable the standard AVI InfoFrame. This provides complete freedom in programming any of the fields in the AVI InfoFrame and enables the use of a 7-bit VIC.

Another important change in HDMI 2.0 is the addition of an extra bit, Y2, to set the color format in the AVI InfoFrame. The Y2, Y1, and Y0 values in the AVI InfoFrame are used to distinguish between YCrCb 4:2:2, YCrCb 4:4:4, RGB, and YCrCb 4:2:0. To enable 4:2:0 mode, the Y2,Y1, and Y0 values in the AVI InfoFrame must also be set correctly to 011, respectively, in binary format. It is unnecessary to send a vendor specific InfoFrame when transmitting 4:2:0 video format.

The ADV8005 and ADV7625/ADV7626/ADV7627 products have been tested and verified using 4k × 2k at 60 Hz 4:2:0 formatted video. The scripts used for the testing are included in this application note.

ADV7625/ADV8005 SCRIPT

Figure 3 shows the test setup used to evaluate the ADV8005 HDMI 4:2:0 functionality. A video generator is used as a source for the 4:2:0 format. The ADV7619 is used as a HDMI receiver and outputs the video to the ADV8005 digital pixel inputs.

The VSP processing is bypassed in the ADV8005 and the 4:2:0 data is routed directly to its HDMI Tx devices. The script details all of the I²C writes to the ADV7619 and to the ADV8005 for this test setup.

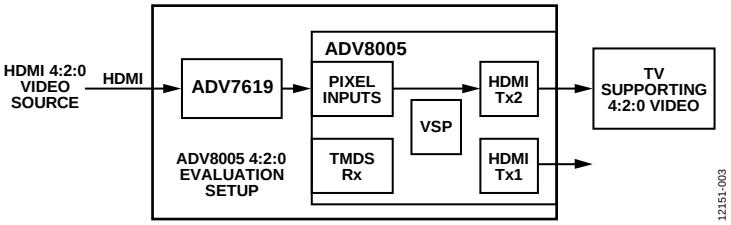

Figure 3. ADV8005 HDMI 4:2:0 Test Setup

SCRIPT 1 HDMI 4:2:0 VIDEO PROCESSING

```
//***********ADV7619 Writes***************
98 FF 80
98 F4 80
98 F5 7C
98 F8 4C
98 F9 64
98 FA 6C
98 FB 6A
98 FD 44
50 20 00
6A C0 03
98 01 06
98 02 F2
98 03 54
98 05 28
98 06 A0
98 0C 42
98 15 80
98 19 83
98 33 40
98 DD A0
4C B5 01
4C C3 80
4C CF 03
6A 3E 69
6A 3F 46
6A 4E 7E
6A 4F 42
6A 02 03
6A 57 A3
6A 58 07
6A 83 FC
6A 84 03
6A 85 10
6A 86 9B
6A 89 03
6A 9B 03
```

```
//********** ADV8005 Initialization ****************
1A 1A5B 42
1A 1A5F 00
1A 1A61 06
1A 1AA0 13
1A 1AA1 01
1A 1AA2 25
1A 1AA3 1D
1A 1AA4 81
1A 1AA5 81
1A 1AA7 10
1A 1AA8 B4
1A 1AFE 08
1A E0C0 C4
1A E889 03
1A E88A 46
1A E88B 7A
1A E88C 00
1A E600 03
1A E601 C5
1A E602 0A
1A E603 00
1A E604 03
1A E605 D8
1A E606 06
1A E607 00
1A E608 03
1A E609 EB
1A E60A 02
1A E60B 00
1A E60C 03
1A E60D FD
1A E60E FE
1A E60F 00
1A E664 04
1A E665 10
1A E666 FA
1A E667 00
1A E668 04
1A E669 23
1A E66A F6
1A E66B 00
1A E66C 04
1A E66D 36
1A E66E F2
1A E66F 00
1A 1A45 00
```

```
1A 1A46 A8
1A 1A47 00
1A 1A48 FB
1A 1A4E 08
1A 1A4F 08
1A E93B 40
1A E949 F0
1A 1A44 88
1A 1A39 0A
1A E662 81
1A 1A9D FF
1A 1A9E 55
1A 1BC8 FF
1A 1BC9 FF
1A 1BCA FF
1A 1BCB FF
1A 1BCC FF
1A 1BCD FF
1A 1BCE FF
1A 1BCF FF
1A 1BD0 FF
1A 1BD1 FF
1A 1BD2 FF
1A 1BD3 FF
1A 1BD4 FF
//************ ADV8005 4k × 2k TTL Input Mode ****
1A 1A07 26
1A 1B48 0D
1A 1B4B 80
1A E401 10
1A E430 58
//************** CPLD Writes *********************************
EA 07 00
EA 03 0D
EA 03 2D
EA 03 45
EA 03 60
EA 03 80
EA 03 A0
EA 03 CE
EA 03 E0
```

```
//******** ADV8005 Tx – 32 kHz PCM I2S Multichannel Audio Mode
1A F441 10
1A F401 00
1A F402 10
1A F403 00
1A F413 FF
1A F415 30
1A F416 61
1A F440 80
1A F44C 06
1A F455 40
1A F456 08
1A F473 07
1A F476 1F
1A F496 20
1A F4AF 96
1A F4BA 70
1A F4D0 44
1A F4D1 3C
1A F4D3 07
1A F4D6 02
1A F4DB 0B
1A F4E0 90
1A F4E1 FC
1A F4E3 D0
1A F4E8 F0
1A F4EA 1D
1A F4ED 40
1A F4EE 40
1A F4EF 41
1A F4F3 01
1A F4F5 CC
1A F4F6 08
1A F4F7 F0
1A F4DA 40
1A F4F5 D4
1A F480 7F
1A F481 88
1A F482 88
1A F483 81
1A F484 81
1A F485 81
1A F486 81
1A F4FC 55
1A F441 30
1A F441 10
1A FB24 40
```

```
//***********ADV8005 Tx Source Termination On**********
1A F480 7F
1A F483 03
1A F484 03
1A F485 03
1A F486 03
1A F4EA BD
1A F4ED B8
1A F4EE B8
1A F4EF B9
//***********ADV8005 Tx  Enabling Spare Packets**********
1A F44C 04
1A F440 83
1A F444 69
1A FAC0 81
1A FAC1 01
1A FAC2 04
1A FAC3 6B
1A FAC4 03
1A FAC5 0C
1A FAC6 00
1A FAC7 00
1A FAC8 00
1A FAC9 00
1A FACA 00
1A FACB 00
1A FACC 00
1A FACD 00
1A FACE 00
1A FACF 00
1A FAD0 00
1A FAD1 00
1A FAD2 00
1A FAD3 00
1A FAD4 00
1A FAD5 00
1A FAD6 00
1A FAD7 00
1A FAD8 00
1A FAD9 00
1A FADA 00
1A FADB 00
1A FADC 00
1A FADD 00
1A FADE 00
1A FADF 00
1A FADF 80
```

```
1A FADF 00
1A FAE0 82
1A FAE1 02
1A FAE2 0D
1A FAE3 7D
1A FAE4 60
1A FAE5 A8
1A FAE6 00
1A FAE7 61
1A FAE8 00
1A FAE9 00
1A FAEA 00
1A FAEB 71
1A FAEC 08
1A FAED 00
1A FAEE 00
1A FAEF 01
1A FAF0 0F
1A FAF1 00
1A FAF2 00
1A FAF3 00
1A FAF4 00
1A FAF5 00
1A FAF6 00
1A FAF7 00
1A FAF8 00
1A FAF9 00
1A FAFA 00
1A FAFB 00
1A FAFC 00
1A FAFD 00
1A FAFE 00
1A FAFF 00
1A FAFF 80
1A FAFF 00
```

REFERENCES

CEA-861F Specification. Consumer Electronics Organization, 2013.

*HDMI 2.0 Specification. (*Note that the specification is available to HDMI 2.0 adopters after paying licensing fee via the HDMI 2.0 online forum.)

Jack, Keith. *Video Demystified*. Newnes, 2007.

Kaczurba, Witold. AN-1283 Application Note. *Receiving the 4:2:0 Stream with the ADV7619.* Analog Devices, Inc., 2014.

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).