**Digital Potentiometers: Frequently Asked Questions**

**INTRODUCTION**

This application note answers a series of frequently asked questions (FAQs) about Analog Devices, Inc., digital potentiometer (digiPOT) products. It includes general questions as well as specific questions, including product-specific questions. In addition, digiPOT configuration information is provided.

**What is a digiPOT?**

A digiPOT is a digitally controlled resistor that changes the impedance between the terminals and wiper depending on the code loaded in the RDAC register. Digital potentiometers avoid the problems that mechanical potentiometers face, such as physical size and wear and tear, as well as sensitivity to vibration, temperature, and humidity. A digiPOT may be configured in two different modes, potentiometer and rheostat.

A potentiometer (see Figure 1) has three terminals. Terminal A, Terminal B, and Terminal W (wiper).

A rheostat is formed when one of the terminals is hardwired to either Terminal A or Terminal B (see Figure 2). Some parts only offer two terminals, Terminal A and Terminal W.

A Windows®-compatible evaluation software, along with the driver software, is often included on a CD that comes with the evaluation board kit. For newer products, most of this information is available online.

**Where do I find the evaluation tools and software pertaining to the evaluation board?**

EngineerZone is an Analog Devices online support community. Support for the digiPOT is found in the community named Precision DACs. Customers from all over the world can post questions, and view existing questions and answers as well as review and contribute to ongoing discussions in this community.
DIGIPOT FAQS BY CATEGORY

GENERAL FAQS

Is there a recommended power-up sequence?
Yes, the product data sheet provides a recommended start-up sequence to refer to before powering up the device.

Generally, it is good practice to power VDD first and VSS second. The order of VA, VB, and VW is not important, but these should be powered last.

There are ESD protection diodes between the VDD and the A, B, and W terminals. For example, the cathode of one of the diodes connects to VDD and the anode connects to the A terminal. As a result, any voltage occurring at the A terminal before VDD forward biases the diode and powers the VDD.

For some of the digiPOTs, the digital signals should also be powered after VDD. This is documented in the relevant data sheet.

Are all digiPOTs limited to |5 V|?
No, a wide portfolio of digiPOTs are available to handle large unipolar and bipolar power supplies. Refer to the online brochure for an up-to-date product list.

Do digiPOTs handle bipolar and ac operations?
Yes, Analog Devices offers digiPOTs with dual ±2.5 V, ±5 V, or ±15 V supplies that can handle bipolar or ac operation. One can still achieve ac operation with a single dc supply if one raises the dc offset. Terminal A, Terminal B, and Terminal W have no polarity constraints with respect to one another.

For dual-supply digiPOTs, if VDD/VSS are +2.5 V/−2.5 V, respectively, can digital inputs be fed from a standard 3.3 V CMOS logic component without logic level translation? What are the logic level thresholds when VDD is +2.5 V and VSS is −2.5 V?
When using a bipolar ±2.5 V digiPOT, the maximum digital supply is limited to VDD +0.3 V or VLOGIC + 0.3 V. Otherwise, the internal protection diodes clamp the voltage and may be damaged. Be sure to check the data sheets for more details on digiPOT levels.

Is there a dependency between the logic level and power consumption?
Yes. If the logical level is lower than the logic supply (VDD or VLOGIC, if available), the input gates do not switch completely and the part consumes more power.

Why replace a mechanical potentiometer with a digiPOT?
There are a few advantages to using a digiPOT vs. a mechanical potentiometer, namely
- Higher resolution
- More reliability
- Better dynamic control

However, a digiPOT is not a direct replacement for a mechanical potentiometer. See the Is a digital potentiometer a real replacement for a mechanical potentiometer or are there restrictions regarding voltage potentials? question for more information.

Is a digital potentiometer a real replacement for a mechanical potentiometer or are there restrictions regarding voltage potentials?
A digital potentiometer is not an exact replacement for a mechanical potentiometer. VA and VB must not be greater than VDD or less than VSS (or GND if the part does not have a VSS pin). For example, if the desired VA and VB are +2 V and −2 V respectively, then VDD must be lower than or equal to +2 V and VSS must be higher than or equal to −2 V.

Refer to the AN-1121 Application Note, Replacing Mechanical Potentiometers with Digital Potentiometers for more information on this topic.

For digiPOTs without nonvolatile memory, what is the state during power-up?
Most Analog Devices digiPOTs (with the notable exception of the AD8400/AD8402/AD8403) contain power-on reset (POR) circuitry, which presets the wiper-to-terminal resistance to the middle value of the terminal-to-terminal resistance. For example, if RAB = 10 kΩ, then, at power-up, RWB = RWA = 5 kΩ.

For the digiPOTs that do not have this feature, the wiper-to-terminal resistance can be anything at power-up. Refer to the relevant data sheets for more details.

Is there a particularly low power digital potentiometer?
Yes. The AD5165 is an Analog Devices product that offers ultralow power consumption. An online brochure provides an up-to-date product list.

Does the memory allow the device to return to the last stored value without an update from a microprocessor?
Yes. It is automatically set to the previously stored value each time the device is powered. By default, the EEPROM is factory programmed to midscale.

How good is the resistance matching between Ch1 and Ch2 in the dual digital potentiometer?
The matching is typically 0.1% to 0.2% and ±1% is usually specified as a maximum.

How is the resistance matching device to device?
Assuming the parts come from the same batch, the resistance matching device to device is believed to be ±1%.
What is the resistance tolerance of the digiPOTs?

Refer to the relevant device data sheets for an exact figure. If using the potentiometer in the 3-terminal voltage divider mode (without any series resistor), the tolerance is irrelevant because the resistances RWA and RWB are ratiometric. If using the potentiometer in the 2-terminal rheostat mode, account for the worst case variation.

On some nonvolatile digiPOTs, resistance tolerance is stored in memory at the factory with an accuracy of 0.1%. Thus, users can retrieve the resistance tolerance and calibrate the system accordingly.

Can I cascade, serialize, or parallel multiple digiPOTs to get the resistance or resolution needed? My requirement is for a 250 Ω digital potentiometer with approximately 1 Ω per step. I plan to use four 1 kΩ AD8403 in parallel with each set to nominally the same value?

Yes, see the AN-582 Application Note, Resolution Enhancements of Digital Potentiometers with Multiple Devices.

How is a digital potentiometer designed? How ideal are the wiper switches?

A digiPOT is a purely CMOS device. All switches are large CMOS transmission gates operated in the linear region to yield low uniform $R_{DS(ON)}$. All resistor elements are polysilicon or thin film resistors.

What is the tempco of the digital potentiometer?

There are two components that make up the resistance at any given setting. They are the polysilicon or thin film resistors (step resistor $R_s$) and the CMOS switch resistor ($R_{SW} = 50 \, \Omega$ at 5 V supply). Together, they add up such that

$$R_{WB} = R_s + R_{SW}$$

$$R_s = \frac{R_{SW}}{2^N}$$

The temperature coefficient (tempco) of the step resistor, which is published in the data sheet, is typically −35 ppm/°C for thin film or 600 ppm/°C for polysilicon. The resistance of the switch, on the other hand, doubles in 100°C. As a result, the overall tempco is nonlinear and it is worse off at low value codes where the switch resistance dominates. Users should refer to the tempco graphs in the data sheets for more detailed information.

What is the maximum current I can force into the digital potentiometer?

The maximum current is limited by three boundaries at a given resistance setting. They are the maximum applied voltage across any two of the A, B, and W terminals, the power dissipation of the package and the maximum current handling capabilities of the internal switches.

Each data sheet refers to this maximum current in the Absolute Maximum Ratings section (see Table 1 for an example).

Do Analog Devices digiPOTs suffer from leakage currents which could affect the gain of the circuit?

DigiPOTs are manufactured with a very low leakage analog switch process, which results in low leakage currents. They are usually specified with a common-mode leakage current of 1 nA typical.

Table 1. Maximum Current Through DigiPOT Terminal: Absolute Maximum Ratings Table Example

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{A, B, W}$</td>
<td>Pulsed</td>
</tr>
<tr>
<td>Frequency &gt; 10 kHz</td>
<td>$R_{SW} = 5 , \Omega$ and 10 $\Omega$ $\pm 6 , mA/d$</td>
</tr>
<tr>
<td>$R_{SW} = 80 , k\Omega$</td>
<td>$\pm 1.5 , mA/d$</td>
</tr>
<tr>
<td>Frequency ≤ 10 kHz</td>
<td>$R_{SW} = 5 , \Omega$ and 10 $\Omega$ $\pm 6 , mA/\sqrt{d}$</td>
</tr>
<tr>
<td>$R_{SW} = 80 , k\Omega$</td>
<td>$\pm 1.5 , mA/\sqrt{d}$</td>
</tr>
<tr>
<td>Continuous</td>
<td>$R_{SW} = 5 , \Omega$ and 10 $\Omega$ $\pm 6 , mA$</td>
</tr>
<tr>
<td>$R_{SW} = 80 , k\Omega$</td>
<td>$\pm 1.5 , mA$</td>
</tr>
</tbody>
</table>

Note that $d$ stands for pulse duty factor.

Calculating the pulsed current is dependant on the frequency. If the frequency is less than or equal to 10 kHz, the formula is as follows:

$$I_d = I_{peak} \times \sqrt{d}$$

If the frequency is greater than 10 kHz, the formula is as follows:

$$I_d = I_{peak} \times d$$

where:

$I_d$ = Maximum dc current

$I_{peak}$ = Maximum peak current value for waveform

$d$ = Duty factor (0.1 = 10% duty cycle)

Regarding the specification on R-DNL, I am only concerned with relative adjustments. What if I’m not concerned with the actual value of the resistor in the digiPOT, but need the digiPOT to be monotonic?

In a digiPOT that is in rheostat mode, there are two specifications known as R-INL and R-DNL, resistor integral nonlinearity and resistor differential nonlinearity, respectively. INL is defined as the maximum deviation between the ideal output of a DAC and the actual output level. R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. DNL is the maximum deviation between two consecutive codes over the DAC transfer function. R-DNL measures the relative step change from the ideal between successive tap positions.

All Analog Devices digiPOTs are guaranteed monotonic.

Is there crosstalk between Ch1 and Ch2 of a dual digiPOT such that a sine wave applied to Ch1 occurs in Ch2 as well?

Yes. The product data sheet usually details such performance. It is typically −70 dB.
If Ch 1 is programmed from zero to full scale, should one expect Ch 2 to be disturbed?

This is step response crosstalk. It is different from analog crosstalk. The data sheet usually details this information. This crosstalk is typically in the range of 5 nV/sec to 10 nV/sec. Figure 4 shows an example of digital crosstalk.

What is digital feedthrough?

Digital feedthrough is the amount of noise from clock or data coupled into the output. It is usually very small (few nV/sec range). Figure 5 shows an example of digital feedthrough.

How is the THD performance of the digital potentiometer?

This parameter is code and VDD dependent. Typically, it is in the range of −86.02 dB to −60 dB. Refer to the product data sheet for specific performance. The best THD performance is achieved when the part is operated at its maximum operating voltage. The AD5292 can achieve THD up to −100 dB.

How can I control a digiPOT that requires a 6-bit word length using an 8-bit word length from my controller?

SPI interface digital potentiometers operate by disregarding the first two MSBs and reading the next six bits. Refer to product data sheet for more information.

How can I control a digiPOT that requires a 12-bit word length using an 8-bit word length from my controller?

Issue a 2-byte word. The first four MSBs are disregarded. Refer to product data sheet for more information.

How can multiple digiPOTs be daisy-chained?

To daisy-chain digiPOTs, the SDO pin of one package must be tied to the SDI pin of the next package. The clock period may need to be increased due to propagation delay.

In Figure 6, two AD5122 digiPOTs are tied together. In this setup, 32 bits are required; the first 16 bits are sent to U2 and the second 16 bits are sent to U1. During this 32-bit write, SYNC is kept low.

Once all bits are clocked in, the SYNC pin is pulled high to complete the write. With the AD5144 and other similar SPI parts, to prevent data from corruption due to noise, for example, the digiPOTs include internal counters. If the number of clocks is different than expected, then the data is ignored. When SYNC is high, the counter resets. Refer to product data sheet for more information.
Can I program two channels of a multichannel digital potentiometer at the same time?

Yes. With a selection of digiPOTs, such as the AD5251/AD5252/AD5253/AD5254 and AD5232/AD5233/AD5235 are able to increment and decrement all the channels simultaneously. In addition, the user can write to each EEMEM and then issue a reset command to update all the RDAC settings simultaneously.

Some of the products, such as the AD5144, include an LRDAC pin (for loading the RDAC input register) which transfers data from the input register to the RDAC register and updates the wiper position. Either a single RDAC register or all registers can be updated at once.

Can the wiper setting of digiPOTs be readback? How about the contents of two RDAC registers of dual I2C-compatible digiPOTs, such as the AD5242 and AD5282?

Yes, one can readback the wiper setting with a selection of digiPOTs.

Once can also readback the RDAC register content (the RDAC value of a specific channel). However, one can only read the RDAC channel that was selected during the previous write mode. If the channel one wants to read from is different from the channel previously written to, a dummy write command is necessary to select the desired channel. Refer to the respective data sheet for details.

Is there a digiPOT controlled by a parallel input?

No.

What are the WP, PR, and RDY features?

WP stands for write protect. For example, on the ADN2850, WP disables any changes to the scratchpad register contents. A scratchpad register directly controls the digital resistor wiper and has no limit on the number of changes (unlike the EEPROM, which has a limitation on the number of writes).

However, commands that restore the wiper position using the EEPROM are still allowed. Therefore, the WP pin is used as a method of protecting the EEPROM contents.

In addition, on the ADN2850, the hardware override preset (PR) pin can be used to overwrite the scratchpad register with the EEPROM contents.

The RDY pin signifies when commands have been completed thus indicating readiness for the next command.

For further information, refer to the specific product data sheet.

What is the ESD rating of digital potentiometers?

All digiPOTs have ESD ratings higher than 1 kV. Refer to the product data sheet for more information.

How can I determine the end-to-end $R_{AB}$ resistance value on the digiPOT package?

The ordering guide section of each data sheet includes a model number and branding code. For example, the AD8400 uses a SOIC package which is branded with AD8400AR1, AD8400AR10, and AD8400AR100, which represents an $R_{AB}$ of 1 kΩ, 10 kΩ, or 100 kΩ, respectively. With the more compact packages, three letter codes are used. Using the branding code in the data sheet helps to determine the $R_{AB}$. 
FAQS ABOUT DIGIPOTS WITH EEPROM MEMORY

Will the data in the EEMEM need to be refreshed after 15 years when it is operated at 55°C?

Yes. The EEPROM cells lose their charge over a period of 15 years when operating at 55°C.

Measured as retention time, it is extrapolated using a model as defined by De Salvo et al. in Experimental and Theoretical Investigation of Nonvolatile Memory Data-Retention. This IEEE article can be found online.

\[ t_R = t_0 \times e^{\frac{E_a}{kT}} \]

where:
- \( t_R \) is retention time based on temperature
- \( t_0 \) is retention time corresponding to an infinite temperature
- \( E_a \) is activation energy
- \( k \) is Boltzmann's Constant
- \( T \) is temperature

For other operating temperatures, see Figure 7. Analog Devices digiPOTs are qualified in accordance with the JEDEC Retention Lifetime Specification (A117) at a specific junction temperature of \( T_j = 55°C \).

As part of this qualification procedure, the Flash/EE memory is cycled to its specified endurance limit before data retention is characterized. This means that the Flash/EE memory is guaranteed to retain its data for its full specified retention lifetime every time the Flash/EE memory is reprogrammed. Note that retention lifetime, based on an activation energy of 0.7 eV, derates with \( T_j \). This data applies to all nonvolatile memory digiPOTs.

![Figure 7: Example of Data Retention vs. Temperature](image)

After the specified EEMEM data retention timeout period, can the power be turned off and then back on so that the part is considered refreshed?

No. Doing so only refreshes the RDAC register, but not the EEPROM. The data will have to be reloaded again after 15 years to put a fresh charge into the EEPROM cell. This can be done by writing the RDAC wiper register data back to the EEPROM before the end of 15 years.

Why is the maximum operating temperature for some Digipots only 85°C instead of the standard 125°C?

The digiPOTs that contain EEPROMs usually only work up to 85°C. This is because EEPROMs are only guaranteed to safely operate below 85°C.
If I use the digital potentiometer in audio volume control, will I experience zipper noise?

There is noticeable zipper noise. However, Analog Devices has developed a logarithmic audio volume control with glitch reduction using the AD5292 digital potentiometer. Refer to the AN-1209 Application Note, Logarithmic Audio Volume Control with Glitch Reduction Using the AD5292 Digital Potentiometer.

Can digital potentiometers do log taper adjustment?

Pseudo log taper adjustment is usually preferred in applications such as audio control. However, the answer is yes, for users of the AD5231/AD5232/AD5233/AD5235 or ADN2850. On the other hand, a pseudo log taper adjustment is possible in other linear adjustment potentiometers (pots) with this simple configuration. For more information, an article titled Tack a Log Taper onto a Digital Potentiometer, published in January 2000 by Hank Zumblen, is available online.

Audio Volume Control

Because of its good THD performance and high voltage capability, the AD7376 can be used for digital volume control. If the AD7376 is used directly as an audio attenuator or gain amplifier, a large step change in the volume level at any arbitrary time can lead to an abrupt discontinuity of the audio signal, causing an audible zipper noise. To prevent this, a zero-crossing window detector can be inserted to the $CS$ line to delay the device update until the audio signal crosses the window. Since the input signal can operate on top of any dc levels rather than absolute zero volt level, zero-crossing, in this case, means the signal is ac-coupled and the dc offset level is the signal zero reference point.

The configuration to reduce zipper noise and the result of using this configuration are shown in Figure 9 and Figure 10, respectively. The input is ac-coupled by C1 and attenuated down before feeding into the window comparator formed by U2, U3, and U4B. U6 is used to establish the signal zero reference. The upper limit of the comparator is set above its offset and, therefore, the output pulses high whenever the input falls between 2.502 V and 2.497 V (or 0.005 V window) in this example. This output is AND'ed with the chip select signal such that the AD7376 updates whenever the signal crosses the window. To avoid constant update of the device, the chip select signal should be programmed as two pulses, rather than the one shown in the AD7376 data sheet.

In Figure 10, the lower trace shows that the volume level changes from a quarter scale to full scale when a signal change occurs near the zero-crossing window. The AD7376 shutdown sleep mode programming feature can be used to mute the device at power-up by holding SHDN low and programming zero scale.

Figure 8. Logarithmic Audio Volume Control with Glitch Reduction (Simplified Schematic: Decoupling; All Connections Not Shown)
Audio Amplifier with Volume Control

The AD5228 and SSM2211 can form a 1.5 W audio amplifier with volume control that has adequate power and quality for portable devices, such as PDAs and cell phones. The SSM2211 can drive a single speaker differentially between Pin 5 and Pin 8 without any output capacitor. The high-pass cutoff frequency is \( f_{H1} = \frac{1}{2 \pi R_1 C_1} \).

The SSM2211 can also drive two speakers as shown in Figure 11. However, the speakers must be configured in single-ended mode, and output coupling capacitors are needed to block the dc current. The output capacitor and the speaker load form an additional high-pass cutoff frequency as \( f_{H2} = \frac{1}{2 \pi R_5 C_3} \). As a result, \( C_3 \) and \( C_4 \) must be large to make the frequency as low as \( f_{H1} \).

NOTES
1. THE LOWER TRACE SHOWS THAT THE VOLUME LEVEL CHANGES FROM QUARTER SCALE TO FULL SCALE, WITH THE CHANGE OCCURRING NEAR THE ZERO-CROSSING WINDOW.

Figure 11. Audio Amplifier with Volume Control
Can I adjust the digiPOT for frequencies around 1 MHz to 10 MHz for adjusting the gain of a video signal?

Bandwidth is a function of the code and end-to-end resistance $R_{AB}$. Lower $R_{AB}$ and codes yield higher bandwidth. Note that 10 MHz bandwidth or above is possible on some digiPOTS. Refer to product data sheets for the Bode plots.

What is the maximum frequency that can be applied to the digital potentiometer CLK input?

For SPI and Up/Down (U/D) digital interfaced digiPOTS, the maximum clock frequency is in the range of 10 MHz to 50 MHz. For I²C-compatible digiPOTS, the maximum clock frequency is guaranteed for 400 kHz.

LCD Panel VCOM Adjustment

A special feature of the AD5259 is its separation of the $V_{\text{LOGIC}}$ and $V_{\text{DD}}$ supply pins. The separation provides greater flexibility in applications that do not always provide needed supply voltages.

In particular, LCD panels require a VCOM voltage in the range of 3 V to 5 V.

Figure 12 shows a rare exception in which a 5 V supply is available to power the digital potentiometer.

![Figure 12. VCOM Adjustment Application](image)

In the more common case shown in Figure 13, only analog 14.4 V and digital logic 3.3 V supplies are available. By placing discrete resistors above and below the digital potentiometer, $V_{\text{DD}}$ can now be tapped off the resistor string itself. Based on the chosen resistor values, the voltage at $V_{\text{DD}}$ in this case equals 4.8 V, allowing the wiper to be safely operated all the way up to 4.8 V. The current draw of $V_{\text{DD}}$ will not affect the bias of the node because it is only on the order of microamps. $V_{\text{LOGIC}}$ is tied to the MCU 3.3 V digital supply because $V_{\text{LOGIC}}$ draws the 35 mA needed when writing to the EEPROM. It would be impractical to try and source 35 mA through the 70 kΩ resistor, therefore, $V_{\text{LOGIC}}$ is not connected to the same node as $V_{\text{DD}}$.

![Figure 13. Circuitry When a Separate Supply is not Available for $V_{\text{DD}}$](image)

For this reason $V_{\text{LOGIC}}$ and $V_{\text{DD}}$ are provided as two separate supply pins that can either be tied together or treated independently; $V_{\text{LOGIC}}$ supplies the logic/EEPROM with power and $V_{\text{DD}}$ biasing the A, B, and W terminals for added flexibility.

For a more detailed look at this application, an article entitled, Simple VCOM Adjustment uses any Logic Supply Voltage in the September 30, 2004 issue of EDN magazine can be found online.

Manual Control with Rotary Encoder

Figure 14 shows another way of using the AD5227 to emulate a mechanical potentiometer in a rotary knob operation. The rotary encoder U1 has a C ground terminal and two out-of-phase signals, A and B.

When U1 is turned clockwise, a pulse generated from the B terminal leads a pulse generated from the A terminal and vice versa. Signals A and B of U1 pass through a quadrature decoder U2 that translates the phase difference between A and B of U1 into compatible inputs for U3 AD5227. Therefore, when B leads A (clockwise), U2 provides the AD5227 with a logic high U/D signal, and vice versa. U2 also filters noise, jitter, and other transients as well as debouncing the contact bounces generated by U1.

Refer to the AN-1150 Application Note for information on how to control the AD5111, AD5113, and AD5115 with a traditional dial interface.
**Six-Bit Controller**

The AD5227 can form a simple 6-bit controller with a clock generator, a comparator, and some output components. Figure 15 shows a generic 6-bit controller with a comparator that first compares the sampling output with the reference level and outputs either a high or low level to the AD5227 U/D pin. The AD5227 then changes step at every clock cycle in the direction indicated by the U/D state. This circuit is self-contained, easy to design, and can adapt to various applications.

**Multiple Devices on One I²C Bus**

The AD5253/AD5254 are equipped with two addressing pins, AD1 and AD0, that allow up to four AD5253/AD5254 devices to be operated on one I²C bus. To achieve this result, the states of AD1 and AD0 on each device must first be defined.

An example is shown in Table 2 and Figure 16. In I²C programming, each device is issued a different slave address—01011(AD1)(AD0)—to complete the addressing.

<table>
<thead>
<tr>
<th>AD1</th>
<th>AD0</th>
<th>Device Addressed</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>U1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>U2</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>U3</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>U4</td>
</tr>
</tbody>
</table>

In wireless base station smart antenna systems that require arrays of digital potentiometers to bias the power amplifiers, large numbers of AD5253/AD5254 devices can be addressed by using extra decoders, switches, and I/O buses, as shown in Figure 16. For example, to communicate to a total of 16 devices, four decoders and 16 sets of combinational switches (four sets shown in Figure 16) are needed. Two I/O buses serve as the common inputs of the four 2 × 4 decoders and select four sets of outputs at each combination. Because the four sets of combination switch outputs are unique, as shown in Figure 16, a specific device is addressed by properly programming the I²C with the slave address defined as 01011(AD1)(AD0).

This operation allows one of 16 devices to be addressed, provided that the inputs of the two decoders do not change states. The inputs of the decoders are allowed to change once the operation of the specified device is completed.
**Level Shifting for Bidirectional Interface**

While most legacy systems can be operated at one voltage, a new component can be optimized at another voltage. When two systems operate the same signal at two different voltages, proper level shifting is needed. For instance, users can employ a 3.3 V EEPROM to interface with a 5 V digital potentiometer. A level shifting scheme is needed to enable a bidirectional communication so that the setting of the digital potentiometer can be stored in and retrieved from the EEPROM. Figure 17 shows one of the level-shifting implementations. M1 and M2 can be any N-channel signal FETs, or if $V_{DD}$ falls below 2.5 V, M1 and M2 can be low threshold FETs, such as the FDV301N. This circuit is not suitable for 1.8 V logic levels.
GAIN

The following circuits have been designed for dc operation. If the circuits are used with an ac signal excitation, it could result in stability issues. To guarantee that the circuit does not oscillate, it is recommended to place a 10 pF capacitor in the feedback loop.

Additionally, if the recommended op amps are substituted, take note of the following restrictions:

\[
GBP < BW(V_{OUT})
\]

\[
\text{Bandwidth of } V_{OUT} = \frac{1}{2\pi R_{OUT} C}
\]

where:
- \( C \) is the total capacitance connected to the \( V_{OUT} \) pin (pin capacitance).
- \( R_{OUT} \) is the amplifier output impedance.

\( R_{OUT} \) is generally specified in the data sheet specifications or in the typical performance characteristic plots. Refer to the Analog Dialogue article, *Practical Techniques to Avoid Instability Due to Capacitive Loading*, Volume 38, Number 2, 2004.

**Linear Gain Setting Mode**

For information on this topic, refer to the AN-1169 Application Note, *Linear Setting Mode: A Detailed Description*.

**Bipolar Programmable Gain Amplifier**

For applications requiring bipolar gain, Figure 15 shows one implementation. Digital Potentiometer U1 sets the adjustment range; the wiper voltage \( (V_{W2}) \) can, therefore, be programmed between \( V_I \) and \( -K V_I \) at a given U2 setting.

Configure ADA4077-2 (A2) as a noninverting amplifier that yields a transfer function of

\[
\frac{V_O}{V_I} = \left(1 + \frac{R_2}{R_1}\right) \times \left(\frac{D_2}{1024}\right) \times (1 + K) - K
\]

where \( K \) is the ratio of \( R_{W2}/R_{W1} \) set by U1.

![Figure 18. Bipolar Programmable Gain Amplifier](image-url)

In the simpler (and much more usual) case where \( K = 1 \), \( V_O \) is simplified to

\[
V_O = \left(1 + \frac{R_2}{R_1}\right) \times \left(\frac{2D_2}{1024} - 1\right) \times V_I
\]

Table 3 shows the result of adjusting D2, with ADA4077-2 (A2) configured as a unity gain, a gain of 2, and a gain of 10. The result is a bipolar amplifier with linearly programmable gain and 1024-step resolution.

**Table 3. Result of Bipolar Gain Amplifier**

<table>
<thead>
<tr>
<th>D2</th>
<th>R1 = ∞, R2 = 0</th>
<th>R1 = R2</th>
<th>R2 = 9 × R1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>−1</td>
<td>−2</td>
<td>−10</td>
</tr>
<tr>
<td>256</td>
<td>−0.5</td>
<td>−1</td>
<td>−5</td>
</tr>
<tr>
<td>512</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>768</td>
<td>0.5</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>1023</td>
<td>0.992</td>
<td>1.984</td>
<td>9.92</td>
</tr>
</tbody>
</table>

**Gain Control Compensation**

A digital potentiometer is commonly used in gain control such as the noninverting gain amplifier shown in Figure 19.

![Figure 19. Gain Control Compensation](image-url)

When the RDAC B terminal parasitic capacitance is connected to the op amp noninverting node, it introduces a zero for the \( 1/\beta_0 \) term with 20 dB/dec, whereas a typical op amp gain bandwidth product (GBP) has −20 dB/dec characteristics. A large \( R_2 \) and finite \( C_1 \) can cause the frequency of this zero to fall well below the crossover frequency. Therefore, the rate of closure becomes 40 dB/dec, and the system has a 0° phase margin at the crossover frequency. If an input is a rectangular pulse or step function, the output can ring or oscillate. Similarly, it is also likely to ring when switching between two gain values; this is equivalent to a stop change at the input.

Depending on the op amp GBP, reducing the feedback resistor might extend the frequency of the zero far enough to overcome the problem. A better approach is to include a compensation capacitor, \( C_2 \), to cancel the effect caused by \( C_1 \). Optimum compensation occurs when \( R_1 \times C_1 = R_2 \times C_2 \). This is not an option because of the variation of \( R_2 \). As a result, one can use the previous relationship and scale \( C_2 \) as if \( R_2 \) were at its maximum value. Doing this might overcompensate and compromise the performance when \( R_2 \) is set at low values.

Alternatively, it avoids the ringing or oscillation at the worst case. For critical applications, find \( C_2 \) empirically to suit the oscillation. In general, \( C_2 \) in the range of a few picofarads to no more than a few tenths of picofarads is usually adequate for the compensation.

Similarly, \( W \) and \( A \) terminal capacitances are connected to the output (not shown); their effect at this node is less significant and the compensation can be avoided in most cases.
LED DRIVER

Manual Adjustable LED Driver

The AD5228 can be used in many electronics-level adjustments, such as LED drivers for LCD panel backlight controls. Figure 20 shows a manually adjustable LED driver. The AD5228 sets the voltage across the white LED D1 for brightness control. Since U2 handles up to 250 mA, a typical white LED with VF of 3.5 V requires a resistor, R1, to limit U2 current. This circuit is simple, but not power efficient. The U2 shutdown pin can be toggled with a PWM signal to conserve power.

![Figure 20. Low Cost Adjustable LED Driver](image)

Adjustable Current Source for LED Driver

Since LED brightness is a function of current rather than forward voltage, an adjustable current source is preferred over a voltage source as shown in Figure 21.

The load current can be found as the VWB of the AD5227 divided by RSET.

\[
I_D = \frac{V_{WB}}{R_{SET}}
\]

The U1 ADP3333ARMZ-1.5 is a 1.5 V LDO that is lifted above or lowered below 0 V. When VWB of the AD5227 is at minimum, there is no current through D1, so the GND pin of U1 would be at −1.5 V if U3 were biased with the dual supplies. As a result, some of the U2 low resistance steps have no effect on the output until the U1 GND pin is lifted above 0 V.

When VWB of the AD5227 is at its maximum, VOUT becomes VL + VAB, so the U1 supply voltage must be biased with adequate headroom. Similarly, a PWM signal can be applied at the U1 shutdown pin for power efficiency. This circuit works well for a single LED.
VOLTAGE TO CURRENT CONVERSION

Voltage to Current Conversion: Programmable Current Source

A programmable current source can be implemented with the circuit shown in Figure 22.

\[
I_L = \frac{V_{\text{REF}} \times D}{R_s \times 1024}
\]

The circuit is simple, but be aware that there are two issues. First, dual-supply op amps are ideal because the ground potential of REF191 can swing from −2.048 V at zero scale to \(V_L\) at full scale of the potentiometer setting. Although the circuit works under single-supply, the programmable resolution of the system is reduced. Second, the voltage compliance at \(V_L\) is limited to 2.5 V or equivalent to a 125 Ω load. Should higher voltage compliance be needed, users can consider digital potentiometers AD5260, AD5280, and AD7376.

Figure 22 shows an alternate circuit for high voltage compliance. To achieve higher current, such as when driving a high power LED, the user can replace UI with an LDO, reduce \(R_s\), and add a resistor in series with the digital potentiometer A terminal. This limits the current of the potentiometer and increases the current adjustment resolution.

Voltage to Current Conversion: Programmable Bidirectional Current Source

For applications that require bidirectional current control or higher voltage compliance, a Howland current pump can be a solution.

If the resistors are matched, the load current is

\[
I_L = \frac{(R2A + R2B)}{R1} \times \frac{V_W}{R2B}
\]

\(R2B\), in theory, can be made as small as necessary to achieve the current needed within the A2 output current-driving capability. In this circuit, ADA4077-2 delivers ±5 mA in both directions, and the voltage compliance approaches 15 V. It can be shown that the output impedance is

\[
Z_O = \frac{R1' R2B (R1 + R2A)}{R1 R2' - R1' (R2A + R2B)}
\]

\(Z_O\) can be infinite if the R1 and R2 resistors match precisely with R1 and R2A + R2B, respectively. On the other hand, \(Z_O\) can be negative if the resistors are not matched.

As a result, C1, in the range of 1 pF to 10 pF, is needed to prevent oscillation from the negative impedance.
FILTERING

Programmable Low-Pass Filter

In analog-to-digital conversions, it is common to include an antialiasing filter to band limit the sampling signal. Therefore, the dual channel AD5235 can be used to construct a second order Sallen-Key low-pass filter as shown in Figure 24.

The design equations are

\[ \frac{V_{C}}{V_{i}} = \frac{\omega_{o}^{2}}{S^{2} + \omega_{o}S + \omega_{o}^{2}} \]

\[ \omega_{o} = \frac{1}{\sqrt{R_{1}R_{2}C_{1}C_{2}}} \]

\[ Q = \frac{1}{R_{1}C_{1}} + \frac{1}{R_{2}C_{2}} \]

First, users should select convenient values for the capacitors. To achieve maximally flat bandwidth, where \( Q = 0.707 \), let \( C_{1} \) be twice the size of \( C_{2} \) and let \( R_{1} \) equal \( R_{2} \). As a result, the user can adjust \( R_{1} \) and \( R_{2} \) concurrently to the same setting to achieve the desirable bandwidth.

Programmable State Variable Filter

One of the standard circuits used to generate a low-pass filter or band-pass filter is the state variable active filter. The AD5233 can be used in this application to provide full programmability of the frequency, gain, and the Q of the filter outputs.

Figure 25 shows a filter circuit using a 2.5 V virtual ground which allows for a \( \pm 2.5 \) V peak input and output swing. RDAC2 and RDAC3 set the low-pass, high-pass and band-pass cut-off and center frequencies, respectively. RDAC2 and RDAC3 should be programmed with the same data (as with ganged potentiometers) to maintain the best circuit Q.

The transfer function for the band-pass filter is

\[ \frac{V_{BP}}{V_{i}} = \frac{A_{o} \frac{\omega_{o}}{Q} S}{S^{2} + \frac{\omega_{o}}{Q} S + \omega_{o}^{2}} \]

where \( A_{o} \) is the gain.

For \( R_{WB2(D2)} = R_{WB3(D3)}, R_{1} = R_{2} \) and \( C_{1} = C_{2} \),

\[ \omega_{o} = \frac{1}{R_{WB}C_{1}} \]

\[ A_{o} = \frac{R_{WB1}}{R_{WA1}} \]

\[ Q = \frac{R_{WB4}}{R_{WB4} \times R_{WB1}} \]

Figure 25 shows the measured filter response at the band-pass output as a function of the RDAC2 and RDAC3 settings, which produce a range of center frequencies from 2 kHz to 20 kHz.

The filter gain response at the band-pass output is shown in Figure 25. At a center frequency of 2 kHz, the gain is adjusted over the \(-20 \) dB to \(+20 \) dB range, determined by RDAC1. Circuit Q is adjusted by RDAC4 and RDAC1. Suitable op amps for this application are ADA4077-2, AD8604, OP279, and AD824.
MISCELLANEOUS

Programmable Voltage Source with Boosted Output

For applications that require high current adjustment, such as a laser diode driver or tunable laser, a boosted voltage source can be considered (see Figure 26).

In this circuit, the inverting input of the op amp forces $V_O$ to be equal to the wiper voltage set by the digital potentiometer. The load current is then delivered by the supply via the N-Ch FET N1 (see Figure 26). N1 power handling must be adequate to dissipate $(V_I - V_O) \times I_L$ power.

This circuit can source a 100 mA maximum with a 5 V supply. For precision applications, a voltage reference, such as the ADR421 or ADR03, can be applied at Terminal A of the digital potentiometer.

High Voltage DAC

The AD7376 can be configured as a high voltage DAC as high as 30 V. The circuit is shown in Figure 27. The output is

$$V_O(D) = \frac{D}{128} \times \left[ 1.2 V \times \left( 1 + \frac{R_2}{R_1} \right) \right]$$

where $D$ is the decimal code from 0 to 127.

Programmable Oscillator

In a classic Wien bridge oscillator, the Wien network (R||C, R'C') provides positive feedback, whereas R1 and R2 provide negative feedback.

At the resonant frequency, $f_0$, the overall phase shift is zero, and the positive feedback causes the circuit to oscillate. With $R = R'$, $C = C'$, and $R_2 = R_2A / (R_2B + R_{DIODE})$, the oscillation frequency is

$$\omega_0 = \frac{1}{RC} \quad \text{or} \quad f_0 = \frac{1}{2\pi RC}$$

where $R$ is equal to $R_{WA}$ such that

$$R_{WA}(D) = \frac{1024 - D}{1024} \times R_{AB} + R_W$$

At resonance, setting $R_2/R_1 = 2$ balances the bridge. In practice, $R_2/R_1$ should be set slightly larger than 2 to ensure that oscillation can start. On the other hand, the alternate turn on of the diodes, D1 and D2, ensures that $R_2/R_1$ is smaller than 2, momentarily stabilizing the oscillation. When the frequency is set, the oscillation amplitude can be turned by $R_{2B}$ because

$$\frac{2}{3} V_O = I_D R_{2B} + V_D$$

$V_O$, $I_D$, and $V_D$ are interdependent variables. With proper selection of $R_{2B}$, an equilibrium is reached such that $V_O$ converges. $R_{2B}$ can be in series with a discrete resistor to increase the amplitude, but the total resistance cannot be too large to saturate the output.
Constant Bias with Supply to Retain Resistance Setting

Users who consider EEMEM potentiometers, but cannot justify the additional cost and programming for their designs, can consider constantly biasing the AD5227 with the supply to retain the resistance setting as shown in Figure 29.

The AD5227 is designed specifically with low power to allow power conservation even in battery-operated systems. As shown in Figure 30, a similar low power digital potentiometer is biased with a 3.4 V 450 mA/hour Li-Ion cell phone battery. The measurement shows that the device drains negligible power. Constantly biasing the potentiometer is a practical approach because most portable devices do not require detachable batteries for charging. Although the resistance setting of the AD5227 is lost when the battery needs to be replaced, this event occurs so infrequently that the inconvenience is minimal for most applications.
I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).