

Optimizing Video Platforms for Automated Post-Production Self-Tests

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INTRODUCTION

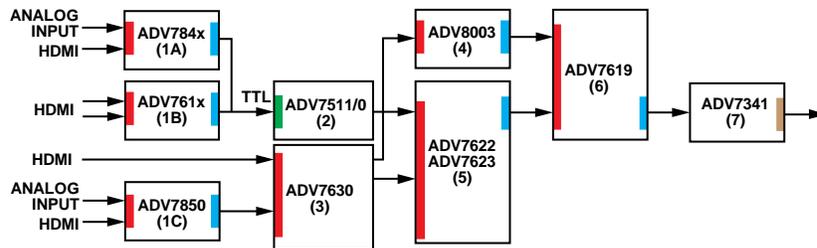
This application note describes techniques to use for post-production testing and debugging of video platform using advanced video (ADV) series devices.

Advanced video systems are becoming more complex and the video chains contain more and more links. Employing built-in, self-tests on video evaluation systems allows a significant increase in productivity by automated tests.

The ADV parts include features that allow finding a short, a disconnection, or a problem in video processing, audio

processing, or data/control circuitry. Many of ADV parts contain internal pattern generators, synchronization detection circuitry (for video), and built-in external memory tests that can be used to test a platform and facilitate the process of debugging a potentially faulty platform.

To test the system, it is assumed that final video processing circuitry contain a microprocessor unit that has a connection to tested video parts and contains a post-production program that can be enabled and run at least once after production.



BUILT-IN VIDEO BLOCKS ALLOWING DIAGNOSTICS:

- SIMPLIFIED STANDARD DETECTION BLOCK
(BASIC DETECTION OF 861-COMPLIANT INCOMING VIDEO TIMING)
- HDMI PARAMETERS AND/OR STDI DETECTION BLOCKS
(DETECTION OF INCOMING VIDEO)
- FREE RUN CAPABILITY
(ALLOWS INTERNALLY GENERATED VIDEO OUTPUT)
- BASIC VIDEO PATTERN GENERATOR
(ALLOWS INTERNALLY GENERATED VIDEO OUTPUT)

Figure 1. Hypothetical Video Chain Without External Memories, SPI, and I²C Buses

11339-001

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REVISION HISTORY

3/13—Revision 0: Initial Version

INTRODUCTION

SYSTEM TEST

The post-production test can be embedded into the processor's main code and executed once a jumper or external circuitry tells the microprocessor to post-test the board or system. Certain microprocessors allow the program stored in flash memory to rewrite its own flash memory content, which includes information regarding whether the self-test passed or not. Once passed, the test suite is never executed in a released product to a customer.

ALGORITHM

The self-test algorithm should maximize the number of tests to narrow the quantity of potentially failing circuitry. With this in mind, assume that the I²C and SPI interfaces that allow communication and carry out further tests must be tested first. In the case of big systems containing daisy-chain connected video processing parts, an additional set of tests can be implemented to find the specific unit failing to pass the video stream.

Figure 2 is an example algorithm showing one of the possible testing scenarios.

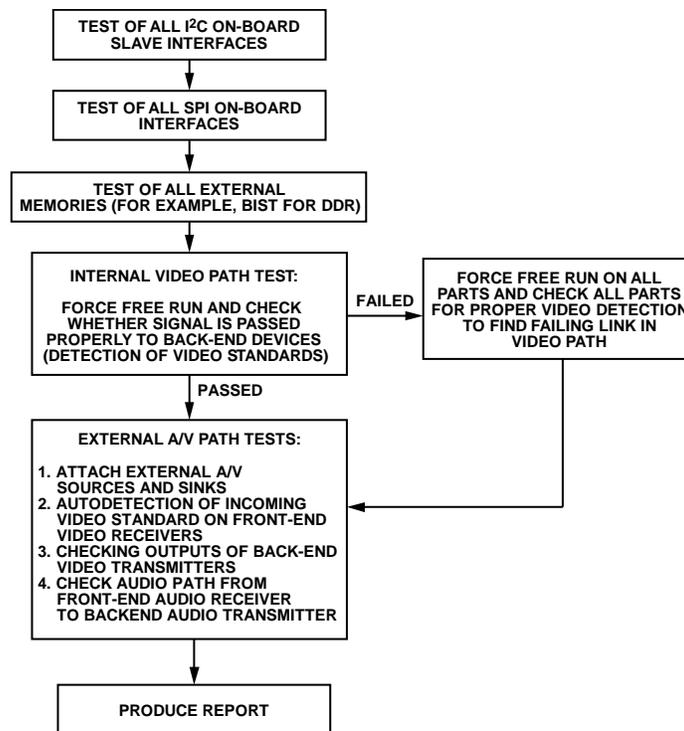


Figure 2. An Example Testing Algorithm

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VIDEO PATH TESTING

In the case of daisy-chained video devices, it might be difficult to find a break without employing proper tests.

Considering the scenario shown on Figure 3, it is possible to find the connection problem using the built-in HDMI® detection block. The algorithm should apply stimulus (HDMI signal) to the first HDMI transceiver (TRx) and check consecutive parts starting from the first one for proper HDMI signal on its receiver's side. Each of HDMI receivers and transceivers contain an HDMI parameter block (refer to the HDMI Measurement Block in HDMI Rx and TRx section) which allows checking of incoming HDMI link information. Based upon readbacks from blocks of each part, it is possible to find the broken link.

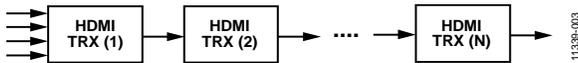


Figure 3. Daisy-Chained *ADV7630*

Note that long daisy-chaining systems can lead to aggregated jitter building in certain architectures. Therefore, they should be carefully monitored during system-level evaluation.

Figure 1 shows a hypothetical video chain using various Analog Devices, Inc., video processing components. Each of the parts contains the capability of generating video output (free run or basic video pattern generator; see the Testing of Video Data Output section) and/or detection of incoming video (STDI or HDMI parameter block; refer to the Testing of Video Input section). Those built-in features allow testing of video chains. Each of the parts capable of outputting video (such as 1A, 1B, 1C, 4, 5, and 6 in Figure 1) can be tested against the back-end part connected to it (2, 3, 4, 5, and 6, respectively, in Figure 1). Therefore, it is possible to test almost the entire internal video path without applying the external signal.

Figure 1 omits the external peripherals, such as external RAM memories, nonvolatile EDID I²C EEPROMs and other peripherals, that can also be tested during post-production self-test. Refer to the Tests of Peripherals section for further information.

TESTS OF PERIPHERALS

I²C, \overline{CS} , \overline{RESET} AND \overline{RESET} ASSERTION TEST

I²C, \overline{RESET} , and \overline{CS} lines (if they exist on a particular part) can be tested by reading back an I²C register, such as Chip Revision Code (in the case of the [ADV7611/ADV7612/ADV7619](#), the RD_INFO register is accessible through the IO map).

1. When \overline{CS} is high or \overline{RESET} is low, the part does not give an I²C acknowledge.
2. Accessing I²C registers, such as RD_INFO, is possible after releasing \overline{RESET} and asserting \overline{CS} .
3. Testing of the \overline{RESET} line can be done by writing a value X to a selected R/W register and checking if value of the register is reset to default after asserting and deasserting the \overline{RESET} . For example, in the case of ADV7612, a register CP_SLAVE_ADDR (a programmable I²C slave address for CP map), write 0x40 and ensure that resetting sets the register to its default value of 0x00.
4. Similarly, the \overline{CS} line can be tested by checking that the part does not respond to I²C writes when \overline{CS} is set low. This is important when the system features many I²C devices using the same I²C address.
5. When read back, if the value of the RD_INFO register is other than expected, then an incorrect device has been soldered onto the board.

This procedure can be used also to verify ALSB pin functionality. The ALSB allows setting of the LSB (least significant bit) of the address of the device main I²C map address. Proper detection of two different addresses set by ALSB confirms proper ALSB functionality.

Note that the \overline{RESET} pulse should be at least 5 ms long (refer to the Timing Characteristics section of the relevant data sheet).

SPI MASTER INTERFACE

Parts featuring an EDID replicator (such as the [ADV7842](#), [ADV7844](#), [ADV7850](#), and [ADV7630](#)) with the SPI master interface can verify external SPI EEPROM memory using I²C writes. The I²C command EDID_STORE writes the contents of data stored in internal EDID map to external SPI memory. The I²C command EDID_LOAD reads the data from external SPI memory into an internal EDID memory map.

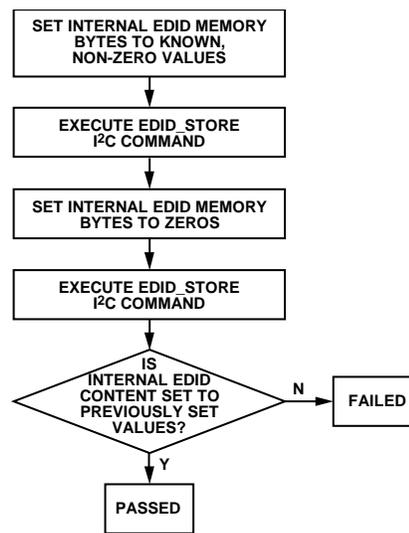


Figure 4. Algorithm Testing External SPI EDID

Refer to the I²C maps and the EDID replicator section of the appropriate hardware user guide.

The quick test of the SPI master interface for devices containing EDID replicator (like [ADV7630](#)) can be done by programming and reading back the contents of EEPROM. The EDID-replication capable device (like [ADV7630](#)) should indicate an error when the write-read fails.

XTAL TEST

The proper clock signal provided from XTAL or the oscillator is critical for any application. When the part lacks a clock source, the I²C slave machine still works in the majority of ADV parts.

The lack of a proper clock signal, however, can easily be detected in video decoders and HDMI receivers and transceivers. In those parts, the STDI block, relying on XTA, will not function properly resulting in invalid readbacks. HDMI-parameters block existing HDMI receivers, and transmitters will not work properly.

An incorrect frequency of /Osc. clock can be detected on HDMI parts using TMDSFREQ which measures the frequency of an incoming HDMI stream using XTAL as a reference. To test for the proper frequency of the crystal, an HDMI receiver or transmitter can be supplied with the incoming HDMI stream of known frequency (for example, 148.5 MHz is standard for 1080p60). The TMDSFREQ register accurately reflects the same frequency as long as the crystal is of the proper frequency and the XTAL_FREQ_SEL register is selected properly. Refer to relevant hardware user guide for register details.

Video decoders processing SD-stream (PAL/NTSC/SECAM) do not lock to color burst causing monochrome output when the clock is of an incorrect frequency. They are also likely to misdetect SD video standard.

The test of XTAL frequency on video decoders can be done in a similar fashion to the HDMI test. For component video modes, the video decoder should be provided with a video signal of known resolution and vertical frequency. The STDI register readbacks properly reflect video timing and confirm proper clock frequency of XTAL.

HDMI transmitters (such as [ADV7511](#)) and video encoders (ADV732x, ADV734x, ADV739x) do not use the XTAL clock signal, but they rely on an externally provided pixel clock. Lack of a pixel clock prevents video encoders and HDMI transmitters from outputting video.

BIST TEST FOR EXTERNAL MEMORY

The more advanced video parts containing external memory ([ADV7842](#), [ADV7844](#)) may be tested by using an internal BIST test. The BIST test should be started by an appropriate I²C write. The end of the BIST is signaled by another I²C readable register. Once the test is done, as indicated by an I²C register BIST_DONE message, an additional register readback can be done to determine whether memory is satisfactory.

ADV7800/ADV7802/ADV7842/ADV7844 Memory Test Procedure

The memory BIST on [ADV7842](#) and [ADV7844](#) generates a pseudo-random sequence that is output to the external memory and readback in order to check for errors. A hardware reset is recommended before the memory BIST test is executed.

Assuming that the IO map has an address of 0x40, the AFE map has an address of 0x4C, the SDP Map has an address of 0x90 and SDP_IO has an address of 0x94 (refer to the hardware user guide of [ADV7844/ADV7842](#) on register map addresses) the writes should be carried out in order shown here.

Initialization

40 00 01; Program SDP 4x1
 40 01 00; Program SDP mode
 4C 80 92; SDP recommended write
 4C 9B 01; SDP recommended write
 4C 9C 60; SDP recommended write
 4C 9E 02; SDP recommended write
 4C A0 0B; SDP recommended write
 4C C3 02; Memory BIST initialization
 40 0C 40; Power up ADV7844
 40 15 BA; Enable outputs
 90 12 00; Disable 3-D comb, Frame TBC, and 3DNR
 40 FF 04; Reset memory controller

Wait 5 ms

90 12 00; Disable 3-D comb, Frame TBC, and 3DNR
 94 2A 01; Memory BIST initialization
 94 7C 19; Memory BIST initialization
 94 80 87; Memory BIST initialization
 94 81 4A; Memory BIST initialization
 94 82 2C; Memory BIST initialization
 94 83 0E; Memory BIST initialization
 94 84 94; Memory BIST initialization
 94 85 62; Memory BIST initialization
 94 7D 00; Memory BIST initialization
 94 7E 1A; Memory BIST initialization

Wait 5 ms

94 D9 D5 Enable BIST test

90 12 05 Enable Frame TBC and 3-D comb test results

Result of BIST test can be read back from following registers:

- SDP_IO Map Register 0xDB[4]—Test completed if this bit is 1
- SDP_IO Map Register 0xDB[5]—Test failed if this bit is 1

Once enabled, the memory test runs endlessly in the loop testing different values. At the end of each iteration of loop registers: test completed and test failed is updated. If during any iteration an error is detected, the test failed register will be set high until the reset is forced or until the complete memory test is run again. It is recommended to allow test memory to run for at least 200 ms.

ADV7186 Memory Test Procedure

The [ADV7186](#) provides external memory test capabilities. Refer to the [ADV7186](#) documentation for more details.

ADV7850 DDR2 Memory Test Procedure

The [ADV7850](#) memory test procedure is outlined in the [ADV7850](#) Hardware Manual. Refer to the DDR2 BIST TEST discussion.

ADV8003 Memory Test Procedure

The [ADV8003](#) relies on the external memory to provide advanced video processing options. Those parts provide memory test. Refer to the [ADV8003](#) documentation for details.

TESTING OF VIDEO DATA OUTPUT

Video Decoders and HDMI Receivers

The basic video output test on video decoders and HDMI receivers can be done by forcing free-run (refer to the appropriate user guide). The Free Run outputs a flat video pattern of a chosen color (8-bit per channel, MSB-aligned) with accompanying synchronization signals. Each video part that contains component processor core (CP core) contains Free-Run features.

The [ADV7401](#), [ADV7403](#), [ADV7611](#), [ADV7612](#), [ADV7619](#), [ADV7604](#), [ADV7622](#), [ADV7623](#), [ADV7800](#), [ADV7802](#), [ADV7842](#), [ADV7844](#), and [ADV7850](#) parts have the bits listed here related to free run functionality.

- CP_FORCE_FREERUN bit in CP map (0xBF[0])
- CP_DEF_COL_AUTO bit in CP map (0xBF[1]),
- CP_DEF_COL_MAN_VAL bit in CP map (0xBF[2])
- DEF_COL_CHA in CP map (0xC0[7:0])
- DEF_COL_CHB in CP map (0xC1[7:0])
- DEF_COL_CHC in CP map (0xC2[7:0])

The CP_FORCE_FREERUN bit set to 1 forces free run output. When CP_DEF_COL_MAN_VAL is set to 1 and free run is output, the color output color is set by registers DEF_COL_CHA[7:0], DEF_COL_CHB[7:0], DEF_COL_CHC[7:0]. The video format of free run is determined by the VID_STD and PRIM_MODE parameters located in the first two bytes of IO map of respective part.

In the case of HDMI Rx parts, setting PRIM_MODE = 4 (graphics) and VID_STD = 8 should produce video resolution of 640x480 at 60 Hz. However, settings PRIM_MODE = 5 (component) and VID_STD = 0x5 outputs 1080i60 (refer to the Recommended Settings for HDMI Inputs table in [UG-237](#)).

In the case of parts not supporting HDMI input, PRIM_MODE = 1 and VID_STD = 5 should output 1080i60, and PRIM_MODE = 2 and VID_STD = 8 should result in 64 × 480p. The backend output of the part should be programmed as it is done in standard scripts; [ADV7401](#), [ADV7403](#), [ADV7611](#), [ADV7612](#), [ADV7619](#), [ADV7604](#), [ADV7800](#), [ADV7802](#), [ADV7842](#), and [ADV7844](#) output video via a standard output pixel bus (requires enabling output, setting OP_FORMAT_SEL, OP_CH_SEL, and so on; refer to standard scripts).

Parts such as [ADV7622](#), [ADV7623](#), and [ADV7850](#) output video through embedded HDMI Tx (requires additional writes as done in standard scripts).

Listing 1. [ADV7611/ADV7612/ADV7619](#) Free-Run Script Setting 1080p60 Output

```

98 FF 80 ; I2C reset
98 FD 44 ; CP
98 00 1E ; VID_STD = 1080P60 @ 60Hz
98 01 05 ; Prim_Mode = 101b HDMI-COMP
98 03 42 ; 36 bit SDR 444 Mode 0
98 05 28 ; AV codes off
98 0B 44 ; Power up part
98 0C 42 ; Power up part
98 14 7F ; Max drive strength
98 15 80 ; Disable tristated
98 19 83 ; LLC DLL phase
98 33 40 ; LLC DLL enable
44 BA 01 ; Set HDMI Free-Run
44 BF 17 ; FORCE FREE RUN; Manual color settings
44 C0 00 ; Manual color: Green channel
44 C1 00 ; Manual color: Red channel
44 C2 A0 ; Manual color: Blue channel
44 C9 05 ; Disable auto-buffering of free-run parameters
    
```

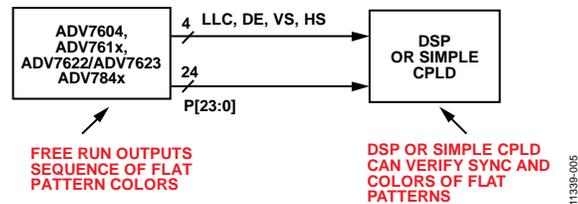


Figure 5. Forcing a Particular Color Through Free Run Checks the Video Pixel Bus Connection

Video Encoders

Video encoders, such as [ADV7340](#), [ADV7341](#), [ADV7342](#), [ADV7343](#), [ADV7391](#), [ADV7392](#), and [ADV7393](#) allow the output of video test patterns. In order to output video patterns, the encoder must be provided with a clock and the encoder must have its registers programmed. This mode does not require additional sync information because the video standard can be chosen via the I²C registers.

For a discussion of internal test pattern generation, see the [ADV7340/ADV7341](#) data sheet, the [ADV7342/ADV7343](#) data sheet, or the [ADV7390/ADV7391/ADV7392/ADV7393](#) data sheet.

Standalone HDMI Transmitters and Video DACs

Standalone video HDMI transmitters ([ADV7511](#)) and video DACs do not generate internal video patterns. However, video transmitters, such as [ADV7511](#), as well as HDMI Tx embedded into the [ADV7622](#), [ADV7623](#), and [ADV7850](#) can check the output connection to the HDMI sink using registers such as

- HPD state (0x42[6] main map)
- Monitor sense state (0x42[5], main map)
- PLL lock status (0x9E[4])

HPD state indicates status of the HPD line. Monitor sense state detects termination of the backend device. The PLL lock status indicates the status of PLLs. Locked PLL means that the part is sending video to the downstream HDMI sink; this is possible when video data is provided to the HDMI Tx and a downstream device is properly connected. Refer to the hardware user guides for the [ADV7511](#) for more details.

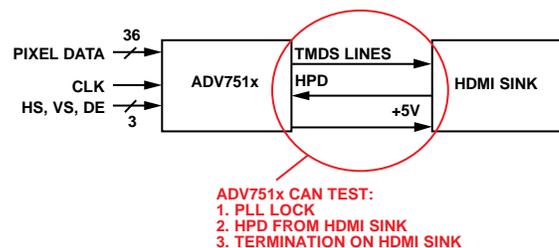


Figure 6. HDMI TX Allow Testing of Connection to a Downstream HDMI Sink

MIPI/DSI Receiver with HDMI Transmitter

The latest generation [ADV7533](#) MIPI/DSI receiver with an HDMI transmitter features a built-in video generator that can generate number of video patterns. Refer to the [ADV7533](#) documentation for more details.

TESTING OF AUDIO DATA OUTPUT

The audio data output of HDMI receivers can only be tested when an HDMI receiver is currently receiving an HDMI stream with embedded audio. Audio control and configuration is discussed in [UG-216](#).

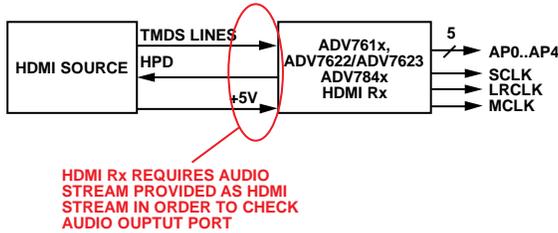


Figure 7. Audio Output Testing Requires HDMI Source

TESTING OF VIDEO INPUT

SD Video Decoders

The SD video decoders feature a detection block that allows detection of incoming video. The Global Status Register description in the [ADV7180](#) data sheet lists registers, such as AD_RESULT, STATUS 1, STATUS 2, and STATUS 3, allowing detection of incoming video stream. All video decoders featuring the standard definition processing core contain such registers.

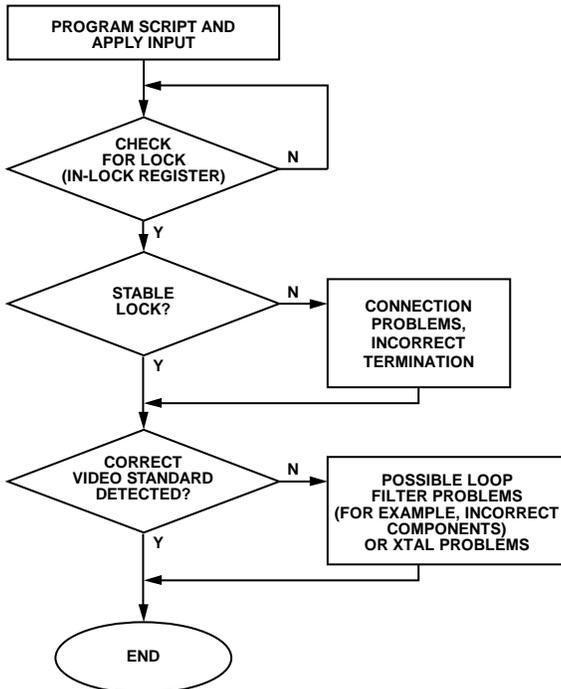


Figure 8. Testing SD Analog Inputs

Refer to the following documentation for more information:

- [ADV7180](#) data sheet for information on autodetection results
- [ADV7184](#) data sheet for information on global status registers
- [ADV7188](#) data sheet for information on global status registers
- [ADV7800](#) and [ADV7802](#) Hardware User Guide for SDP autodetection results
- [ADV7844](#) Hardware User Guide for autodetection of SDP modes

Component Processing Video Decoders and HDMI Receivers

Component processing video decoders ([ADV7401](#), [ADV7403](#), [ADV7844](#), [ADV7842](#), [ADV7850](#)) and HDMI video receivers ([ADV7611](#), [ADV7612](#), [ADV7619](#), [ADV7622](#), [ADV7623](#), [ADV7842](#), [ADV7844](#), and [ADV7850](#)) contain STDI indicating proper synchronization signal lock. The STDI block allows detecting of video standards. It can be used for the HDMI receiver block (if it exists on the part) as well as for component video standards (if such exist on the part). The STDI block uses external crystal and counts the number of lines during vertical sync signal (VS) and, during field, it measures the number of crystal periods in blocks of eight lines as well as the number of clock cycles between successive VS.

Based on readbacks of all STDI values, it is possible to detect the video standard and indicate its consistency (STDI video lock signal). See the [UG-216](#) for information on sync processed by CP, or [UG-214](#) for a discussion on standard detection and identification.

The CP processor also contains CP_LOCK and DE_REGEN_LCK that can be used to trigger an interrupt when two frames have different timing parameters. This can be used to detect any type of video kicks caused by timing inconsistency.

HDMI Measurement Block in HDMI Rx and TRx

The HDMI receivers such as [ADV7610](#), [ADV7611](#), [ADV7612](#), [ADV7619](#), [ADV7842](#), [ADV7844](#), and [ADV7850](#) as well as transceivers and muxes, such as [ADV7622](#), [ADV7623](#), and [ADV7630](#), feature an HDMI parameters measurement block.

The HDMI parameters measurement block provides much more detailed information than the STDI block about the incoming video stream, including the following:

- Cable detection: each of HDMI receivers contain +5 V cable detect registers. See the +5 V cable detect description in [UG-216](#)).
- TMDS clock activity detection. See [UG-216](#) for TMDS clock activity detection information)
- HDMI parameters:
- TMDS frequency

- Exact video parameters (horizontal, vertical sync, front-, back- porches, beginning and end of active region). See the HDMI synchronization parameters in [UG-216](#)).

Note that the registers discussed in this section allow detection of the smallest inconsistencies of an incoming HDMI video stream caused by unstable video sync or TMDS clock frequency.

Standalone HDMI Transmitters

Standalone HDMI transmitters, such as [ADV7511](#), do not provide extensive information about the incoming video stream; however, they offer basic CEA-861 video standards detection that is reported back through the I²C register. Register

Vic Detected, Address 0x3E, in the main map of the above HDMI transmitters provides such information.

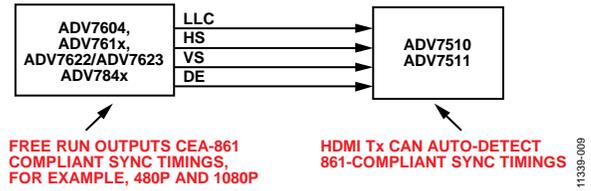


Figure 9. Verification of Proper Sync Connection

It is therefore possible to detect various standards (for example, 720p and 1080p60) coming into HDMI transmitter. Proper detection of such means proper clock and sync connection.

APPENDIX A

Table 1 shows built-in blocks that can be used for automated testing.

Table 1. Built-In Features for Automated Testing

Parts	SD Standard Det.	STDI	HDMI Parameters Block	Free-Run Capability	Basic Incoming VIC Det.	Pattern Generator	BIST for External Memory	External SPI EEPROM	I ² C
Video DACS ADV7123/ADV7125	–	–	–	–	–	–	–	–	–
Video Decoders ADV7180/ADV7182/ ADV7184/ADV7188 ADV7181D ADV7401/ADV7403 ADV7800/ADV7802	Y Y Y Y Y	– Y Y Y Y	– – – – –	Y Y Y Y Y	– – – – –	– – – – –	– – – – –	– – – – –	Y Y Y Y Y
Video Encoders ADV7341/ADV7343/ ADV739x	–	–	–	–	–	Y	–	–	Y
Video Decoders with HDMI ADV7604 ADV7842/ADV7844/ ADV7850	Y Y	Y Y	Y Y	Y Y	– –	– –	– Y	– Y	Y Y
HDMI Receivers ADV7610/ADV7611/ ADV7612/ADV7614/ ADV7619	–	Y	Y	Y	–	–	–	–	Y
HDMI Transceivers ADV7622/ADV7623	–	Y	Y	Y	–	–	–	Y	Y
HDMI Transmitters ADV7511/ADV7511W/ ADV7513 ADV7523/ADV7526/ ADV7528 ADV7533	– – – –	– – – –	– – – –	– – – –	Y Y – –	– – – Y	– – – –	– – – –	Y Y – –

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