

Printed Circuit Board Layout Guidelines for Step-Down Regulators, Optimizing for Low Noise Design with Dual Channel Switching Controllers

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INTRODUCTION

"Noise problem!" Two words every circuit board designer has heard that trigger hours of lab testing time to identify the culprit. Only later to learn that the noise is due to poor layout of the switching power supply. Such problems incur a new layout, schedule slip, and additional development costs. This application note presents printed circuit board (PCB) layout guidelines for avoiding these types of noise problem scenarios. An example switching regulator layout using the [ADP1850](#) dual channel synchronous switching controller begins with identifying the current paths of the regulator. The current paths then determine the placement of the components in this low noise layout design.

PCB LAYOUT GUIDELINES

Identifying Current Paths

In switching converter designs, high current paths and low current paths are all in close proximity. Alternating current (ac) paths carry spikes and noise, high direct current (dc) produces significant voltage drops, and low current paths tend to be sensitive to noise. The key to proper PCB layout is to identify the critical paths and then arrange the components and provide sufficient copper area to avoid high currents from corrupting low currents. Symptoms of poor performance show up as ground bounce and noise injected into the IC and the rest of the system.

Figure 1 shows a synchronous buck regulator design with a switching controller and the external power components: high-side switch, low-side switch, inductor, input capacitor, output capacitor, and bypass capacitor. The arrows in Figure 1 show the flow of the high switching current. It is important to place these power components carefully to avoid unwanted parasitic capacitance and inductance, which cause excess noise, overshoot, ringing, and ground bounce.

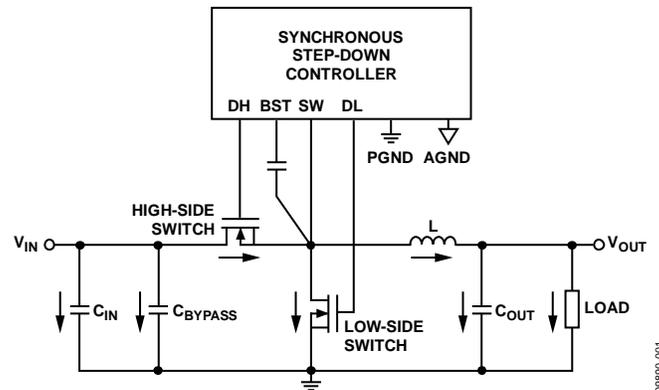


Figure 1. Typical Switching Regulator (Showing AC and DC Current Paths)

Switch current paths, such as DH, DL, BST, and SW, come off the controller and need proper placement to avoid excessive parasitic inductance. These lines carry high $\delta I/\delta t$ ac switching pulse currents that can reach more than 3 A for a few nanoseconds. Keeping the high current loops small is critical to avoid additional noise pickup and minimize output ringing.

Low value, low amplitude signal paths, such as the compensation and feedback components, are noise sensitive. Keep them away from the switch nodes and the power components to avoid unwanted noise injection.

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REVISION HISTORY

5/11—Revision 0: Initial Version

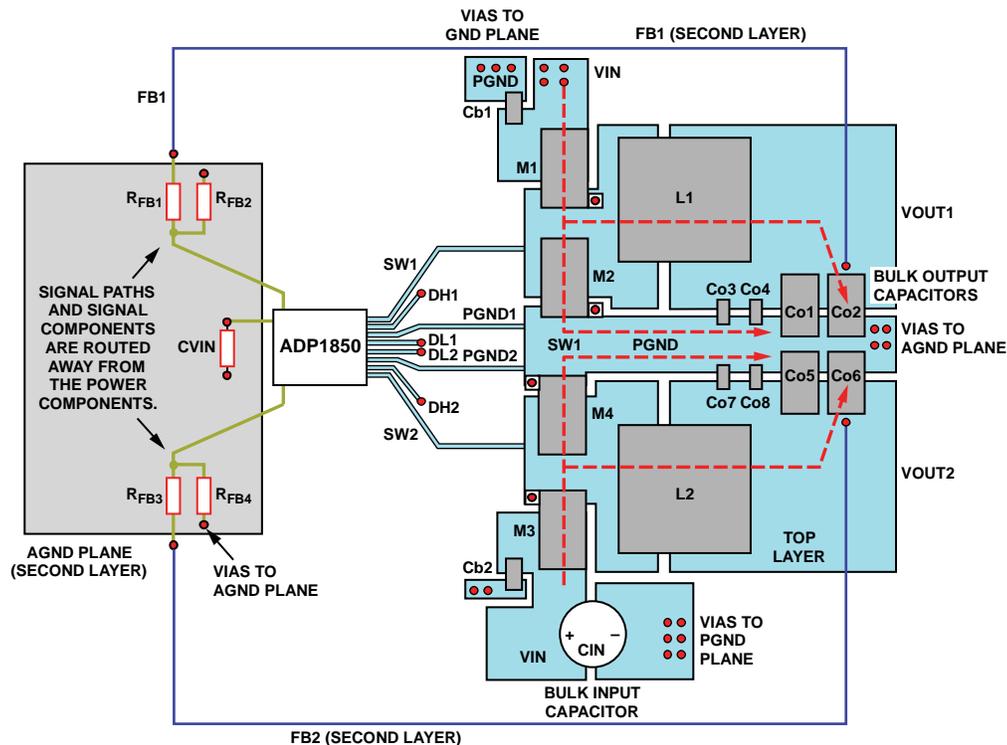
Layout Floor Planning

A PCB floor plan is important to minimize current loop area and arrange the power components so that the current flows smoothly, avoiding sharp corners and narrow paths. This helps reduce parasitic capacitance and inductance, therefore, eliminating ground bounce. Figure 2 shows the PCB layout of a dual output step-down converter using the ADP1850 switching controller. Note that the power component placements minimize the current loop area and any parasitic inductance. The dashed lines indicate the high current paths. This same floor planning technique applies to synchronous and nonsynchronous controllers. In a non-synchronous controller design, a Schottky diode replaces the low-side switch.

POWER COMPONENTS: MOSFETS AND CAPACITORS (INPUT, BYPASS, AND OUTPUT)

The current waveform at the top and bottom power switches is a pulse with very high $\delta I/\delta t$. Therefore, the path to each individual switch should be as short as possible to minimize any noise pickup by the controller and noise transmission from the inductive loop. When using a pair of DPAK or SO-8 package FETs on one side of the PCB, it is best to counter-rotate the two. This allows the switch node to be on one side of the pair and the high-side drain bypassed to the low-side source with a suitable ceramic bypass capacitor. Be sure to place the bypass capacitor as close as possible to the MOSFETs (see Figure 2). This minimizes the inductance around the loop through the FETs and the capacitors.

The placements of the input bypass capacitor and input bulk capacitor are critical for controlling ground bounce. Tie the negative terminal of the output filter capacitor as close as possible to the source of the low-side MOSFET. This helps minimize loop inductance that contributes to ground bouncing. Cb1 and Cb2 in Figure 2 are ceramic bypass capacitors, and the recommended value range for these capacitors is from 1 μF to 22 μF . Add a larger value filter capacitor in parallel for high current applications, as shown by CIN in Figure 2.



- NOTES**
1. LAYER 1: SIGNAL AND HIGH CURRENT PATHS.
 2. LAYER 2: AGND PLANE.
 3. LAYER 3 AND 4: PGND PLANES. M1 AND M2 ARE SUPERSO8 PACKAGES HIGH-SIDE AND LOW-SIDE MOSFETS FOR REGULATOR 1, RESPECTIVELY. SIMILARLY, M3 AND M4 ARE FOR REGULATOR 2. Co1 TO Co8 ARE OUTPUT CAPACITORS. CIN IS THE INPUT BULK CAPACITOR. Cb1 AND Cb2 ARE BYPASS MULTILAYER CERAMIC CAPACITORS (MLCC).

Figure 2. PCB Layout of a Dual Output Step-Down Converter Using the ADP1850 Controller

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THERMAL CONSIDERATION AND GROUND PLANES

The equivalent series resistance (ESR) of the power MOSFETs, inductors, and bulk capacitors contributes to a significant amount of heat generation under heavy load conditions. To dissipate the heat efficiently, the example shown in Figure 2 places large areas of copper under these power components.

A multilayer PCB is better for heat dissipation than a 2-layer PCB. For improved thermal and electrical conduction, use a 2 ounce copper thickness over the standard 1 ounce copper layers. Several PGND planes connected together with vias also help. Figure 3 shows the PGND plane spread over the top, the third layer, and the fourth layer in a 4-layer PCB design.

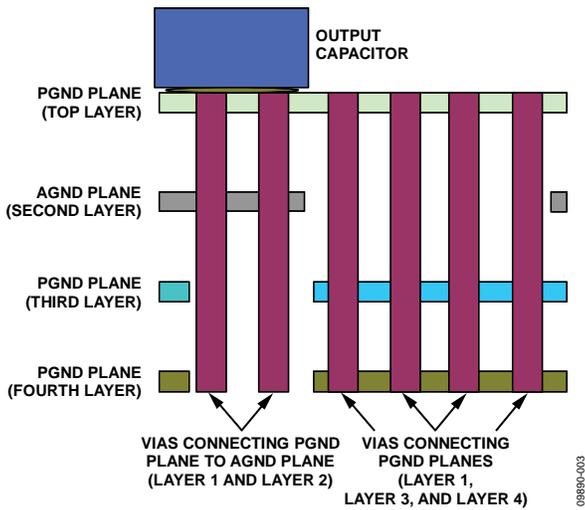


Figure 3. Cross-Section View: Connecting PGND Planes to Improve Heat Dissipation

This multiground plane approach insulates noise sensitive signals. As shown in Figure 2, the negative terminals of compensation components, the soft start capacitor, the bias input bypass capacitors, and the output feedback divider resistors all tie to an AGND plane. Do not directly connect any high current or high $\delta I/\delta t$ paths to the isolated AGND plane. The AGND is a quiet ground plane with no large currents flowing through it.

The negative terminals of all power components, such as the low-side switch, bypass capacitor, and input and output filter capacitors, connect to the PGND plane. The PGND plane carries high current.

The voltage drop within the GND plane could be significant enough to affect the output accuracy. Connecting the AGND plane to the negative terminal of the output capacitors through a wide trace (see Figure 4) significantly improves output accuracy and load regulation.

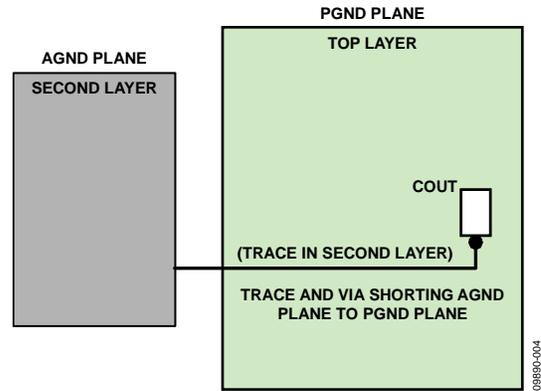


Figure 4. AGND Plane-to-PGND Plane Connection

The AGND plane extends all the way to the output capacitor, where the AGND and PGND planes connect to the vias at the negative terminal of the output capacitor.

Figure 2 shows an alternative technique for connecting the AGND and the PGND planes, where the AGND plane connects to the PGND plane through vias near the negative terminals of the output bulk capacitors. Figure 3 shows the cross-section of a location on the PCB where the AGND and PGND plane connects through vias near the negative terminals of the output bulk capacitors.

CURRENT SENSE PATHS

Proper layout of the current sensing path in current mode switching regulators is important to avoid unwanted noise that causes inaccuracies. Particularly, dual channel applications need more care to avoid any channel-to-channel crosstalk.

The ADP1850 dual channel step-down controller uses the $R_{DS(ON)}$ of the low-side MOSFET as part of the control loop architecture. This architecture senses the current through the low-side MOSFET between the SWx and PGNDx pins. Ground current noise in one channel can couple into the adjacent channel. Therefore, it is essential to keep the SWx and PGNDx traces as short as possible and place them close to the MOSFETs for accurate current sensing. Be sure the connections to the SWx and PGNDx nodes implement the Kelvin sensing technique, as illustrated in Figure 2 and Figure 5. Note that the respective PGNDx trace connects to the source of the low-side MOSFET. Do not arbitrarily connect the PGND plane to the PGNDx pin.

In contrast, for dual channel voltage mode controllers, such as the ADP1829, the PGND1 and PGND2 pins directly tie to the PGND plane with vias.

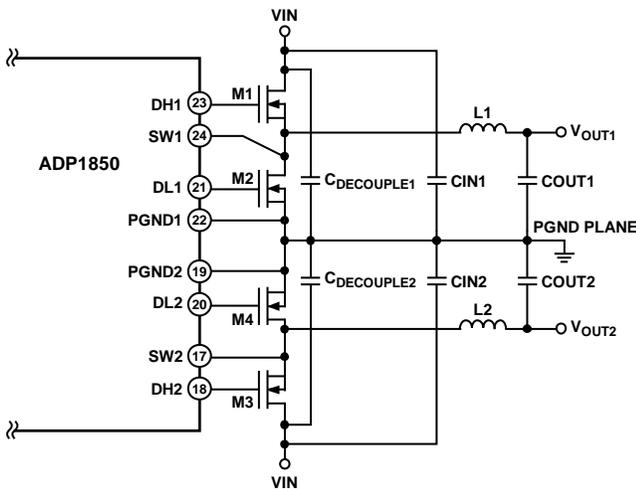


Figure 5. Grounding Technique for Two Channels

FEEDBACK AND CURRENT-LIMIT SENSE PATHS

The feedback (FB) and current-limit (ILIM) pins are low signal level inputs; therefore, they are sensitive to capacitive and inductive noise pickup. Avoid running FB and ILIM traces close to high $\delta I/\delta t$ traces. Watch out for trace routings that form loops that increase unwanted inductance. Adding a small MLCC decoupling capacitor, for example, 22 pF, between ILIM and PGND helps with additional noise filtering.

THE SWITCH NODE

The switch (SW) node is the noisiest place in the switching regulator circuit because it carries large ac and dc voltages and currents. This SW node needs a large area of copper to minimize resistive voltage drops. Place the MOSFETs and inductor close together on a copper plane to minimize series resistance and inductance.

Applications that are more sensitive to electromagnetic interference, switch node noise, and ringing can take advantage of a small snubber. A snubber is a resistor in series with a capacitor (see R_{SNUB} and C_{SNUB} in Figure 6). The snubber that is placed between the SW node and the PGND plane reduces ringing on the SW node and provides a reduced level of EMI. Keep in mind that this addition can slightly reduce the overall efficiency by 0.2% to 0.4%.

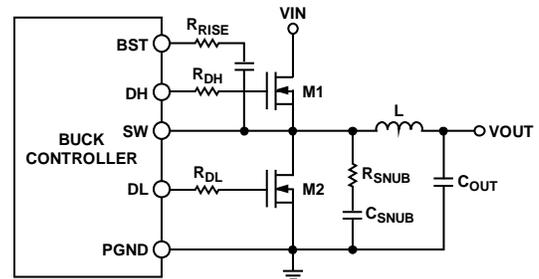


Figure 6. Snubber and Gate Resistance Circuit

GATE DRIVER PATHS

Gate drive traces (DH and DL) also handle high $\delta I/\delta t$ and tend to produce ringing and overshoot. These traces should be as short as possible. It is best to route them directly, avoid using feedthrough vias. If vias are necessary, use two vias for each one to reduce the peak current density and parasitic inductance.

Slowing the gate drive with a small resistor (approximately 2 Ω to 4 Ω) in series with the DH or DL pins also mitigates gate noise and overshoot. Another option is a resistor between the BST and SW pins (see Figure 6). Reserving the space with 0 Ω gate resistors during layout adds great flexibility later during evaluation. The added gate resistance increases the gate charge rise and fall times and thus increases the switching power loss in the MOSFET.

SUMMARY

Understanding the current paths, their sensitivities, and proper placement of the components is key to avoiding noise problems in PCB layout designs. All Analog Devices, Inc. power component evaluations boards implement the presented layout guidelines for best performance. Evaluation board documents, [UG-204](#) and [UG-205](#), provide detail layouts specific to the ADP1850.

Note that all switching power supplies have common components and similar current path sensitivities. Therefore, the guidelines highlighted in the ADP1850 example for a current mode step-down regulator applies directly to voltage mode and/or step-up switching regulator layouts.

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