

Wireless Transmitter IQ Balance and Sideband Suppression

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INTRODUCTION

Direct complex modulation has increasingly become the architecture of choice for implementing transmitter signal chains for end applications, such as cellular base stations, WiMAX, and wireless point-to-point applications. This technique directly modulates the output IQ signals of a digital-to-analog converter onto an RF carrier (direct conversion), which eliminates the need for an intermediate IF stage and the associated filtering. A typical direct conversion transmitter is shown in Figure 1.

It is widely known that during the analog modulation process, gain and phase mismatches of IQ signals have a direct impact on sideband suppression performance. This results in degraded

error vector magnitude (EVM) at the receiver, which in turn degrades the bit error rate (BER).

This application note discusses the major causes of nonideal sideband suppression and discusses design considerations for component selection and PCB design/layout. The wireless transmitter example in this application note consists of an AD9122 TxDAC+ from Analog Devices, Inc., and an analog quadrature modulator, such as the ADL5375, ADL5372, and/or ADRF670x from Analog Devices.

The information provided in this application note also applies to other Analog Devices high speed DAC products, such as the AD9125, AD9148, AD9788, and AD9779A.

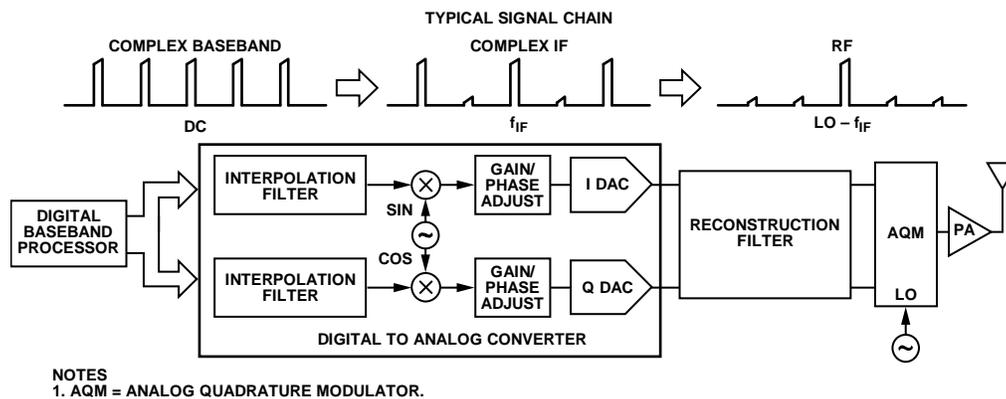


Figure 1. Typical Direct Conversion Transmitter

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REVISION HISTORY

12/10—Revision 0: Initial Version

CAUSES OF NONIDEAL SIDEBAND SUPPRESSION

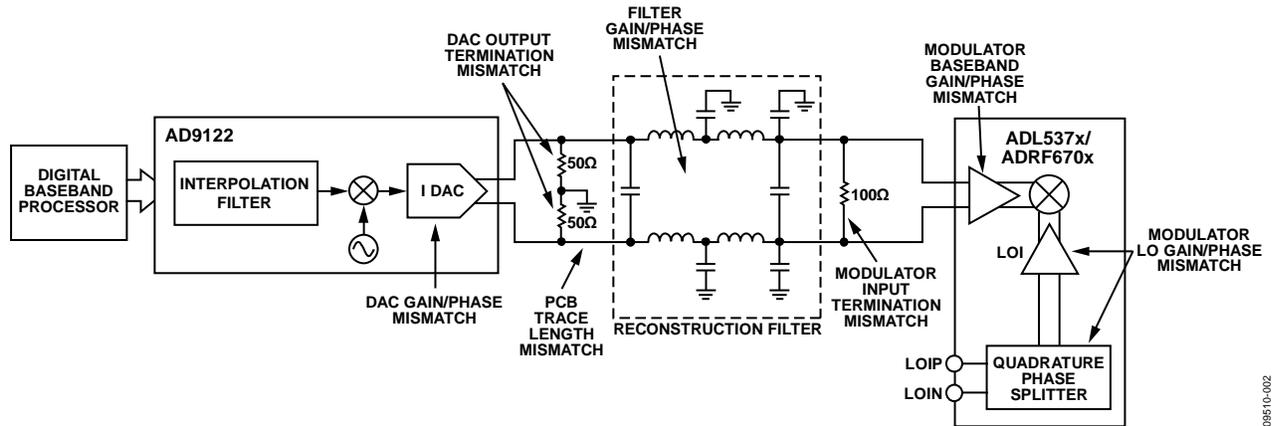


Figure 2. Schematic of Typical Direct-Conversion Transmit Signal Chain

Figure 2 shows the schematic of a typical direct-conversion transmit signal chain. Due to the symmetry of the transmitter, only the I channel is shown in Figure 2.

Potential mismatches are identified in the diagram. IQ signals in the digital domain are assumed to be perfectly matched in this application note. The mismatches to be discussed, by nature, only exist in the analog portion of the signal chain.

Table 1 lists the areas that can possibly cause IQ mismatches. The following sections discuss these potential mismatches and the potential impact.

Table 1. IQ Mismatches in a Typical Direct Conversion Transmitter

Mismatch Contributor	Gain Mismatch	Phase Mismatch
DAC	DAC output gain error	DAC output phase error
IQ MOD	Modulator baseband gain error	Modulator baseband phase error
	Modulator LO gain error	Modulator LO phase error
Reconstruction Filters	Filter gain error	Filter phase error
Termination Resistors	Termination resistor tolerance	N/A
PCB Traces	Differential pair length mismatch	PCB trace length mismatch

DAC Output Gain Error

The DAC output gain error is the difference between the actual and ideal output span. Figure 3 shows a simplified block diagram of the DAC full-scale output current control in the AD9122. The control path consists of a voltage reference, a 10 kΩ external full-scale adjustment resistor, a reference control amplifier, and a current scaling array. The full-scale adjustment resistor and the voltage reference, along with the reference control amplifier, set up the internal bias currents for the DAC.

This bias current is mirrored and multiplied in the current scaling array to set up the full-scale current of the DACs.

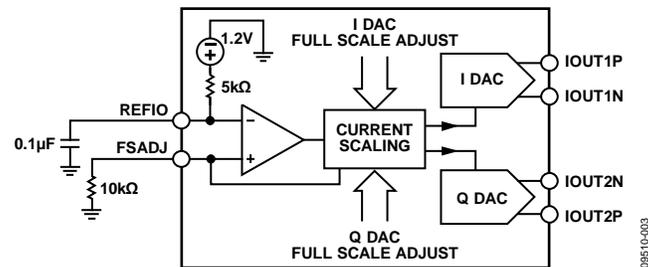


Figure 3. Block Diagram of AD9122 Full-Scale Current Control

Therefore, the ideal DAC full-scale output current can be calculated according to Equation 1.

$$I_{FS} = \frac{V_{REF}}{R_{SET}} \times \left(72 + \left(\frac{3}{16} \times DAC_{GAIN} \right) \right) \quad (1)$$

V_{REF} is the reference voltage. R_{SET} is the full-scale adjustment resistor. DAC_{GAIN} is the digital control code in the current scaling array. A gain error exists if the actual full-scale output current deviates from this ideal value.

The AD9122 data sheet specifies the gain error to be $\pm 3.6\%$ of the full scale, which is the gain error in the worst-case scenario. It includes all variations, such as process, voltage, and temperature. In practice, the gain error between I and Q DAC on the same device is much smaller. I and Q DACs in the same device share the same bias current circuitry, full-scale adjustment resistor, and the reference control amplifier. The variations introduced by voltage and temperature drifts in these blocks track each other on I and Q DACs. The only mismatch exists in geometry variations of the transistors from the wafer manufacturing process in the current scaling blocks. An equation can be formulated to estimate the IQ DAC gain error in the same device, from the analysis described here and from the data sheet specifications.

If the following is denoted

I_{MAIN} is the output current error due to main DAC linearity.

I_{GAIN} is the output current error due to gain DAC linearity.

Then, the IQ DAC gain error can be expressed as

$$G_{DAC} = \frac{\sqrt{I_{MAIN}^2 + I_{GAIN}^2}}{I_{FS}} = \frac{\sqrt{(INL_{MAIN\ DAC} \times LSB_{MAIN\ DAC})^2 + (INL_{GAIN\ DAC} \times LSB_{GAIN\ DAC})^2}}{I_{FS}}$$

Using numbers from the AD9122 data sheet,

$$= \frac{\sqrt{(7.4 \times 0.3 \mu A)^2 + (2 \times 30.9 \mu A)^2}}{19.6 \text{ mA}} = 0.3\%$$

The actual gain error of IQ DACs may vary depending on the device specifications, but the calculation indicates that the IQ gain error of the same device is typically much smaller (an order of magnitude smaller, in this case) than the gain error specified in the DAC data sheet. The result from this calculation is used in the analysis provided in this application note.

DAC Output Phase Error

The DAC output phase error is the skew between I DAC output and Q DAC output when the same input signal is fed into both DACs. This skew comes from mismatches of internal clocking paths and mismatches of the DAC core. Again, the majority of the mismatches come from the wafer manufacturing process. The skew varies from wafer lot to wafer lot and from device to device. This specification is not usually specified in the data sheet. The measurements on the AD9122 indicate that typically the skew is within 20 ps. For an IF output of 150 MHz, the IQ phase error caused by the skew is less than 1°.

IQ Modulator Baseband Gain Error and Phase Error

The baseband gain error and phase error in an IQ modulator is caused by mismatches in the baseband input circuitry, mainly from wafer manufacturing variations. Referring to the [ADL5372](#) data sheet, typically the gain error at 1.9 GHz is 0.09 dB (1%) and the phase error at the same LO frequency is 0.21°.

IQ Modulator LO Gain Error and Phase Error

The LO gain error and phase error are the mismatches between in-phase and quadrature LO signals in an IQ modulator. As shown in Figure 4, the LO input is divided into two quadrature signals, LOI and LOQ, by a quadrature phase splitter. Each quadrature LO signal then passes through a limiting amplifier that provides the mixer with a limited drive signal.

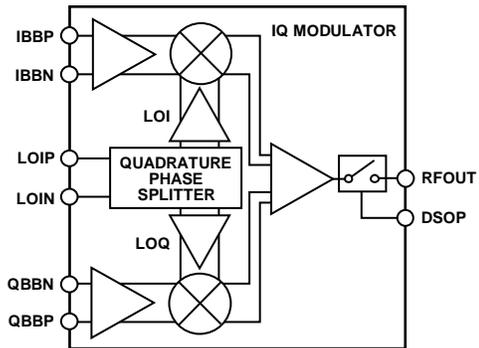


Figure 4. IQ Modulator Functional Block Diagram

The following analysis shows how sideband suppression performance is impacted by gain and phase errors of the LO signal.

If the baseband IQ signals (I_{bb} , Q_{bb}) and LO IQ signals (I_{LO} , Q_{LO}) are denoted as follows

$$I_{bb} = \sin(\omega_{bb}t)$$

$$Q_{bb} = G_{bb} \cos(\omega_{bb}t + \varphi_{bb})$$

$$I_{LO} = \sin(\omega_c t)$$

$$Q_{LO} = G_{LO} \cos(\omega_c t + \varphi_{LO})$$

where:

G_{bb} and φ_{bb} are the amplitude and phase imbalance in the baseband signals.

G_{LO} and φ_{LO} are the amplitude and phase imbalance in the LO signals.

The RF signal at the IQ modulator output can be expressed as

$$RF = I_{bb}I_{LO} - Q_{bb}Q_{LO} =$$

$$\sin(\omega_{bb}t)\sin(\omega_c t) - G_{bb}\cos(\omega_{bb}t + \varphi_{bb})G_{LO}\cos(\omega_c t + \varphi_{LO})$$

Applying trigonometry identities, the undesired sideband signal is

$$RF_{sb} = \frac{1}{2} \{ \cos(\omega_c - \omega_{bb})t - G_{LO}G_{bb}\cos[(\omega_c - \omega_{bb})t + \varphi_{LO} - \varphi_{bb}] \}$$

This shows that the gain and phase error in the LO signals has the same impact on sideband suppression as those in the baseband signals. If assuming the baseband signals are ideal, and the unwanted sideband image power results completely from imbalance in the LO signals,

$$G_{bb} = 1 \text{ and } \varphi_{bb} = 0$$

then, the level of the image power can be calculated using the sideband suppression equation as follows

$$\text{sideband suppression (dBc)} = 10 \log \left(\frac{G_{LO}^2 - 2G_{LO} \cos \varphi_{LO} + 1}{G_{LO}^2 + 2G_{LO} \cos \varphi_{LO} + 1} \right)$$

Thus, LO gain and phase errors are critical merits of an IQ modulator. A good IQ modulator comes with minimal LO gain and phase errors, so that they do not limit the system sideband suppression performance. However, in the system design, close attention must be paid to the quality of the incoming LO signal to achieve the optimal sideband suppression performance. Even with a well-designed IQ modulator, the LO phase error can still be corrupted by an undesired LO signal. Harmonic levels and duty cycle of the LO signal are two critical specifications that have significant impact on sideband suppression. The topology of the quadrature phase splitter determines the desired LO signal the IQ modulator expects to see.

There are two phase splitter topologies widely used in the IQ modulator design: the polyphase splitter and the 2XLO splitter.

Polyphase Phase Splitter

The polyphase phase splitter is an RC-CR phase-shift network, which creates a low-pass transfer function from input to one output and a high-pass transfer function from input to the other output, as shown in Figure 5. If the R and C values of the two polyphase legs are matched, ideally the two outputs are always in quadrature, regardless of the input frequency.

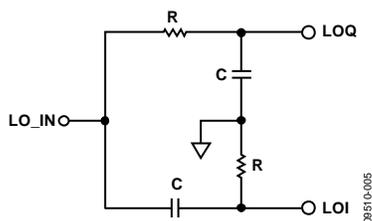


Figure 5. First Order Polyphase Circuit

This phase splitter topology is used in the ADL537x IQ modulators from Analog Devices. Limiting amplifiers are included at the output of the polyphase circuit, as shown in Figure 6, to convert the sinusoidal outputs of the polyphase splitter to square waves. Therefore, in theory, LOI and LOQ outputs are balanced in both phase and amplitude, which are

the ideal switching waveforms needed to drive the modulator mixers.

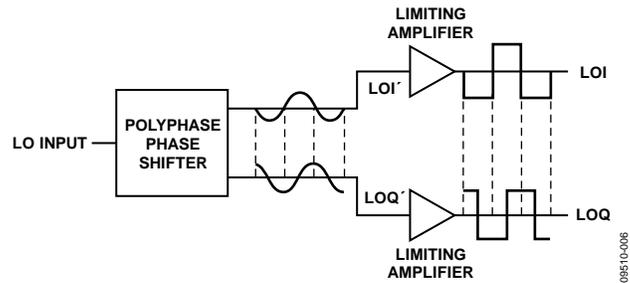


Figure 6. Polyphase LO Phase Splitter

When there are high harmonic contents in the input LO signal, both the LO signal and its harmonics are phase shifted by the polyphase splitter and LOI' and LOQ' outputs contain the phase-shifted version of all the frequency contents. The composite waveform at the output of the phase splitter is a distorted sine wave with zero-crossing points shifted away from perfect quadrature.

Figure 7 shows an example of such output with a 3rd order harmonic of -20 dBc in the LOI signal. Although the limiting amplifier corrects the amplitude distortion, the switching waveform outputs are no longer quadratural. The zero crossings are shifted about 5.5° from their ideal positions. The larger the harmonic components, the larger the phase error in the quadrature LO signals and thus the worse the sideband suppression performance.

Simulation and measurement results show that the odd order harmonics contribute more than the even order harmonics to quadrature error. In order to achieve a sideband suppression performance of -40 dBc or better, all the harmonic contents must be attenuated to below -30 dBc.

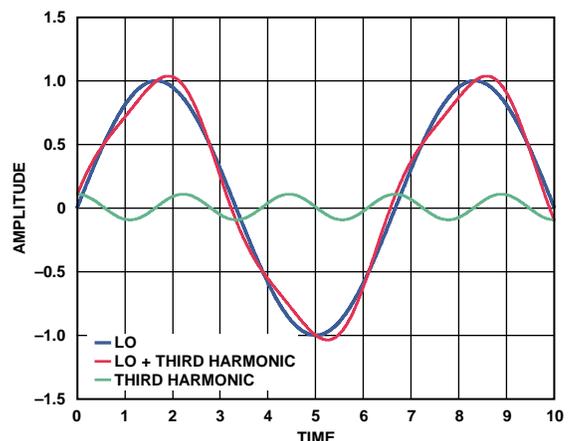


Figure 7. Effect of High Harmonic Content in the LO Signal

Typically in a direct conversion transmitter, the LO signal is generated from a PLL/VCO synthesizer, such as the ADF4007 and ADF4350. It is not unusual that the output of the synthesizer has high harmonic levels. The ADF4350 second harmonic and third harmonic levels are -19 dBc and -13 dBc, as given in the data sheet. A low pass or band pass filter must be

followed to the RF output of the synthesizer to suppress the harmonic components.

For more information on designing a low/band pass filter to sufficiently suppress the LO harmonic levels, refer to the [CN-0134](#) Circuit Note.

2XLO Phase Splitter

Using the 2XLO phase splitter is another approach to generate LO quadrature signals. Figure 8 is a block diagram of this phase splitter topology. Unlike a polyphase phase splitter, it is a digital circuit that uses D flip-flops and an inverter to generate precise quadrature. Due to its digital nature, excellent quadrature can be achieved over a large frequency range.

The circuit requires an input LO operating at twice the frequency of the desired LO. It also requires the duty cycle of this input LO to be 50%. Anything other than a 50% duty cycle at the input translates degree by degree to an LO phase error and, thus, degrades sideband suppression performance.

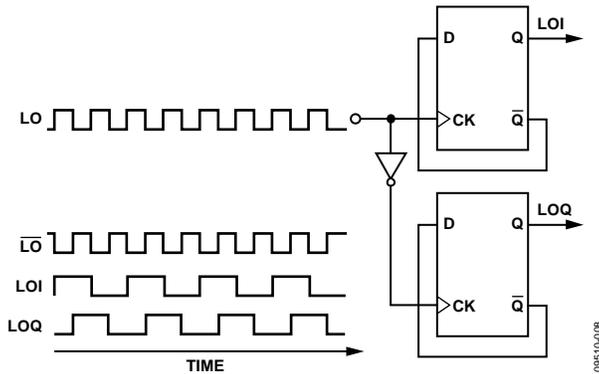


Figure 8. 2XLO Phase Splitter

PLL/VCO synthesizers are designed to generate 50% duty cycle RF signals. However, no design is perfect. A certain amount of duty cycle variation is expected. A component with minimum duty cycle variation over temperature and supply voltage should be selected. The layout of the LO traces is another area that can distort the duty cycle. A mismatch between the positive and negative trace in a differential pair changes the duty cycle of a differential signal. This is described in the PCB Trace Length Mismatch section.

Reconstruction Filter Gain Error and Phase Error

The reconstruction filter is designed to suppress sampling images and other high frequency contents from the DAC. Its design typically allows the signal to pass the filter with minimum amplitude distortion and group delay variation while providing enough suppression on the targeted frequency contents. The pass-band gain and group delay are functions of filter topologies and component values.

Component tolerance and parasitics are dominating factors in the gain and phase errors of the filter. Figure 9 is the schematic of a low-pass filter design on the AD9122 evaluation board (AD9122-M5375-EBZ). There are two 50 Ω DAC termination resistors at the input of the filter and one 100 Ω IQ modulator

input termination resistor at the output. It is a 5th order Butterworth filter with the input and output both matched to 100 Ω.

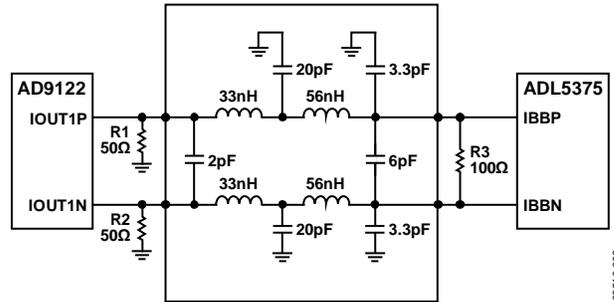


Figure 9. AD9122 DAC Output Reconstruction Filter Schematic

It is apparent that the tolerance of R1, R2, and R3 need to be as tight as possible because mismatches on these resistors directly affect amplitude matching of IQ signals. It is recommended that resistors with <1% tolerance be used for these resistors.

To show how component tolerance affects the filter gain and group delay, Monte Carlo simulations were run to extract those parameters from the worst corners with a 150 MHz IF signal. All the components were assumed to have the same tolerance. The simulations were repeated for 5%, 10%, and 20% tolerance for comparison. The results in Figure 10a and Figure 10b indicate that the standard deviation of the group delay and 3 dB bandwidth is roughly proportional to the component tolerance. The larger the tolerance is, the larger the variations are.

To put the numbers in perspective, in the case of 10% tolerance, there is more than one-third (33%) of a chance that the IQ phase imbalance introduced by the filter is larger than what an AD9122 TxDAC+ introduces. Therefore, loose tolerance is more likely to cause the aggregate imbalance in the signal chain to surpass the compensation range from the DAC. It is recommended that component tolerance with <10% be used for the reconstruction filter.

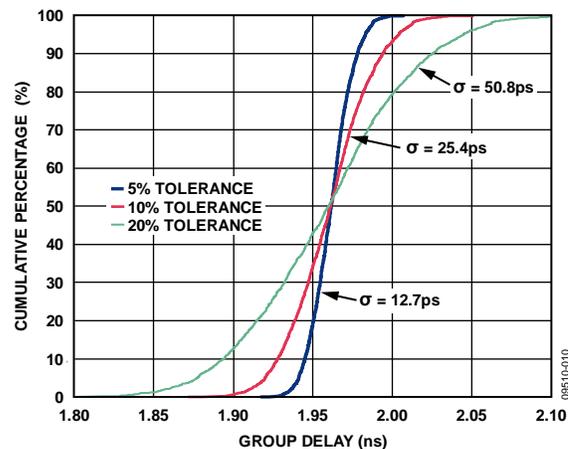


Figure 10a. Reconstruction Filter Group Delay Variation vs Component Tolerance

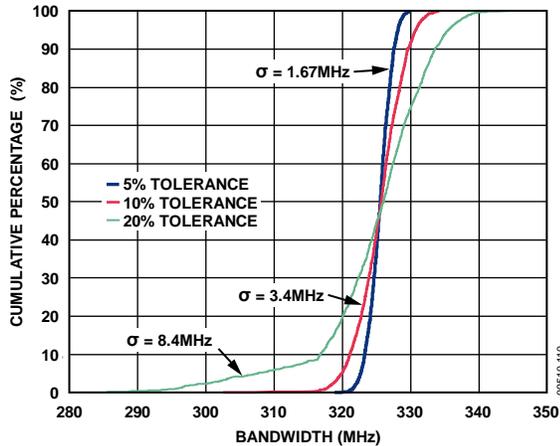


Figure 10b. Reconstruction Filter Bandwidth Variation vs Component Tolerance

PCB Trace Length Mismatch

PCB traces are treated as transmission lines in a high speed board design. Their inductance and capacitance per unit length determines the propagation delay per unit length. This depends on trace width, trace thickness, trace shape, distance of the trace from its reference plane, and the dielectric constant of the board material. Ideally, the traces on the signal path from the DAC output to the modulator input should be symmetrical between the I channel and Q channel and between the positive side and negative side within a channel. In reality, due to variations of PCB design rules and manufacturing limitations, trace lengths are not perfectly matched. The mismatches cause the signal in one channel to be skewed from the other, and, therefore, result in IQ phase errors. Typically there are two types of trace length mismatches as shown in Figure 11.

- Mismatch between I channel and Q channel
- Mismatch between positive and negative side in the same channel

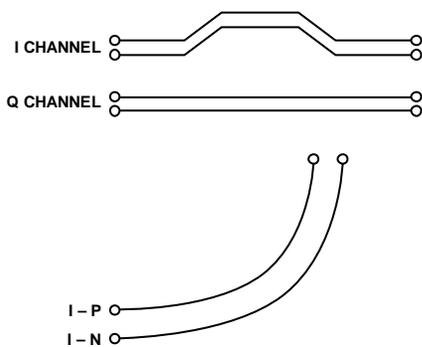


Figure 11. PCB Trace Length Mismatch Examples

Trace mismatches between I and Q channels degrade IQ phase errors. Here one utilizes a widely used rule of thumb for boards made from FR-4 epoxy glass material to estimate the phase error caused by this mismatch. This rule states that a 5 cm (2-inch) long trace introduces 320 ps propagation delay. For a 150 MHz IF signal, a 3 mm (118 mil) mismatch translates to a phase error of about 1° between the I and Q channel.

Mismatches between the positive and negative side in a channel distort a differential signal by skewing the two sides away from 180° out of phase. This causes both gain and phase errors. Typically, the traces in a differential pair are laid out very close to each other. Its potential mismatch is relatively small. However, when the differential pair is long, every time it makes a turn on the PCB, the external trace adds a little bit more in the total length than the internal one. It can accumulate to a certain level where the mismatch starts to have an impact on sideband suppression. Figure 12 shows how a 3 mm (118 mil) mismatch in a differential pair affects zero-crossing points of a 150 MHz IF signal. The zero crossings of the differential signal are shifted about 19 ps, which is 1° of the signal cycle. It is recommended that the matching of the trace length be controlled within ±0.5 mm (±20 mil).

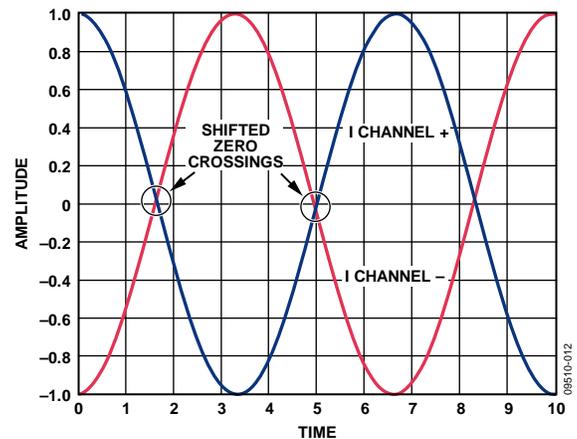


Figure 12. Effect of Trace Mismatch in a Differential Pair

CONCLUSION

While modern high speed DACs and IQ modulators offer excellent out-of-the-box gain and quadrature accuracy, there are other aspects in the system that cause IQ gain and phase imbalance. The sideband suppression performance can be improved using gain and quadrature correction functions provided by the DAC. However, the system must be carefully designed to ensure that the composite errors are within the correction range of the DAC. For more information on calibrating gain and phase errors, refer to the AN-1039 Application Note.

Table 2 summarizes the root causes of IQ gain and phase errors and the design considerations to minimize their effect.

Table 2. Summary of IQ Gain and Phase Errors

Mismatch Contributor	Typical Gain Mismatch	Typical Phase Mismatch
DAC	Determined by the device (< 0.3% for AD9122).	Determined by the device (< 1° for AD9122).
MOD Baseband	Determined by the device (1% @ 1.9 GHz for the ADL5372).	Determined by the device (0.21° @ 1.9 GHz for the ADL5372).
MOD LO	Determined by the device.	Minimized with a clean LO signal.
Reconstruction Filters	Minimized with a flat pass band design and tight component tolerance.	Minimized with a linear phase design and tight component tolerance.
Termination Resistors	Minimized with tight component tolerance.	N/A
PCB Traces	Minimized with good differential pair length matching.	Minimized with good PCB trace length matching.