

## Soldering Recommendations for the Ceramic Vertical Mount Package

by Nitzan Gadish

### INTRODUCTION

Soldering electronic components provides not only electrical connections to those components but also a mechanical connection between the component and the PCB or other substrate. In fact, solder often provides the only mechanical connection holding the component in place.

Mechanical sensors, such as MEMS gyroscopes, are especially sensitive to the mechanical reliability of soldering, as compared with solid state devices. Gyroscopes and other MEMS sensors must be soldered with even more attention paid to their mechanical stability because any movement caused by mechanical instability will be translated to an undesired output signal.

This application note describes soldering recommendations for the ceramic vertical mount package (CVMP). The CVMP can be mounted either vertically (see Figure 1) or lying flat (see Figure 2).

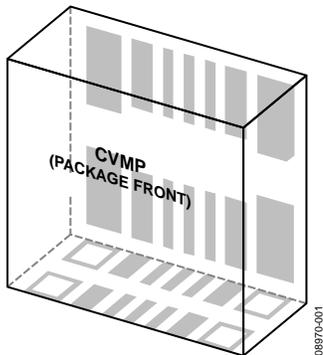


Figure 1. Vertical Mount Package Mounted Vertically

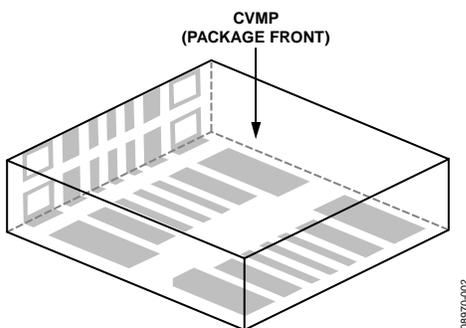


Figure 2. Vertical Mount Package Mounted Horizontally

### SOLDERING THE CVMP PACKAGE

The CVMP package can be soldered using standard reflow techniques. Solder paste is stenciled on using the package footprint. The part is placed, and then the board heated, in accordance with a prescribed temperature profile.

Due to the relatively large mass of the ceramic package, a solder profile (modified from the JEDEC standard temperature profile) is recommended as shown in Figure 3.

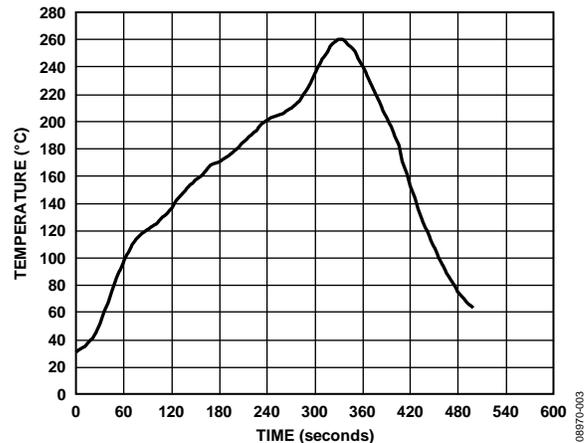
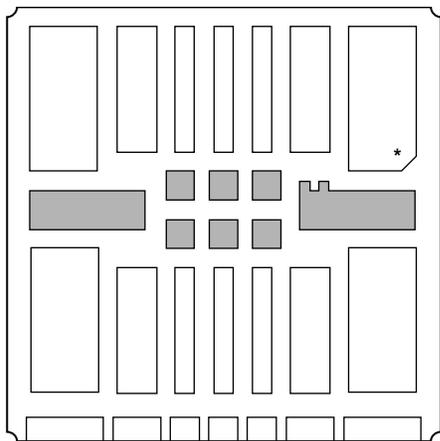


Figure 3. Recommended Solder Profile for CVMP

Solder pad layouts (land patterns) for the CVMP in both vertical and horizontal mounting orientations are provided in the Solder Pad Layouts section of this application note. The land pattern for the backside of the CVMP is shown in Figure 7. Note that there are additional pads on this face of the package (see Figure 4) that are not shown in the land pattern. These pads are used as test points and should not be connected electronically.

**TABLE OF CONTENTS**

Introduction .....	1	Improving Solder Joint Reliability.....	3
Soldering the CVMP Package.....	1	Solder Pad Layouts .....	3

**NOTES**

1. \* INDICATES PIN 1.

08970-004

Figure 4. Backside of CVMP (The pads shaded in gray are test points. Do not connect these test points electronically.)

## IMPROVING SOLDER JOINT RELIABILITY

The effectiveness of a solder process is evaluated using solder-joint reliability, which is a measure of the ability of solder joints to remain in conformance to their mechanical and electrical specifications over a given period of time under a specified set of operating conditions. Mechanical vibration, temperature cycling, or excessive current can have a degrading effect on solder joints.

The embedded leads in the CVMP package provide direct mechanical coupling of the package to the substrate PCB. Unlike other packages, such as SOIC, the CVMP does not have detached leads that provide stress relief; therefore, more stress must be absorbed by the solder joints.

Post-soldering, a narrow space remains between the package and the PCB due to the finite thickness of the solder. It has been shown that filling this space with an underfill material

improves solder fatigue lifetimes by mitigating solder-joint stress in such packages where leads are embedded and do not provide stress relief.

Underfill is a material that is applied following solder reflow to fill the space between the package and the PCB (see Figure 5). It is often applied as a liquid whose very low viscosity allows it to flow into this small gap; it is then cured at a specified temperature. Examples of this material are Dexter's Hysol/FP4531 and Cookson Staychip/3077. Other types of underfill are applied prior to part placement; these flow and cure using a standard solder reflow profile, so no additional cure step is required. One such underfill material is Cookson Staychip/2078E.

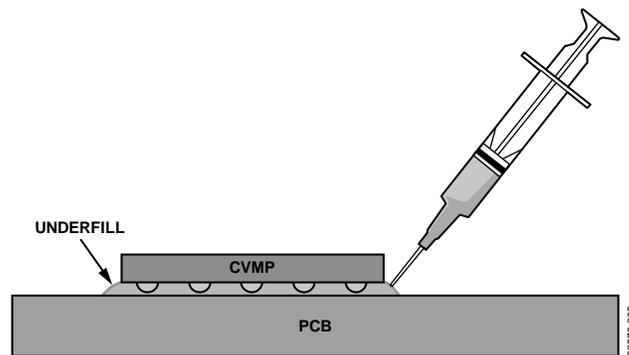
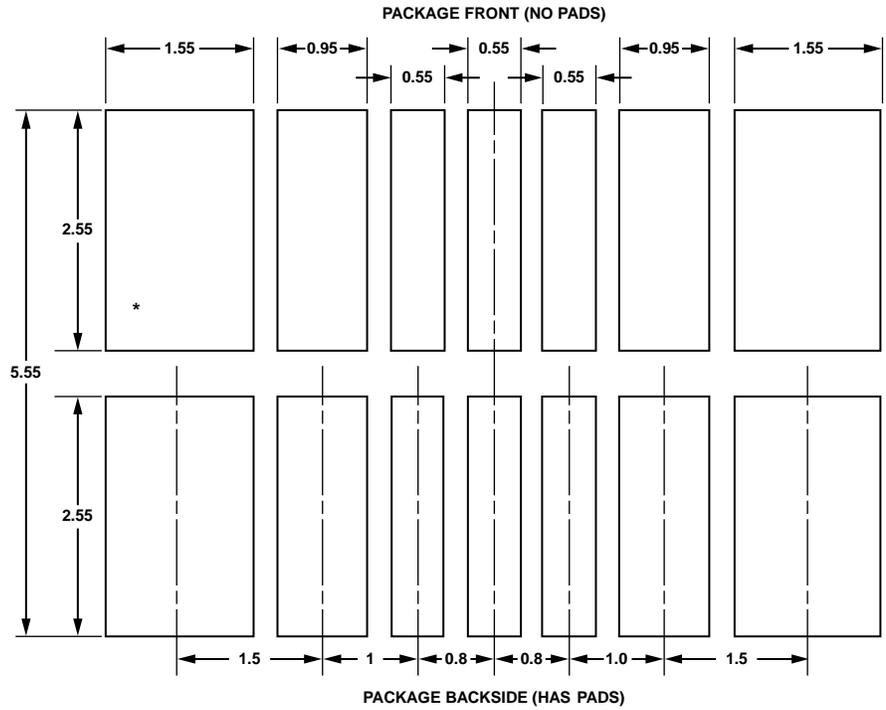


Figure 5. Underfill (This can be applied as a liquid following solder reflow or as a paste or solid prior to placement of the chip onto the PCB.)

## SOLDER PAD LAYOUTS

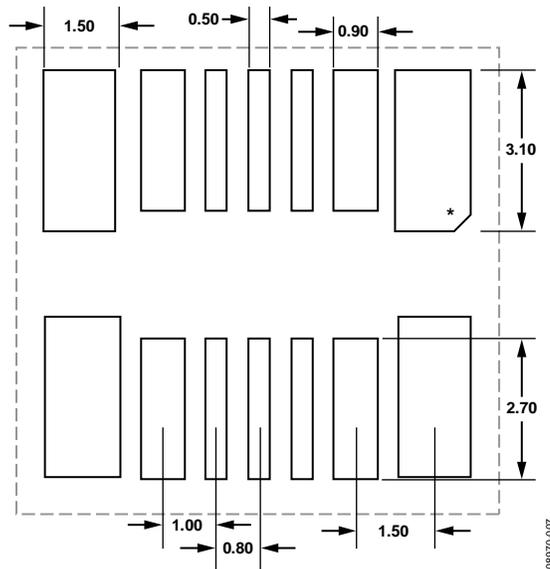
Solder pad layouts (land patterns) for the CVMP in vertical and horizontal mounting orientations are shown in Figure 6 and Figure 7, respectively.



08970-006

**NOTES**  
 1. \* INDICATES PIN 1. THERE IS NO PIN 1 MARKER; PIN 1 IS IDENTIFIED BY PROXIMITY TO THE FRONT OF THE PACKAGE.

Figure 6. Sample Solder Pad Layout (Land Pattern) for Vertically Mounted CVMP; Dimensions Shown in Millimeters



08970-007

**NOTES**  
 1. \* INDICATES PIN 1.

Figure 7. Sample Solder Pad Layout (Land Pattern) for Horizontally Mounted CVMP; Dimensions Shown in Millimeters