A SPICE Op Amp Macromodel for the LT1012
Design Note 28
Walt Jung

Introduction
The Boyle, et al.1, SPICE macromodel for op amps has proven to be quite useful for fast and efficient computer-based IC circuit analysis, used within its limitations. Critics of this type of model point out that it is not optimum for precise transient analysis of amplifiers using complex compensation. On the other hand, the Boyle macromodel may have little match in terms of the computational speed and performance it can achieve, plus how quickly it can be implemented. These virtues are particularly true for lower frequency op amps, or where DC performance parameters are more important.

The Boyle model can be set up to give realistic and quite reasonable working approximations to a variety of IC op amps which use various types of differential transconductance pair front ends. Two fundamental advantages of this model are the relative simplicity and the simulation speed (particularly when a minimum number of junctions are used). Further, the prudent use of the appropriate transistors at the input can simulate real input offset voltage and bias current effects, as well as such IC-unique features as input common-mode clamping2, making the overall model much more realistic and akin to real-world ICs. While the original Boyle paper used an NPN bipolar input example (the 741), the topology of the macromodel is also readily adaptable to PNP bipolars as well as JFETs, as design options.

The LT1012
The LT1012 op amp is a popular “universal” high performance internally compensated precision op amp, available in a variety of electrical grades and packages. It uses a rather unique input stage, comprised of a bias current compensated Super-Beta NPN differential pair. This allows the desirably low drift of an NPN pair to be realized, but with typical bias currents of only 30pA, due to the use of both the Super-Beta process and bias current cancellation. Importantly, the low bias currents are not achieved at the expense of poor drift and high voltage noise, as the LT1012 (C grade) accomplishes a 1μV/°C Max. drift, and a 14nV/Hz1/2 Typ. voltage noise.

The LT1012 has recently been broadened in terms of performance grades, with the addition of a premium “LT1012A” grade part, featuring 25μV Max. VOS, 0.6μV/°C Max. drift, and 500μA Max. supply current. The added “LT1012D” part has a 140μV Max. VOS, a 1.7μV/°C Max. drift, and an 800μA Max. supply current. All device grades have the unusual combination of performance characteristics which allow use as a low-voltage (±1.2V), low supply current micropower op amp as well as a full ±20V supply range general purpose part. The LT1012 actually exceeds the performance of the industry standard OP-07, doing so at 1/20 the bias/offset currents, and 1/8 of the supply current.

The LT1012 Macromodel
While all of the above may be interesting enough to a designer, how the model imitates the real part is more so. The LT1012 macromodel listed in Figure 1 has a number of features worthy of mention. Note that it is based on the LT1012C room temperature typical specs,
taken from the data sheet. \( V_{OS} \), the input offset voltage of the input pair, is modeled by using two slightly different NPN transistor models, \( qm1 \) and \( qm2 \). The ratio of their two saturation currents will produce an offset voltage, which is

\[
V_{OS} = kT/q \ln(I_{s1}/I_{s2})
\]

With the ratio as shown, this produces the typical 10\( \mu \)V offset for the LT1012C.

Bias and offset currents are modeled by using a different \( Bf \) for the two input pair halves, as:

\[
Bf1 = Ic1/Ib1 \quad \text{and} \quad Bf2 = Ic2/Ib2
\]

The \( Bf \) values shown for \( qm1 \) and \( qm2 \) are those which correspond to \( Ib = 30\) pA; \( I_{OS} = 20\) pA. While the gains listed are enormously high (even for Super-Beta transistors) this is not a problem for SPICE, so bias currents in the range of a typical LT1012C are produced.

Other additions to the generic Boyle macromodel are the optional input diode clamps, \( ddm1 \) and \( ddm2 \), as in the real part (they can be deleted, if not used). The substitution of a current source, \( Ip \), in the place of the \( Rp \) of the original model simulates quiescent power supply current. The LT1012, like many modern day ICs, has a quiescent supply current which is quite constant with supply voltage, thus \( Ip \) is more appropriate than a fixed resistor.

The remaining specifications modeled are shown at the head of the listing, consistent with the LT1012C. The model can also be used for the LT1024 (dual LT1012), if the “x” call is added at the end as shown. A sample small signal pulse response waveform of the model is shown in Figure 2, which can be compared to the similar condition scope photo, from the LT1012 data sheet (pg.7).

**References**


**Obtaining This Macromodel**

This model can be entered onto a given computer type simply by typing it in (very carefully!) using an ASCII text editor. Optionally, interested readers may contact LTC at the address or phone number below, for a copy of a PC data disc containing the most recent collection of macromodels (including this model and all those previously released).