

LTM4601A 5V_{IN} to 28V_{IN}, 12A Step-Down μModule Regulator

DESCRIPTION

Demonstration circuit 1414B-A features the LTM®4601A, the high efficiency, high density switch mode step-down power module. The input voltage range is 5V to 20V with a jumper selectable output voltage from 0.6V to 5V. The rated load current is 12A, although derating is necessary for certain V_{IN}, V_{OUT} and thermal conditions. The PLLIN pin supports synchronizing the μModule® regulator to an external clock. The TRACK/SS pin allows the user to program output ramp-up and ramp-down rates which may coincidentally or ratiometrically track with another voltage

rail. Output voltage margining of ±5% from the nominal value is available via the margin control pins MARG0 and MARG1. The LTM4601A data sheet must be read in conjunction with this demo manual prior to working on or modifying demo circuit DC1414B-A.

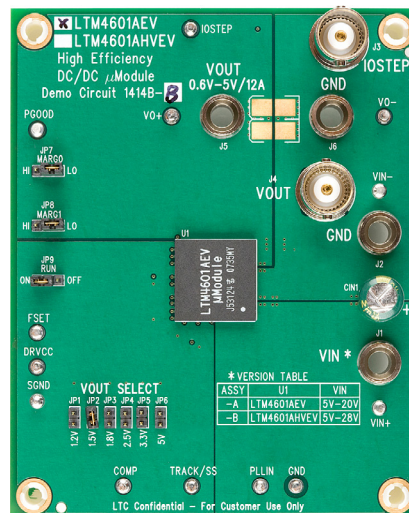
Design files for this circuit board are available.

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PERFORMANCE SUMMARY (T_A = 25°C)

PARAMETER	CONDITION	VALUE
Input Voltage Range		5V to 20V
Output Voltage V _{OUT}	Jumper Selectable (Open for 0.6V)	1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5V
Maximum Continuous Output Current	Derating is Necessary for Certain V _{IN} , V _{OUT} and Thermal Conditions	12A DC
Default Operating Frequency		850kHz
External Synchronous Clock Frequency Range	Please Refer to Data Sheet for Minimum t _{ON} and t _{OFF} Requirement.	600kHz to 1000kHz
Efficiency	V _{IN} = 12V, V _{OUT} = 3.3V, I _{OUT} = 12A	89.5%, See Figure 2

BOARD PHOTO



QUICK START PROCEDURE

Demonstration circuit 1414B-A is easy to set up to evaluate the performance of the LTM4601A. Please refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

1. Place jumpers in the following positions for a typical 1.5V_{OUT} application:

MARG0	MARG1	RUN	V _{OUT} SELECT
LO	LO	ON	1.5V

2. With power off, connect the input power supply, load and meters as shown in Figure 1. Preset the load to 0A and V_{IN} supply to be less than 20V.
3. Turn on the power at the input. The output voltage should be 1.5V ±1%.
4. Once the proper output voltage is established, adjust the load within the operating range and observe the output voltage regulation, ripple voltage, efficiency and other parameters. Output ripple should be measured at J4 with a BNC cable.

5. For optional load transient test, apply adjustable pulse signal between IOSTEP CLK and GND pins. Pulse amplitude sets the current step. The pulse signal should have very small duty cycle (<15%) to limit the thermal stress on the transient load circuit. The output transient current can be monitored at BNC connector J3 (10mV/A).
6. For Margining function test, place jumper MARG0 and MARG1 in the configurations shown in the following table, measure the output voltage at J4.

MARG1	MARG0	ΔV _{OUT}
LO	LO	0
LO	HI	+5%
HI	LO	-5%
HI	HI	0

QUICK START PROCEDURE

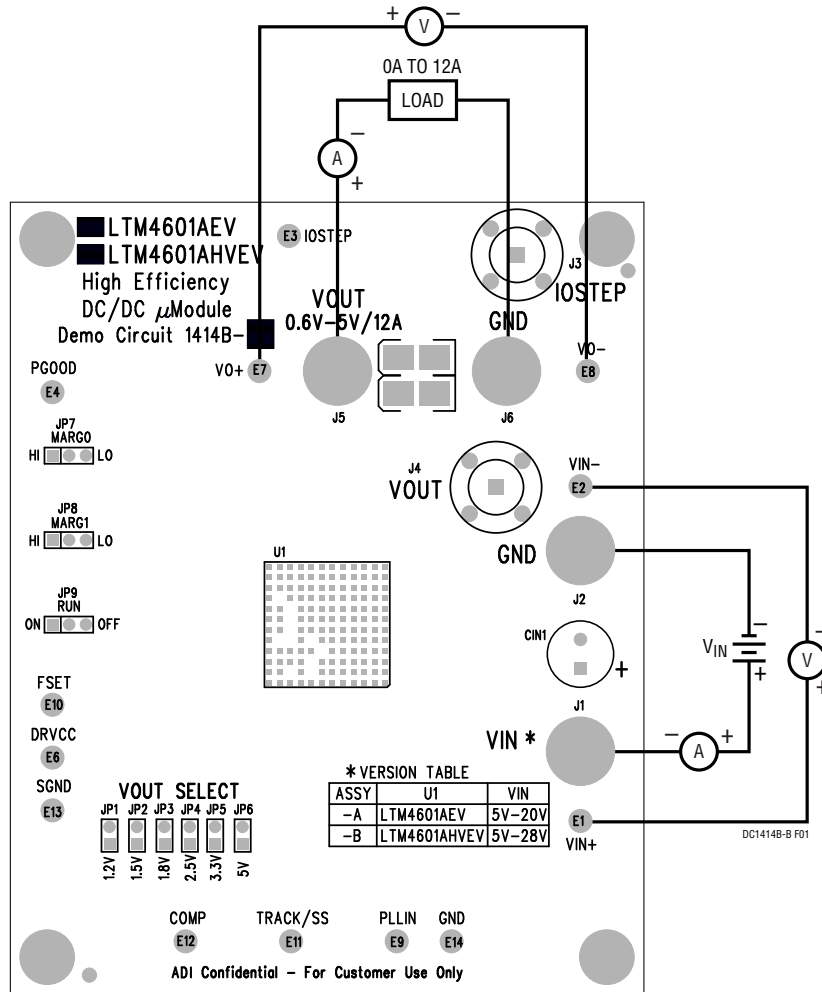


Figure 1. Test Setup of DC1414B-A

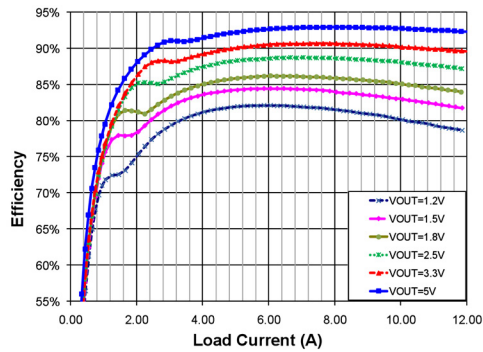


Figure 2. Measured Supply Efficiency with Different V_{OUT} ($V_{IN} = 12V$)

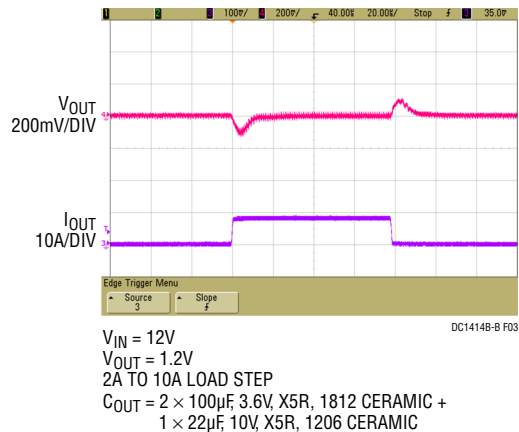


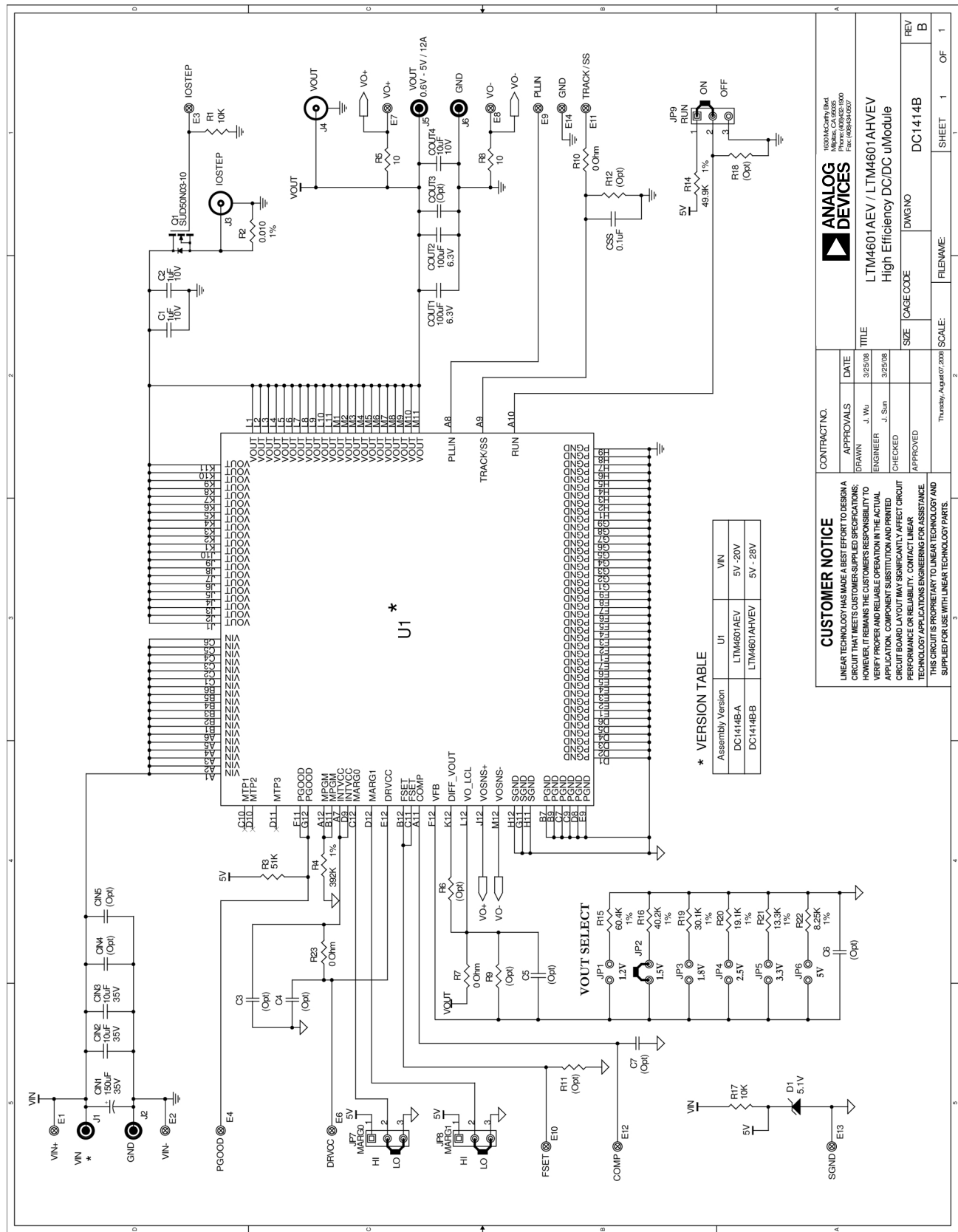
Figure 3. Measured Load Transient Response

DEMO MANUAL DC1414B-A

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	CIN1	Cap., Alum 150µF 35V 20%	SANYO 35ME150WXV+TS (now SUNCON 35ME150WXV)
2	2	CIN2, CIN3	Cap., X7R 10µF 35V 20%	Taiyo Yuden GMK316BJ106ML-T
3	2	COUT1, COUT2	Cap., X5R 100µF 6.3V 20%, 1210/1812	TDK C4532X5R0J107M
4	1	COUT4	Cap., X5R 10µF 10V 10%	Taiyo Yuden LMK316BJ106KL-T
5	1	CSS	Cap., X7R 0.1µF 16V 20%	AVX 0603YC104MAT2A
6	1	D1	Zener Diode, 5.1V	On Semi. MMBZ5231B
7	1	R17	Res., Chip 10k 0.1W 5%	Vishay CRCW060310K0JNEA
8	1	R3	Res., Chip 51k 0.1W 5%	Vishay CRCW060351K0JNEA
9	1	R4	Res., Chip 392k 0.1W 1%	Vishay CRCW0603392KFKEA
10	1	R14	Res., Chip 49.9k 0.1W 1%	Vishay CRCW060349K9FKEA
11	1	R16	Res., Chip 40.2k 0.1W 1%	Vishay CRCW060340K2FKEA
12	1	U1	I.C., Volt. Reg.	Analog Devices LTM4601AEV
Additional Demo Board Circuit Components				
1	0	CIN4, CIN5 (Opt)	Cap., 1206 TBD	
2	0	COUT3 (Opt)	Cap., 1210 TBD	
3	2	C1,C2	Cap., X5R 1µF 10V 10%	Taiyo Yuden LMK107BJ105KA
4	0	C3, C4, C5, C6, C7 (Opt)	Cap., 0603 TBD	
5	1	Q1	MOSFET, N-Channel 30V	Vishay SUD50N03-09P-E3
6	1	R1	Res., Chip 10k 0.1W 5%	Vishay CRCW060310K0JNEA
7	1	R2	Res., LRF, 0.010Ω, 2W, 1%, 2512	IRC LRF2512LF-01-R010-F
8	2	R8, R5	Res., Chip 10Ω 0.1W 5%	Vishay CRCW060310R0JNEA
9	0	R6, R9, R11, R12, R18 (Opt)	Res., 0603 TBD	
10	3	R7, R10, R23	Res/Jumper, Chip 0Ω 1/16W 1 AMP	Vishay CRCW06030000Z0EA
11	1	R15	Res., Chip 60.4k 0.1W 1%	Vishay CRCW060360K4FKEA
12	1	R19	Res., Chip 30.1k 0.1W 1%	Vishay CRCW060330K1FKEA
13	1	R20	Res., Chip 19.1k 0.1W 1%	Vishay CRCW060319K1FKEA
14	1	R21	Res., Chip 13.3k 0.1W 1%	Vishay CRCW060313K3FKEA
15	1	R22	Res., Chip 8.25k 0.1W 1%	Vishay CRCW06038K25FKEA
Hardware-For Demo Board Only				
1	13	E1-E4, E6-E14	Turret, Testpoint	Mill Max 2308-02-00-80-00-00-07-0
2	6	JP1, JP2, JP3, JP4, JP5, JP6	2-Pin 0.079 Single Row Header	SAMTEC TMM102-02-L-S
3	3	JP7, JP8, JP9	3-Pin 0.079 Single Row Header	SAMTEC TMM103-02-L-S
4	4	XJP2, XJP7, XJP8, XJP9	Shunt, 0.079" Center	SAMTEC 2SN-BK-G
5	4	J1, J2, J5, J6	Connector, Banana Jack	Keystone 575-4
6	2	J3, J4	BNC Connector	Connex 112404
7	4		Stand-Off, Nylon, 0.5" Tall	Keystone 8833 (SNAP ON)

SCHEMATIC DIAGRAM



DEMO MANUAL DC1414B-A



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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