ADSP-BF535 Blackfin Processor
High Performance for Networking and Digital Imaging

Key Features

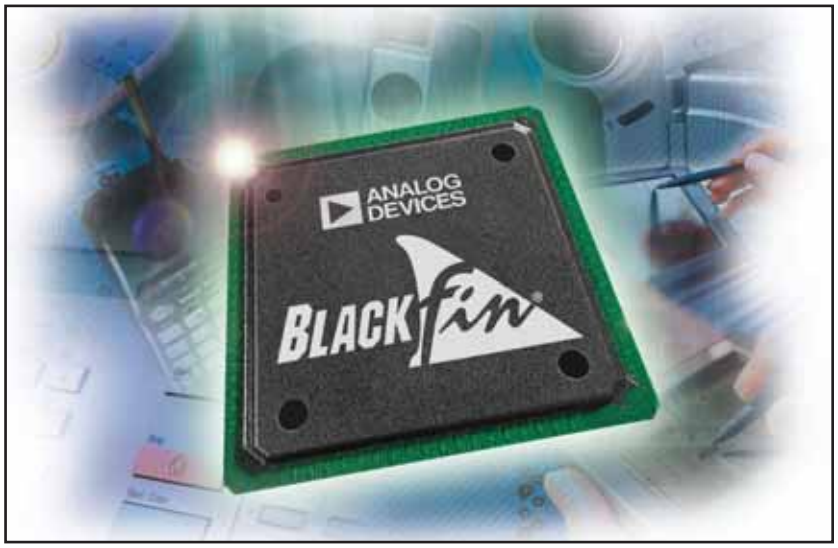
- High performance 16-bit dual-MAC processor core up to 350 MHz
- Flexible, software-controlled Dynamic Power Management
- Optimized RISC instruction set for high code density and programming in C/C++ languages
- Enhanced media instructions to process audio, image, and video for multimedia applications
- Integrated system peripherals, including USP device, PCI, serial ports, UARTs, SPIs, 32-bit timers, and more

Blackfin Processors Utilize

- Single processor core
- Single instruction set
- Single programming model
- Single set of development tools

Target Applications

- Automotive
- Broadband access
- Central office/network switch
- Digital imaging and printing
- Global positioning systems
- Industrial signal processing
- Instrumentation/Telemetry
- Internet appliances
- Modem solutions
- Personal branch exchanges (PBX)
- POS terminals
- Telecommunications
- Video conferencing
- VoIP phone solutions



Blackfin Processor Architecture Highlights

At the heart of the Blackfin® Processor is Analog Devices most advanced 16-bit DSP core architecture. This core, developed jointly by ADI and Intel® Corporation, has three primary objectives:

High Performance
Blackfin Processors employ a dual-MAC DSP that also includes efficient RISC MCU system control functionality and multimedia processing capabilities. All are combined in one simple, optimized instruction-set architecture.

Dynamic Power Management
Blackfin Processors' Dynamic Power Management offers a flexible, software-controlled environment that delivers just the required amount of performance to the processor via independent, dynamic variation of both voltage and frequency. Blackfin Processors also employ a gated clock scheme and multiple power-down modes for minimal power consumption.

Ease of Use
Blackfin Processors employ both an optimized compiler and the architecture to support software development in high level languages (HLL), e.g., C/C++, thus delivering comparable code densities of traditional microcontrollers. The architecture also has embedded features to support efficient use of a Real-Time Operating System (RTOS). Blackfin Processors represent a revolutionary change to the traditional trade-offs that programmers and system architects were forced to make in the past. Blackfin Processors incorporate the world's first truly high performance DSP combined with MCU control functionality into a single architecture that is easy to develop a system around. With Blackfin Processors, OEMs can achieve lower costs and higher performance that will enable the next generation of embedded digital communication and connected media appliances.

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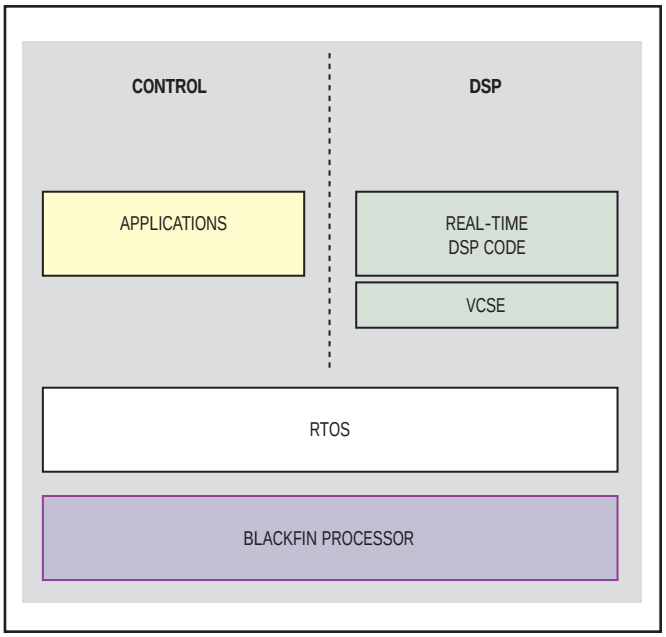
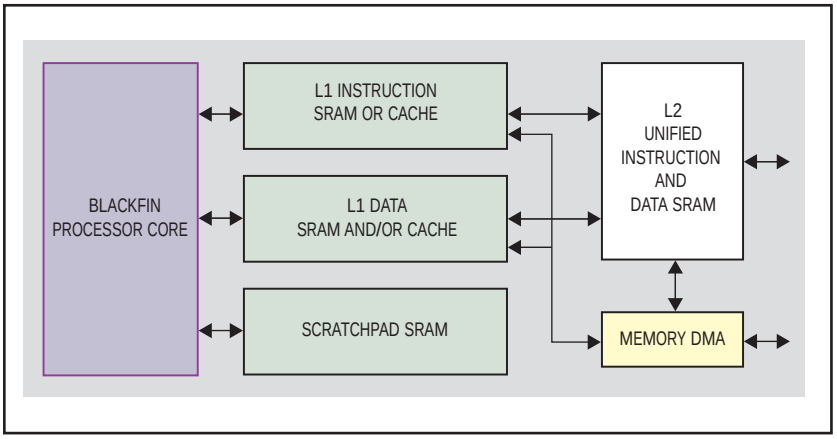
System Development

Blackfin Processors' core performance and architectural partitioning allow for development of a complete, high performance DSP system that could incorporate either ADI's VisualDSP Kernel (VDK) RTOS or many other industry recognized Real-Time Operating Systems—all within a single processor environment. Low latency real-time DSP code can be run on the Blackfin Processor and enhanced by utilizing the expandability and flexibility of VisualDSP Component Software Engineering (VCSE) capabilities now offered in the latest version of VisualDSP++® for Blackfin Processors. Additionally, higher latency control tasks can be simultaneously scheduled and executed, allowing the Blackfin Processor to be at the heart of many embedded systems.



Blackfin Processor system environment.



Blackfin Processor memory hierarchy.

Optimized and Configurable Memory Structure

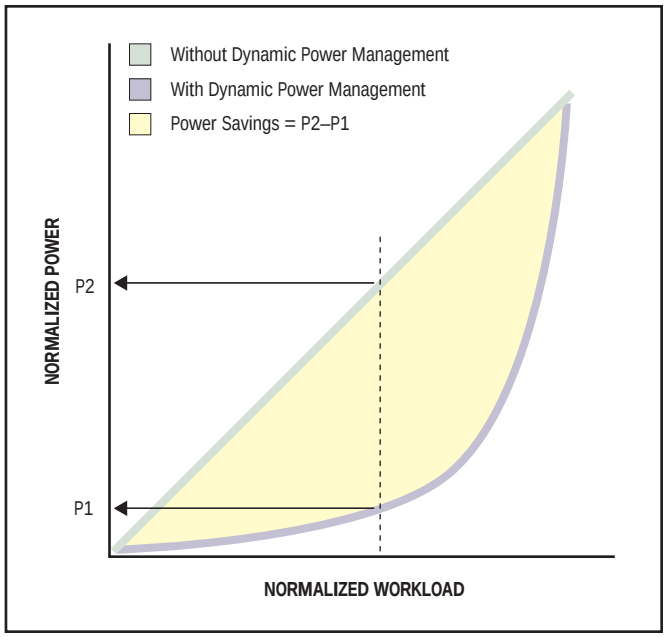
The Blackfin Processor core is a highly parallel, fully interlocked pipeline architecture that allows users to achieve the most work possible per cycle. To complement this, Blackfin Processors utilize a very powerful and flexible L1 and L2 memory hierarchy. Both L1 instruction and data memories can be dynamically configured as SRAM, cache, or a combination—all depending on how the processor core is to be used for a given task. Blackfin Processors can also include an integrated, unified instruction and data L2 SRAM for larger storage needs. Both the L1 and L2 memories are dual-ported so that information can be simultaneously incoming and outgoing for maximum throughput with minimal core processor impact.

Portable Low Power Architecture

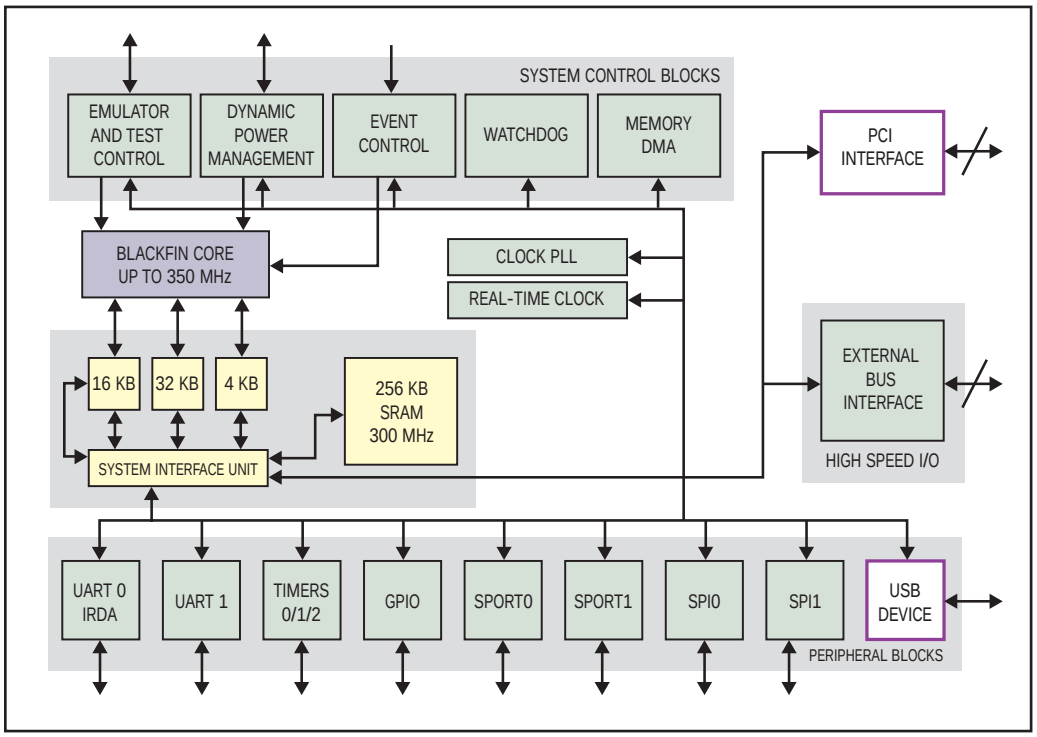
Blackfin Processors use Dynamic Power Management to control critical power consumption and performance parameters, thus allowing system designers to fully optimize the design for the intended application. Blackfin Processors are designed to achieve the most work per cycle to maximize the computational processing power per required mW. Applications may independently vary both frequency of operation and voltage of operation of the processor core, resulting in significantly lower overall power consumption. This translates into longer battery life for portable applications.

System Integration

ADSP-BF535, the first Blackfin Processor, is a highly integrated system-on-a-chip (SoC) solution for the next generation of digital communication and connected media applications. By combining industry-standard communication interfaces with a high performance processor core, OEMs can develop cost-effective solutions quickly and effectively without the need for costly external components. The ADSP-BF535 system peripherals include UARTs, SPIs, serial ports, general-purpose timers, a real-time clock, a watchdog timer, a USB device, and PCI bus interfaces for further peripheral expansion.



Blackfin Processor Dynamic Power Management.



ADSP-BF535 block diagram.

Tools and Support Software

Blackfin Processors are supported by ADI's CROSSCORE® development tools, which include the industry-leading VisualDSP++ development environment, evaluation kits, and emulators. The VisualDSP++ environment consists of a full range of tools such as a C/C++ compiler, linker, debugger, simulator, statistical profiling, the VisualDSP++ kernel, and more. The EZ-KIT Lite™ evaluation system provides an easy way to investigate the power of ADI's family of processors and begin application development. ADI emulators, among other tasks, allow you to load code, set breakpoints, observes variables, observe memory, and examine registers.

Analog Devices also has a large third-party development community, the DSP Collaborative™, supporting signal processing applications. Please consult your ADI representative for selection and availability of products.

ADSP-BF535 Blackfin Processor Features

Core Attributes

- High performance core up to 350 MHz
- Dual 16-bit MAC processor, supporting 700 MMACs of sustained performance
- Two 32-bit ALUs
- Two 40-bit accumulators
- Four 8-bit video ALUs
- Parallel address computational DAGs for circular buffer and bit-reversed addressing support
- 40-bit sifter for bit manipulation and data interleaving
- Flexible, software-controlled Dynamic Power Management
- RISC-like register and instruction model for ease of programming and compiler-friendly support
- Enhanced multimedia instructions for media-rich processing
- Advanced debug, trace, and performance monitoring support

Memory

- 768 MBytes unified address memory map
- 308 KBytes of on-chip memory
  - 16 KBytes of dual-ported L1 instruction SRAM/cache
  - 32 KBytes of dual-ported L1 data SRAM/cache
  - 4 KBytes of high speed Scratchpad SRAM
  - 256 KBytes of full speed, low latency, dual-ported L2 SRAM
- Memory management unit providing memory protection
- Memory controller providing glueless connection to multiple banks of SDRAM, SRAM, FLASH, or ROM
- Flexible memory initialization capability (boot from SPI, serial port, external memory source, or second-stage PCI load)

Peripherals

- 32-bit 33 MHz PCI V2.2 compliant bus interface with both master and slave support
- USB device V1.1 compliant controller supporting up to eight endpoints
- Event handler
- Two UARTS with auto baud capability (one UART includes support for IrDA®)
- Four 32-bit timer/counters—three of which support PWM, pulsewidth, and event count modes
- Two SPI® compatible ports
- Two dual-channel, full-duplex synchronous serial ports (SPORTs)
- 12-channel DMA controller and memory DMA controller capable of internal, external, and PCI transfers
- Real-time clock
- Watchdog timer
- 16 general-purpose I/Os
- Debug/JTAG interface
- On-chip PLL capable of 1x to 31x frequency multiplication

Other

- 1.0 V–1.6 V core V_{DD} with 3.3 V I/O V_{DD}
- Four device offerings:
  - 350 MHz Commercial Temperature ADSP-BF535PKB-350
  - 300 MHz Commercial Temperature ADSP-BF535PKB-300
  - 300 MHz Industrial Temperature ADSP-BF535PBB-300
  - 200 MHz Industrial Temperature ADSP-BF535PBB-200
- 260-lead (19 mm x 19 mm) PBGA package

CROSSCORE Development Tools

- VisualDSP++
  - VisualDSP Kernel (VDK) RTOS
  - VisualDSP Component Software Engineering (VCSE)
- ADSP-BF535 EZ-KIT Lite
- PCI and USB based emulators

Embedded Processing Support

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