Hittite has developed an industry-leading line of high performance clock distribution and clock generation products that enable the system designer to maximize the performance from data converters and physical layer (PHY) components.
Hittite Core Competencies in Clock & Timing ICs:

Clock Generation
- Programmable Output Frequencies for Flexible Frequency Planning
- Industry Leading Phase Jitter of <80 fs RMS
- Advanced Phase Noise Spur Reduction Technique to Reduce Noise Sensitivity

Clock Management
- Jitter Attenuation of Backplane Clocks Up to 3 GHz
- Fractional-N Frequency Generation Using Proprietary Delta-Sigma Modulation Technique
- Exact Frequency Mode to Generate Clocks with 0 Hz Error

Clock Distribution
- Clock Trees with Negligible Additive Jitter & Low Propagation Delays
- Best-in-Class Phase Noise Floor of <-165 dBC/Hz
- Clock De-Skew & Delay Management

Across All Markets:
Our SMT packaged clock generators operate up to 3 GHz, and are ideal for a wide range of high performance cellular/4G infrastructure, fiber optic and networking applications, and deliver best-in-class jitter and industry-leading phase noise floor. Hittite's configurable Clock & Timing ICs offer flexibility in frequency planning and system design. In communications applications, low jitter clock ICs improve link Bit Error Rate (BER) and eye diagram performance for higher bandwidth communication interfaces. In control applications, Hittite's proprietary Fractional-N clock generation architecture allows for configurable frequencies. Similarly, in sensors and entertainment applications, clock generation and distribution devices facilitate clock trees that support multiple frequencies to address system-wide synchronization challenges.

Hittite Heritage:
Hittite has broad engineering expertise in high frequency PLL, VCO and signal amplifiers. As bandwidth requirements increase, the clock speeds that are required to synchronize data converters and PHY components increase as well. Hittite's focus on innovation in high frequency building blocks enable the industry leading Clock & Timing IC products that meet the demands of next generation designs.
CLOCK & TIMING ICs

Clock Distribution

<table>
<thead>
<tr>
<th>Max. Clock Rate (GHz)</th>
<th>Function</th>
<th>Input</th>
<th>Output</th>
<th>Phase Jitter (12 k to 20 MHz)</th>
<th>Rise/Fall Time (ps)</th>
<th>Channel Skew (ps)</th>
<th>Disable Mode</th>
<th>Power Supply (V)</th>
<th>Package</th>
<th>ECCN Code</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>Clock Divider &amp; Delay Management</td>
<td>LVPECL, LVDS, CML, CMOS</td>
<td>LVPECL</td>
<td>13 fs RMS</td>
<td>90</td>
<td>300 to 1500</td>
<td>Yes</td>
<td>5 or 3.3</td>
<td>LP3</td>
<td>3A001.a.11.b</td>
<td>HMC988LP3E</td>
</tr>
<tr>
<td>8</td>
<td>1:9 Fanout Buffer</td>
<td>LVPECL, LVDS, CML, CMOS</td>
<td>LVPECL</td>
<td>8 fs RMS</td>
<td>65</td>
<td>3.1</td>
<td>Yes</td>
<td>3.3</td>
<td>LP5</td>
<td>3A001.a.11.b</td>
<td>HMC987LP5E</td>
</tr>
</tbody>
</table>

Clock Generators

<table>
<thead>
<tr>
<th>Max. Frequency (MHz)</th>
<th>Function</th>
<th>Typical Phase Jitter (fs RMS)</th>
<th>Phase Noise Floor (dBc/Hz)</th>
<th>Maximum Reference Freq. (MHz)</th>
<th>Typical Power Consumption (W)</th>
<th>Figure of Merit (Frac/Int) (dBc/Hz)</th>
<th>Package</th>
<th>ECCN Code</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>500</td>
<td>Integer Mode PLL (x1, x5, x10)</td>
<td>Defined by VCXO</td>
<td>Defined by VCXO</td>
<td>140</td>
<td>0.0064</td>
<td>-208</td>
<td>MS8</td>
<td>EAR99</td>
<td>HMC1031MS8E</td>
</tr>
<tr>
<td>350</td>
<td>Clock Generator with Fractional-N PLL+VCO</td>
<td>116 / 75</td>
<td>-165</td>
<td>350</td>
<td>0.86</td>
<td>-227/-230</td>
<td>LP6G</td>
<td>3A001.a.11.b</td>
<td>HMC1032LP6GE</td>
</tr>
<tr>
<td>550</td>
<td>High Performance +3.3 V Clock Generator</td>
<td>99</td>
<td>-163</td>
<td>350</td>
<td>0.64</td>
<td>-226/-227</td>
<td>LP6G</td>
<td>3A001.a.11.b</td>
<td>HMC1033LP6GE</td>
</tr>
<tr>
<td>2500</td>
<td>High Performance +3.3 V Clock Generator</td>
<td>97</td>
<td>-163</td>
<td>350</td>
<td>0.57</td>
<td>-226/-227</td>
<td>LP6G</td>
<td>3A001.a.11.b</td>
<td>HMC1035LP6GE</td>
</tr>
<tr>
<td>3000</td>
<td>Clock Generator with Fractional-N PLL+VCO</td>
<td>118 / 78</td>
<td>-165</td>
<td>350</td>
<td>0.86</td>
<td>-227/-230</td>
<td>LP6G</td>
<td>3A001.a.11.b</td>
<td>HMC1034LP6GE</td>
</tr>
</tbody>
</table>

Hittite Clock & Timing ICs

Hittite Clock & Timing ICs offer excellent Power Supply Rejection Ratios (PSRR) and spur reduction. For demanding applications where additional supply noise filtering and regulation is required, low noise linear voltage regulators from Hittite reduce system complexity and offer excellent power supply noise immunity. These industry leading regulators are assembled in space saving LP3 (3 mm x 3 mm) packages and offer noise spectral densities of <7 nV/sqrt (Hz) at 1 kHz offsets.

DC POWER CONDITIONING - Linear Voltage Regulators

<table>
<thead>
<tr>
<th>Input Voltage (V)</th>
<th>Function</th>
<th>Output Voltage (V)</th>
<th>Output Current (mA)</th>
<th>Power Supply Rejection Ratio (PSRR) (dB)</th>
<th>Output Noise Spectral Density (nV/√Hz)</th>
<th>Regulated Outputs</th>
<th>Package</th>
<th>ECCN Code</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.35 - 5.6</td>
<td>Quad High PSRR</td>
<td>2.5 - 5.2</td>
<td>15 - 100</td>
<td>80</td>
<td>60</td>
<td>7</td>
<td>3</td>
<td>4</td>
<td>LP3</td>
</tr>
<tr>
<td>3.35 - 5.6</td>
<td>Low Noise, High PSRR</td>
<td>1.8 - 5.2</td>
<td>500</td>
<td>80</td>
<td>60</td>
<td>7</td>
<td>3</td>
<td>4</td>
<td>LP3</td>
</tr>
<tr>
<td>4.8 to 5.6</td>
<td>Low Noise, High PSRR</td>
<td>1.8 to 5.1</td>
<td>400</td>
<td>60</td>
<td>60</td>
<td>6</td>
<td>3</td>
<td>4</td>
<td>LP3</td>
</tr>
</tbody>
</table>

Our Products are Available in SMT Package Format

Hittite’s website contains full datasheets, application notes, as well as ordering information for our complete product offering of over 1075 products across 36 product lines.
HMC1033LP6GE & HMC1035LP6GE

3.3V High Performance Programmable Clock Generator, 25 to 2500 MHz

- Integer & Fractional-N Mode Frequency Translation from 25 MHz to 2.5 GHz
- Configurable Outputs: LVDS-Compatible or LVPECL with 12 Settings to Adjust the Signal Amplitude
- “Phase Noise on Demand” feature to switch between “Power Priority” and “Performance Priority” Modes
- Adjustable PLL Loop Bandwidth via External Loop Filter to Control Setting Time & Noise Profile
- Output Disable/Mute Control
- Lock Detect Signal
- Exact Frequency Mode to Achieve Reference Frequency Tuning for DDS Replacement Applications

40-Lead, 6 x 6 mm SMT Package

New!

HMC1033LP6GE - Excellent Noise Floor
Improves Data Converter SNR

HMC1033LP6GE - Superior PN Performance
Improves PHY BER & Link Jitter

HMC1033LP6GE - Power Savings with Phase Noise on Demand Feature

---

Visit us: www.hittite.com  ContaCt us: timing@hittite.com
**HMC1032LP6GE & HMC1034LP6GE**

Clock Generator with Fractional-N PLL & Integrated VCO, 125 to 3000 MHz

- 125 MHz to 3000 MHz (HMC1034LP6GE)
- 125 MHz to 350 MHz (HMC1033LP6GE)
- <80 fs Phase Jitter @ 2 GHz (12k to 20 MHz Integration), -170 dBc/Hz Phase Noise Floor
- 24-Bit Delta-Sigma Fractional-N Synthesis achieves <3 Hz Typical Resolution
- Adjustable Drive Strength, CML True Differential Outputs
- Adjustable Loop Bandwidth via External Loop Filter (2nd Order R-C)

**Excellent Phase Noise Improves Data Converter SNR**

**Fractional-N Mode Integrated Jitter (1 kHz to 200 MHz)**

- 1000 10000 100000 1000000 10000000 100000000
- 10 MHz noisy input signal
- RMS integrated Jitter (12 kHz to 20 MHz) = 16 ps
- Free running 100 MHz VCXO
- RMS integrated Jitter (12 kHz to 20 MHz) = 58 fs
- 100 MHz HMC1031 Output
- RMS integrated Jitter (12 kHz to 20 MHz) = 58 fs

**HMC1031MS8E**

Clock Generator with Integer-N PLL, 0.1 to 500 MHz

- Integer-N PLL Clock Generator with External VCO/VCXO
- Ultra-Low Power Consumption: <2 mA Typical in Normal Operation
- Hardware Pin Programmable Reference Clock Multiplication Ratios of x1, x5, x10
- Phase Noise Floor (Figure of Merit): -208 dBc/Hz (Typical)

**Very Low Power Consumption**

**Typical Closed Loop Phase Noise, as Jitter Attenuator**

- 2.6 2.8 3 3.2 3.4 3.6
- 1 10 10
- 3 2.5 3 2.5
- 1.5 1.5 1.5
- 2.6 2.8 3 3.2 3.4 3.6
- 1.5 1.5 1.5
- DIV 1, REF/VCXO = 122.88MHz
- DIV 5, REF = 10 MHz, VCXO = 150 MHz
- DIV 10, REF = 10 MHz, VCXO = 100 MHz

VISIT US: www.hittite.com

CONTACT US: timing@hittite.com
HMC987LP5E
3.3V Low Noise, 1:9 Fanout Buffer, DC to 8 GHz

- 8 LVPECL Outputs (800 mVp-p into 50 Ohm Single-Ended Load)
- 1 Adjustable Power RF Output (-3 to 6 dBm)
- Flexible Input Buffer: LVPECL or AC-Coupled Input Compatible
- Serial or Parallel Control & Pin-Controlled Chip Enable
- Single-Ended or Differential-to-Differential Conversion
- Optimized for Very Low Output-to-Output Skew

HMC988LP3E
3.3V Programmable Digital Delay & Divider IC, DC to 4 GHz

- Single Channel Clock Divider & Delay Management IC
- Programmable Clock Divider by 1/2/4/8/16/32
- Delay Adjustment in 1/2 Clock Cycles or in 60 Steps of 20 ps
- -170 dBc/Hz Phase Noise Floor for Negligible Jitter Contribution
- 800 mVp-p LVPECL Output
- 3.3V Operation (or 5V with Optional On-Chip Regulator)
Data Converter Clocking with Hittite Clock Generators

Selecting the right components for clock generation and data conversion enables a designer to extract the best performance from a given architecture. Data converter dynamic range and linearity performance can be improved by careful consideration of clock generator characteristics.

Important criteria to consider when choosing a clock generator are phase jitter and phase noise floor, which impact the SNR of the data converter being clocked. As the graph below indicates, the low phase noise floor of the chosen clock generator as well as its low integrated phase jitter helps to minimize the SNR degradation at higher ADC/DAC frequencies in multi-acquisition applications. The HMC1034LP6GE with integer-mode configuration offers the lowest clock jitter and offers significant improvements over clock generators with higher jitter.

Hittite’s Clock & Timing ICs are designed with data converter applications in mind, and work well with Hittite’s high speed ADC devices. Our clock generators with industry’s best close-in and far-from-carrier phase noise are ideally suited to extract the best performance from data converters.
10G/40G/100G Networking & Storage Line Cards

Frequency Translation with HMC1031MS8E

Together with an external loop filter and a Voltage Controlled Crystal Oscillator (VCXO), the HMC1031MS8E forms a complete clock generator solution targeted at low frequency jitter-cleaner and reference clock generation applications. Quite often, the reference clock in a test & measurement or a communications system is a high accuracy Oven Controlled Crystal Oscillator (OCXO) with excellent long-term stability.

The HMC1031MS8E may find applications when the OCXO frequency needs to be multiplied up to a higher rate to drive the primary clock inputs in a system. The device offers a very low power, small package and high performance method to multiply its incoming frequency in x1, x5 and x10 rates. Such multiplication is needed because the higher reference clocks improve phase noise, ADC/DAC SNR, clock generator jitter and PHY BERs. In this scheme, the HMC1031MS8E may be connected to an external low cost VCXO (e.g. at 50 MHz or 100 MHz), and lock this external VCXO to the excellent long-term stability of the OCXO.
Clock Generation

Our Clock & Timing solutions are ideal for communications, control, sensing & entertainment electronic systems across all markets. Hittite Clock Generation ICs enable deterministic system design with low noise clock signals that have very low jitter and fast rise and fall times.

Clock Distribution

Hittite Clock Distribution ICs with the industry’s best phase noise floor performance are used to distribute Data Converter Sample Clocks with negligible additive jitter.

HMC1034LP6GE vs. Competitor

-150 dBc/Hz Phase Noise Floor
- 228 fs Jitter Generation, 12 k to 20 MHz
- 500 ps Rise and Fall Time

Hittite
- -166 dBc/Hz Phase Noise Floor
- 99 fs Jitter Generation, 12 k to 20 MHz
- 125 ps Rise and Fall Time

16 dB Lower Phase Noise Floor & Faster Rise and Fall Time = Better System Performance

HMC987LP5E vs. Competitor

-157 dBc/Hz Phase Noise Floor
- 102 fs Jitter Generation, 12 k to 20 MHz
- 130 ps Rise and Fall Time

Hittite
- -164 dBc/Hz Phase Noise Floor
- 59 fs Jitter Generation, 12 k to 20 MHz
- 65 ps Rise and Fall Time

7 dB Lower Phase Noise Floor & Faster Rise and Fall Time = Better System Performance
Hittite’s Clock & Timing Evaluation Software enables users to communicate with, and control, Hittite Clock & Timing ICs with their PCs via the provided USB connection board. The software features a simple GUI to set reference and output frequencies, program registers, and select operation modes.
**HITT-PLL: Hittite’s Clock Design & Analysis Tool**

- Accurately Simulate Your Design
- Easily Optimize Performance by Varying Loop Filter Components and Noise Profiles
- Reduce Design Time by Generating Phase Noise Plots and Jitter Measurements
- Model Transient Behavior to Estimate Loop Settling Times and Frequency Changes

---

**Select Optimum Loop Filter Components**

**PLL Design & Analysis Tool Version 1.04**

Programmed Noise Sources Can be Modified by Individual Sources