# Reconfigurable radio and recorder meets demands of diverse, evolving wireless standards; an advanced transceiver IC makes a compact, multichannel, wideband implementation possible

The astonishing, sometimes bewildering array of available wireless standards—with their different frequencies, bandwidths, protocols, and formats—has given users unprecedented connectivity and access. But it has also meant that engineers of wireless systems are faced with severe challenges when designing or investigating issues, performance, and options.

The solution seems obvious: minimize use of dedicated hardware, and instead rely on a software-defined radio (SDR) to implement and manage as much of the transmitting and receiving functionality as possible. Today's high performance, low power processors—including FPGAs—and their ability to execute complicated algorithms at high speed make such real-time implementation practical.



Figure 1. The Maveriq Multichannel Reconfigurable RF Transceiver from Epiq Solutions offers significant SDR capability in a small package and covers a tuning range from 100 MHz to 6 GHz.

But there's a real-world impediment to this solution: it is difficult to design wideband analog circuitry for the receiver and transmitter signal paths. As a result, most broadband SDRs use a set of overlapping, parallel analog channels, each optimized for a specific slice of the overall band, and with bandwidths matched to the signals of interest in each segment. While this approach is technically effective, it requires considerable hardware, PC board real estate, power, and of course, cost.

That's the dilemma that Epiq Solutions (Schaumburg, IL 60173, *www.epiqsolutions.com*), faced as they developed their latest SDR unit, the Maveriq™ Multichannel Reconfigurable RF Transceiver (Figure 1) an advanced platform combining multiple RF transceivers, internal solid state drive (SSD) for data recording, an on-board Intel x86 CPU running Linux, and a gigabit Ethernet interface for high speed data access. As designers and builders of state-of-the-art, reconfigurable radio systems for mission critical applications, their objective was to deliver a more powerful multichannel version of their existing Matchstiq™ SDR.

Despite its advanced features and capabilities, Maveriq is a portable, low power platform, while previous solutions required large and bulky hardware configurations. Combined with a library of ready-to-run specialty software applications, Maveriq can immediately be used to solve challenging signal processing requirements. These include scanning and decoding cellular radio signals from both base stations and mobile phones; recording wideband RF to its internal hard drive (SSD), as well as RF playback; and implementing $2 \times 2$ MIMO (multiple input, multiple output) waveforms.

> "The AD9361 provides the RF flexibility and integration needed to enable our next generation SDR platform."
> **John Orlando, Epiq's CEO and System Architect**

## An IC Enables a New Design Approach

The engineers at Epiq were able to pack this much performance into a small, low power unit because of a new IC, the AD9361 RF Agile Transceiver™ from Analog Devices, specifically tailored for SDR applications. According to John Orlando, Epiq's CEO and System Architect, "The AD9361 provides the RF flexibility and integration needed to enable our next generation SDR platform."

This 10 mm × 10 mm chip scale device with dual independent channels (Figure 2) has user tunable bandwidth from 200 kHz to 56 MHz and 12-bit analog-to-digital and digital-to-analog converters operating at up to 61.44 MSPS, along with other features and performance that are needed to build a signal chain spanning 70 MHz to 6 GHz. Critical operating parameters are user adjustable "on the fly" for optimum matching to the application requirements. Using this component reduces the overall footprint of the entire analog front end (AFE) while keeping power consumption for this portion of the design in the 1 W region—essential to stay within the product power budget.

The overall Maveriq unit (Figure 3) supports 2 × 2 MIMO or 4-channel receiver configurations via a pair of AD9361's, with an RF tuning range from 100 MHz to 6 GHz, 1 kHz step size, and 2 ms tuning time. It includes an integrated GPS receiver with 1 PPS performance, up to a 1 TB internal solid state hard drive (SSD) supporting data recording 100+ MBPS (sustained), and Gigabit Ethernet for interfacing to external systems.

The processing function is centered on a dual-core Intel x86 CPU running Linux plus an FPGA for signal processing tasks, along with run-time loadable/ executable software applications, all supported by an available software development kit (SDK) for custom applications. The entire unit is just 9.1" × 6.6" × 1.7" (23 cm × 16.7 cm × 4.3 cm), weighs 1.9 lbs (0.9 kg), and dissipates 15 W (depending on FPGA and I/O usage).

Of course, processing power is inadequate without suitable RF performance. The receiver has a typical noise figure of less than 8 dB and typical IIP3 of −10 dBm. Transmit side performance parameters such as bandwidth, tuning, and speed complement the receive side numbers, along with output power of +5 dBm.

Although the AD9361 IC was a key enabler for this design, additional improvements are always on the horizon. Certain applications require stretching the RF performance down to the 20 MHz range and below, which is beyond the reach of the AD9361. Further, selection of RF components such as low noise amplifiers (LNAs) capable of operating down to 20 MHz can also be a challenge, especially for size and power constrained designs. It's simplistic to think that advances in low power processing coupled with availability of large amounts of memory plus high speed digital I/O and connectivity—all driven by Moore's law—are sufficient for a viable small, high performance SDR. The reality is that the front-end channel for both receive and transmit paths is just as important, and developments in RF ICs that combine analog processing, filtering, and conversion not only minimize the algorithm burden, but make much of the actual SDR performance possible.
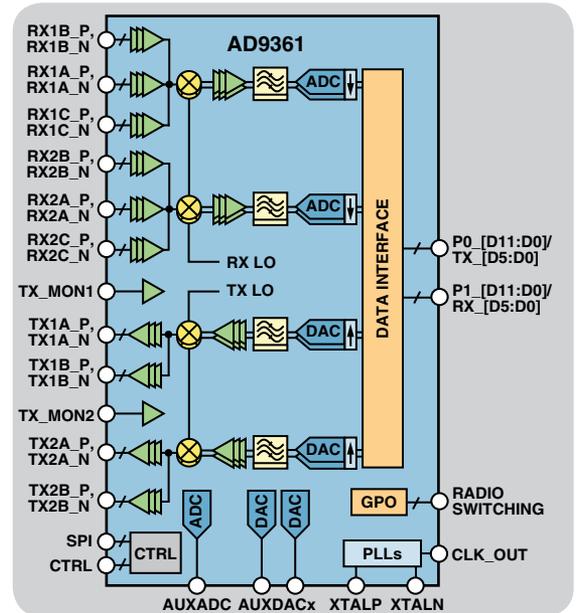


Figure 2. Analog Devices' AD9361 RF Agile Transceiver IC integrates the many RF functions needed for a 2 × 2 analog signal chain while allowing user programmability, thus greatly minimizing board space, power consumption, and cost.
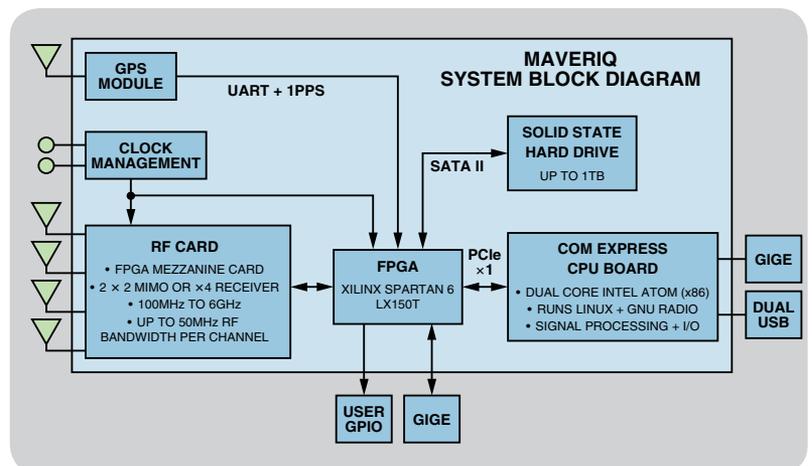


Figure 3. The Maveriq unit comprises RF, baseband, processing, storage, and connectivity functions with much more detail and sophistication than this basic block diagram can reveal.

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