

Zero-Drift Amplifiers: Now Easy to Use in High Precision Circuits

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A zero-drift amplifier, as the name suggests, is an amplifier with offset voltage drift very close to zero. It uses auto-zero or chopping technology, or a combination of both, to continuously self-correct for dc errors over time and temperature. This enables the amplifier to achieve microvolt-level offsets and extremely low offset drifts. Therefore, it is uniquely suited to be used in signal conditioning circuits with high gain and precision performance. For example, a sensor (such as a temperature, pressure, or load cell sensor) typically produces a low level output voltage and hence requires an amplifier to amplify its output without introducing additional errors. Zero-drift amplifiers, designed for ultralow offset voltage and drift, high common-mode rejection, high power supply rejection, and reduced $1/f$ noise, are an ideal choice to achieve a high level of resolution in a demanding system application, such as sensing, with a long product life cycle.

Basic Architecture of a Zero-Drift Amplifier

Figure 1 shows the circuit diagram of a basic chopper amplifier in unity gain configuration. The dc gain path consists of an input chopping switch network ($CHOP_{IN}$), a first transconductance amplifier (G_{m1}), an output chopping switch network ($CHOP_{OUT}$), a second transconductance amplifier (G_{m2}) and frequency compensation capacitors ($C1$ and $C2$). $CHOP$ and $CHOP'$ are controlled by a clock generator and function to correct unwanted amplifier dc offset voltage (V_{OS}).

Figure 2 shows the associated timing diagram and expected output voltage (V_{OUT}). When the $CHOP$ clock signal is high (A phase), amplifier G_{m1} 's differential input and output are connected to the signal path with no inversion. This results in a positive output voltage, V_{OUT} , due to the presence of V_{OS} . When the $CHOP'$ clock signal is high (B phase), G_{m1} 's input and output are connected to the signal path with inversion, resulting in a negative output voltage due to V_{OS} . The positive and negative output voltages from G_{m1} result in an output voltage equal to $\pm V_{OS}$. This chopping concept in the time domain is similar to modulation in the frequency domain. In other words, the offset voltage of G_{m1} is up-modulated by $CHOP_{OUT}$ to the chopping frequency. On the other hand, the input signal is chopped twice by $CHOP_{IN}$ and $CHOP_{OUT}$. This is equivalent to the input signal being up-modulated and then down-modulated to its original frequency. Hence, the input signal gets through to the output with no inversion.

The positive and negative output voltages ($\pm V_{OS}$) from G_{m1} appear as voltage ripples at V_{OUT} (Figure 2). In addition, the $CHOP$ and $CHOP'$ clocks are coupled to the differential input pins through parasitic capacitances associated with the switches. When the clocks change state, charges are injected into the differential input pins. These charge injections are translated into output voltage glitches via the finite input source impedances. The magnitude and shape of the glitches

depend on the amount and matching of the input source impedances and the charge injections at the differential input pins. These output ripples and glitches introduce switching artifacts that appear as increases in noise spectrum at the chopping frequency and its multiple integer frequencies. Also, the magnitude and frequencies of the switching artifacts differ for each zero-drift amplifier and from unit to unit. In this article, the term chopping and switching frequency are used interchangeably.

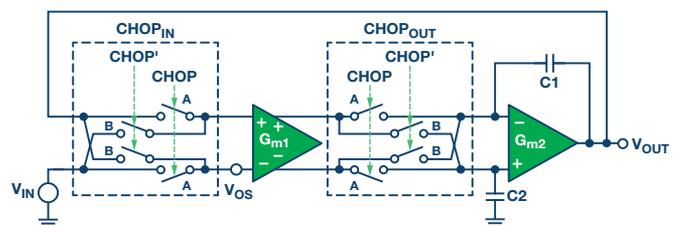


Figure 1. Chopping architecture.

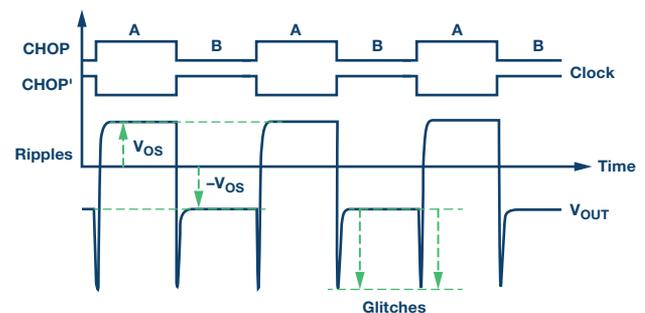


Figure 2. Chopping timing diagram.

Switching Artifacts as Shown on a Data Sheet

Traditionally, zero-drift amplifiers have fairly large broadband noise and low switching frequencies, ranging from a few kilohertz to a few tens of kilohertz. This limits their usage to dc and sub-100 Hz applications so that the switching frequency remains out of the signal bandwidth of interest. For applications requiring high precision and low drift at a higher bandwidth, it is important to use a zero-drift amplifier with higher switching frequency. As a matter of fact, the switching frequency is sometimes viewed as the figure of merit for zero-drift amplifiers. With advanced design architectures, newer zero-drift amplifiers are designed to have smaller switching artifacts at much higher frequencies. For example, in addition to chopping the offset voltage at 4.8 MHz, the [ADA4522-2](#), a high voltage, dual, zero-drift amplifier, uses a patented offset and ripple correction loop circuitry to minimize switching artifacts. The correction loop operates at 800 kHz and functions to null out the offset voltage, $\pm V_{OS}$ (as shown in Figure 2). Reducing $\pm V_{OS}$ to 1% of its original value provides a 40 dB improvement in the switching artifact. This reduces the system designer's effort to achieve targeted system level precision.

The easiest way to detect the switching artifact is by observing the amplifier's voltage noise density spectrum. Figure 3 shows the input referred voltage noise density graph of the ADA4522-2. Note that Channel B exhibits an increase in noise spectrum at its switching frequency of 800 kHz. This increase in noise spectrum, as described in the earlier part of this article, is the byproduct of the charge injection mismatch. Since the mismatch is part-to-part and channel-to-channel dependent, the magnitude of noise spikes are different and not all units exhibit the noise spike. As an example, Channel A of the same unit does not exhibit any noise spikes at the switching frequency of 800 kHz. The switching frequencies could also differ up to a factor of 10% to 20% from unit to unit due to the on-chip clock oscillator frequency variation.

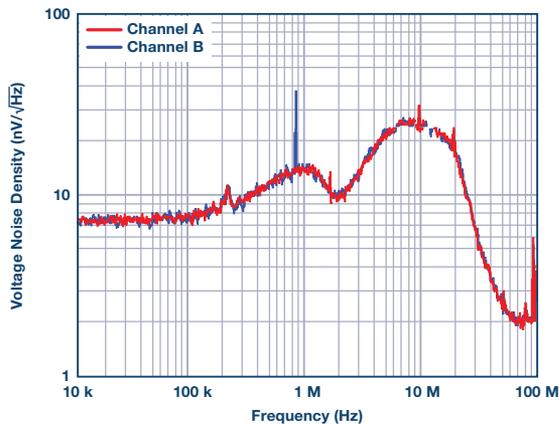


Figure 3. ADA4522-2 voltage noise density.

Noise Comparison Between Different Zero-Drift Amplifiers

Figure 4 shows the input referred voltage noise density of three different leading edge high voltage zero-drift amplifiers. Note that all three zero-drift amplifiers tested exhibit some sort of switching artifacts. Some of the switching artifacts also repeat at its multiple integer frequencies. These switching artifacts could be significant and could introduce errors in a circuit design. Hence, it is important to understand their impact on a circuit and find ways to mitigate the effect. If the amplifier has a closed-loop frequency that is higher than the switching frequency, this increase in noise spectrum will be integrated across the entire bandwidth and be reflected at the output. Not only that, this input-referred voltage noise will be gained up by the amplifier noise gain. For instance, assume that the amplifier is configured in a gain of 100, the effective output referred voltage noise density would also increase by a factor of 100.

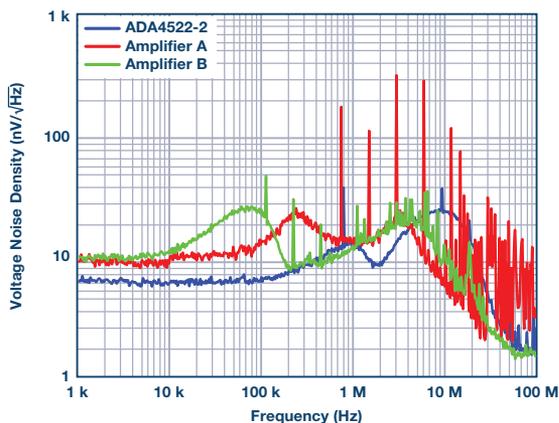


Figure 4. Voltage noise density of different zero-drift amplifiers.

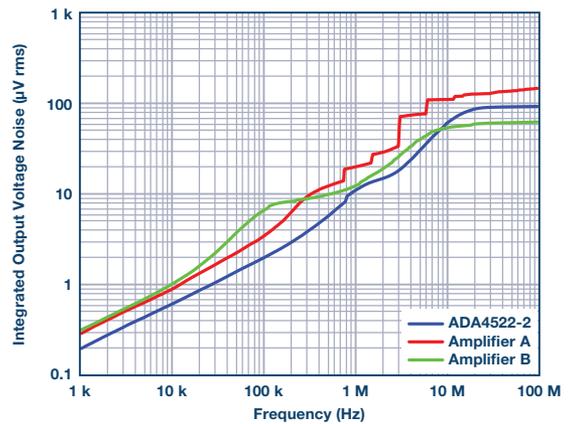


Figure 5. Integrated output voltage noise.

Total rms noise that is integrated at the output of an amplifier depends on the amplifier's bandwidth. Output voltage noise rolls off with the available bandwidth; therefore, the higher the gain or the higher the bandwidth, the higher the amplitude of the output amplifier noise. Figure 5 shows a graph of integrated output voltage noise vs. frequency. This is a helpful graph for understanding the total integrated noise with respect to a frequency. As an example, if the amplifier's bandwidth is limited to 100 kHz by means of filtering, the total output noise due to the inherent amplifier voltage noise can be read off the graph and will be as follows:

Table 1. Output Integrated Noise

Amplifier	Output Noise (μV rms)	Peak-to-Peak Output Noise (μV p-p)
ADA4522-2	1.91	12.61
Amplifier A	3.33	21.98
Amplifier B	6.40	42.24

Using a common multiplier (called crest factor) to convert rms voltage to peak-to-peak voltage, a peak-to-peak noise estimation is shown in the third column of Table 1. In a 5 V system, the ADA4522-2 would provide 18.6 bits of peak-to-peak resolution, whereas Amplifier B provides 16.8 bits of peak-to-peak resolution. Having a lower total integrated output noise is always desirable as it increases the signal-to-noise ratio and enables a higher resolution to the entire system.

Another interesting thing to note about Figure 5 is that the integrated noise increases with a step-like function at the noise spike frequencies. The noise spikes (with increased noise energies), albeit narrow, add significantly to the total output integrated noise.

Switching Artifacts in the Time Domain

Often times, the switching artifacts can be clearly seen in the voltage noise density spectrum in the frequency domain. To understand the time-based behavior of the switching artifact, one can configure the amplifier in a buffer configuration with the noninverting pin grounded and directly monitor

the output with an oscilloscope. Figure 6 shows the typical output of two zero-drift amplifiers. Note that Amplifier A exhibits output voltage spikes in various amplitudes. The spikes repeat themselves every $0.66 \mu\text{s}$. This matches the noise spikes that are seen at 1.51 MHz in Figure 4. On the other hand, the ADA4522-2 does not exhibit any switching artifact in the time domain (blue graph). In other words, the noise spikes that exist are below the noise floor of the measurement system and cannot be detected. This allows designers to use the ADA4522-2 in applications such as driving an ADC with confidence that noise spikes will not be an issue.

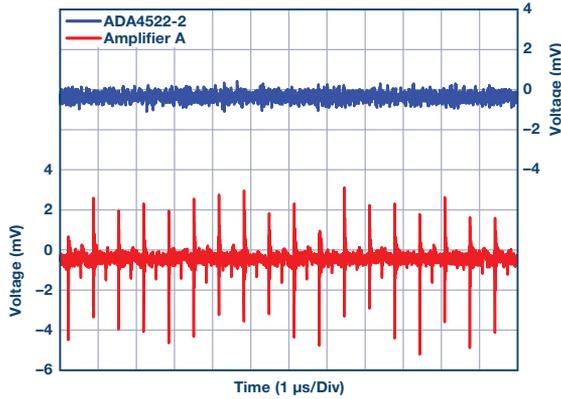


Figure 6. Output voltage noise in the time domain.

Filters to Mitigate Switching Artifact

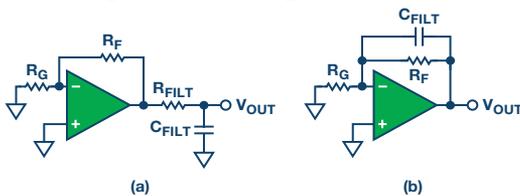


Figure 7. Zero-drift amplifier with filter setup.

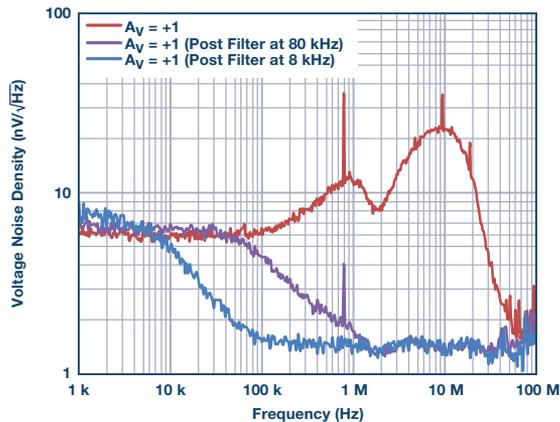


Figure 8. Voltage noise density of a unity-gain zero-drift amplifier with post filter.

To reduce the impact of the switching artifacts, there are a couple of methods that can be implemented. These methods ultimately lead to limiting the amplifier bandwidth such that it is less than the switching frequency. Using a filter is an effective way to suppress the noise spikes. The easiest design is to place a resistor-capacitor network at the amplifier output to create a low pass filter (Figure 7A). Figure 8 shows the voltage noise density of a zero-drift amplifier with a post filter designed at one or two decades below the switching frequency. The noise spike at 800 kHz reduces from $36 \text{ nV}/\sqrt{\text{Hz}}$ (no post filter) to $4.1 \text{ nV}/\sqrt{\text{Hz}}$ (post filter at 80 kHz),

which is below the amplifier's low frequency broadband noise level. With a post filter positioned two decades below the switching frequency (post filter at 8 kHz), the noise spike is no longer visible and the ADA4522-2 looks like any other traditional amplifier.

Some applications might not tolerate having an RC network at the output of the amplifier. Amplifier output current flowing through the filter resistor creates a voltage offset that introduces output error. In this case, one can opt to filter the noise spikes by placing a feedback capacitor across the feedback loop (Figure 7(b)). Figure 9 shows the output voltage noise density of an amplifier configured in gain of 10 with no filtering vs. having a post filter or a feedback filter positioned a decade below the switching frequency. The post filter configuration is more effective as a low-pass filter than the feedback capacitor.

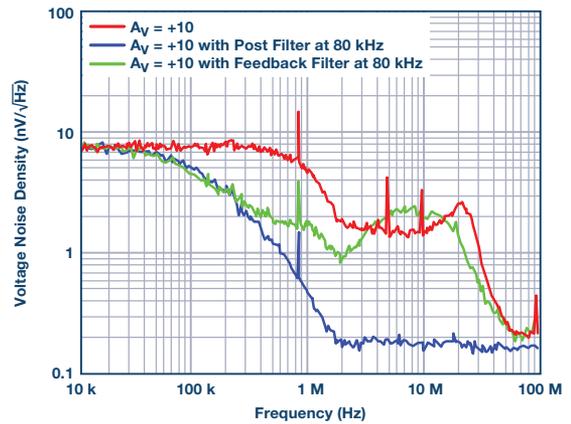


Figure 9. Switching artifact reduces with filters.

Using Zero-Drift Amplifiers in High Gain Configuration Helps

A lot of designers have used zero-drift amplifiers, but have not observed any switching artifacts in their system. One reason could be due to the configuration of the amplifier. Zero-drift amplifiers have low drift and offset, and are most often used to signal condition a low level amplitude sensor signal in a high gain configuration of, for example, a gain of 100 to 1000. Using the amplifier in a high gain configuration has the same effect as placing a low-pass filter on the amplifier. As gain increases, bandwidth decreases. Figure 10 illustrates how having a high gain configuration mitigates the switching effect. With a closed-loop gain of 100, the switching artifact can hardly be seen on the noise plots.

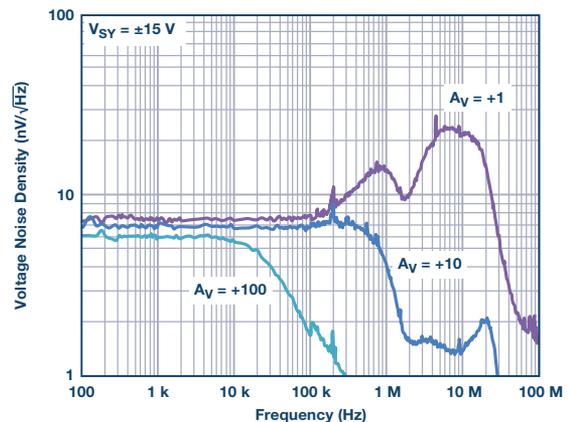


Figure 10. Amplifier bandwidth roll-off with gain.

The Benefits of ADA4522-2 as a Zero-Drift Amplifier

Analog Devices' newest zero-drift operational amplifier, the ADA4522-2, employs a patented and innovative circuit topology to achieve a high switching frequency and to minimize the switching artifacts in comparison to its predecessors. With a unity-gain bandwidth at 3 MHz and a switching frequency at 800 kHz and 4.8 MHz, a gain configuration of 40 is sufficient to filter the switching artifacts, and eliminates the need for external low-pass filtering. Its low offset voltage drift of 22 nV/°C maximum, low noise at 5.8 nV/√Hz (gain of 100 configuration), low input bias current at 150 pA maximum, high common-mode rejection, and power supply rejection make it an ideal choice for precision applications such as weigh scale, current sensing, temperature sensor front ends, load cell and bridge transducers, and many more drift-critical applications.

Conclusions

Zero-drift amplifiers feature very low offset voltage and drift and are an ideal choice for applications requiring precision amplification of low-level signals. Here are a couple of insights when using one.

All zero-drift amplifiers exhibit some sort of switching artifacts and this can most commonly be detected in the voltage noise density plots.

The magnitude of the switching artifact differs from unit to unit.

The switching frequency could differ from unit to unit up to a factor of 20%.

Switching artifacts can be detected in the frequency and the time domain. Depending on the application, they could present errors.

Zero-drift amplifiers are often used in a high gain configuration, where bandwidth is reduced and thus many times, switching artifacts do not pose an issue.

It is important to mitigate the switching artifacts to reduce the amount of output error. Apply a low-pass filter (RC post filter or feedback capacitor) to roll off the amplifier's bandwidth before the switching frequency to suppress the artifacts.

A high switching frequency simplifies filter requirements for a wide, useful, and artifact-free bandwidth.

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