

Next Generation SAR ADC Simplifies Precision Measurement

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Agenda

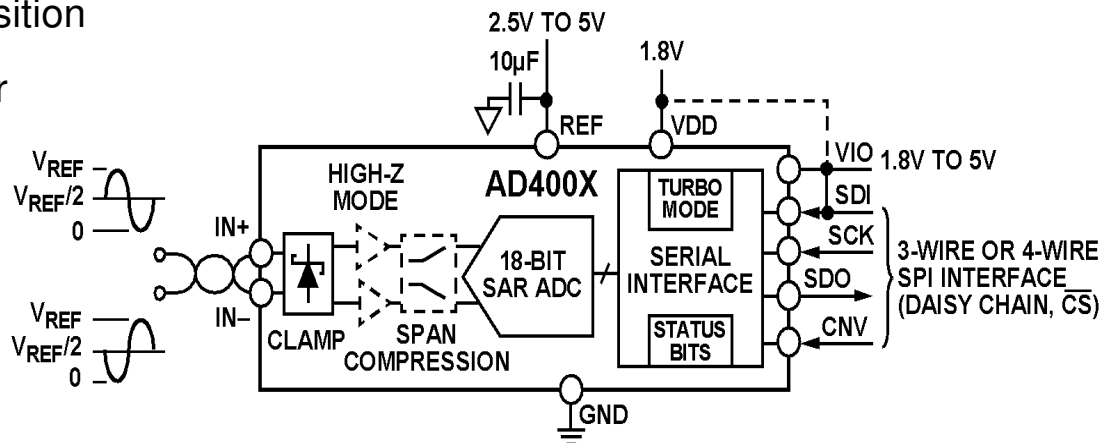
- ▶ **Introduction**
- ▶ **AD400X Ease of Use System-Level Benefits**
 - **Ease of Drive**
 - **Internal Overvoltage Clamp**
 - **Span Compression**
 - **Efficient Digital interface**
- ▶ **Performance Benefits**
- ▶ **Key Attributes and End Applications**
- ▶ **Design Resources**
- ▶ **ADI's First 20-bit Precision SAR ADC**
- ▶ **Conclusion**

AD400X: Next Generation of Industry Leading 16/18/20-Bit Precision SAR ADC Family

- ▶ Enables low power precision data acquisition
- ▶ Signal conditioning can be optimized for frequency bandwidth of interest
- ▶ Easy to achieve datasheet performance
 - Reduces design time, debug, risk

Key Benefits

- ▶ **Ease of Drive**
 - High-Z mode plus long acquisition phase enables the use of low power precision ADC drive amplifier when the bandwidth of interest is low
 - Reduces signal chain power consumption
- ▶ **Ease-of-Digital interface**
 - Low SPI clock rate requirements reduce IO power consumption and simplifies the requirements on digital Isolation
- ▶ **Reduced sensitivity to external circuitry**
 - Reduced performance sensitivity to resistor values in RC filter



AD4003: 18-Bit, 2MSPS Precision SAR ADC

Benefits and Features

► Ease of Use

► High Performance

- Throughput: 2 MSPS
- DNL: 18-bit No Missing Codes
- INL: $\pm 1.0\text{LSB}$ ($\pm 3.8\text{ppm}$) Max
- SNR: 100.5dB typ @ 1Khz
- THD: -123dB typ @ 1Khz

► True differential analog input range: $\pm V_{\text{REF}}$

- 0 V to V_{REF} with V_{REF} between 2.4 V to 5.1 V

► Low Power: Scales linearly with throughput

- 80 μW typ @ 10kSPS
- 16 mW typ @ 2MSPS (Total)

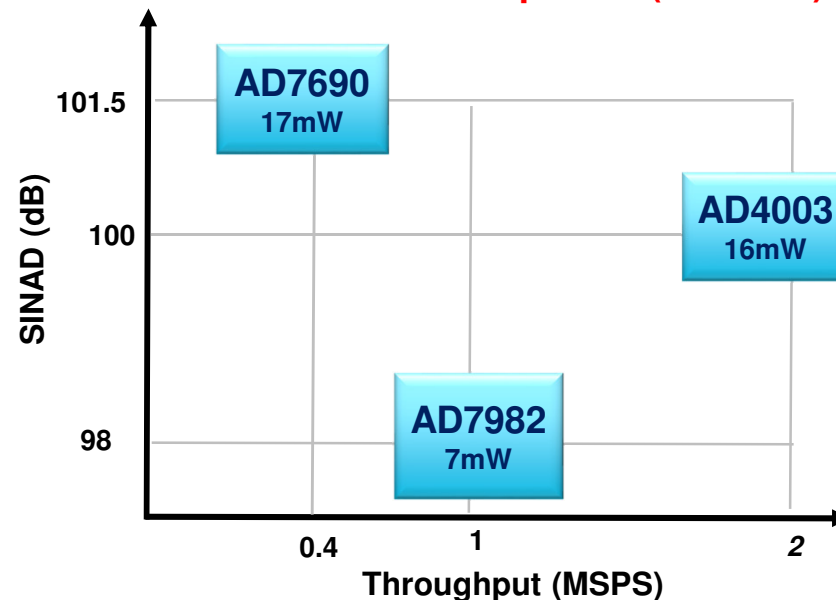
► Small Form Factor

► Guaranteed Operation: - 40°C to +125°C

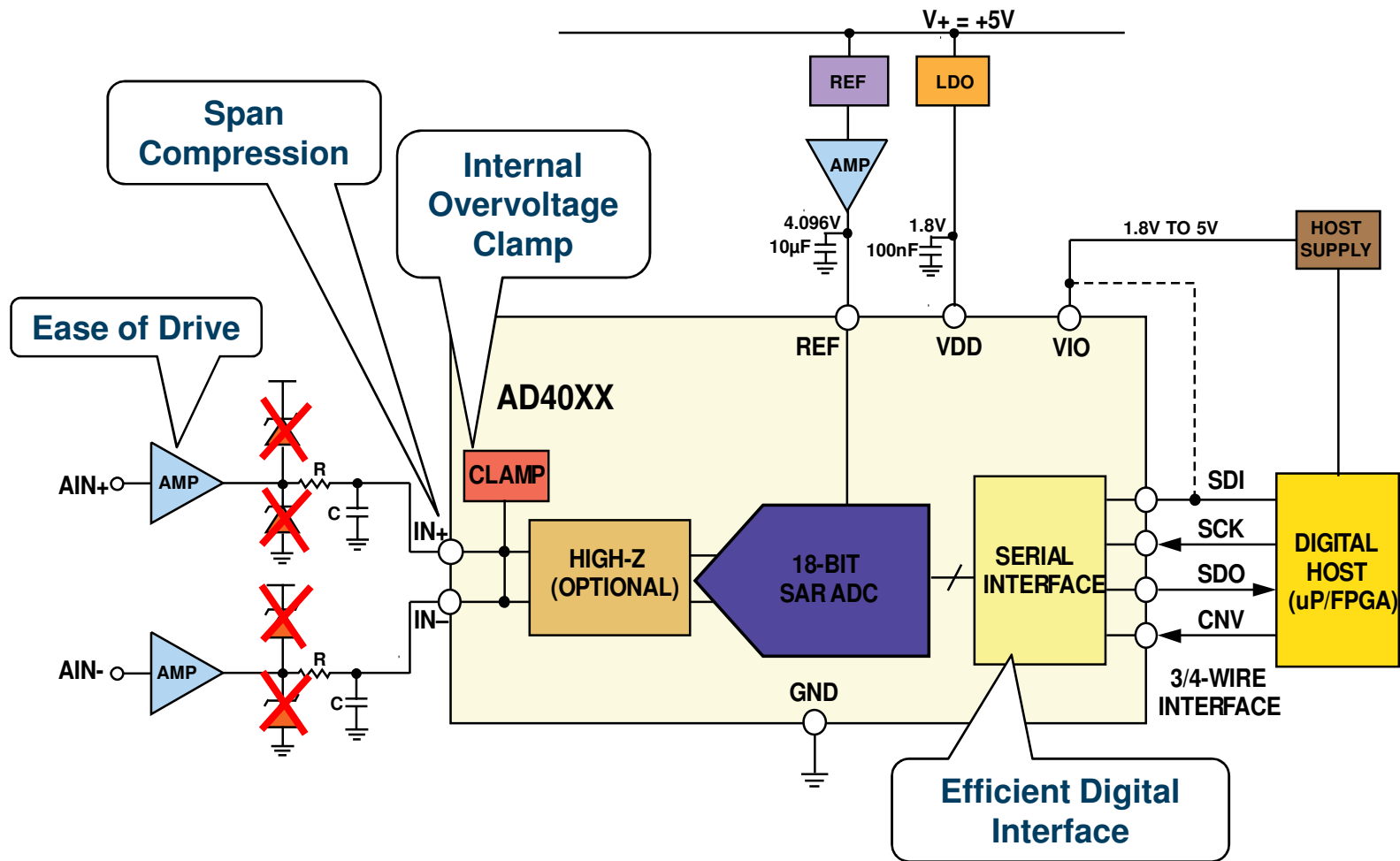
Resolution	VREF	VDD	Interface	Input	Package
18 Bits	2.4V to 5.1V	1.8V	SPI 1.8V/2.5V/3V/5V	Differential $\pm V_{\text{REF}}$	10-Icd MSOP 3x4.9mm 10-Icd LFCSP 3x3mm

Portfolio Positioning

► Pin-For-Pin Compatible (10- Lead)

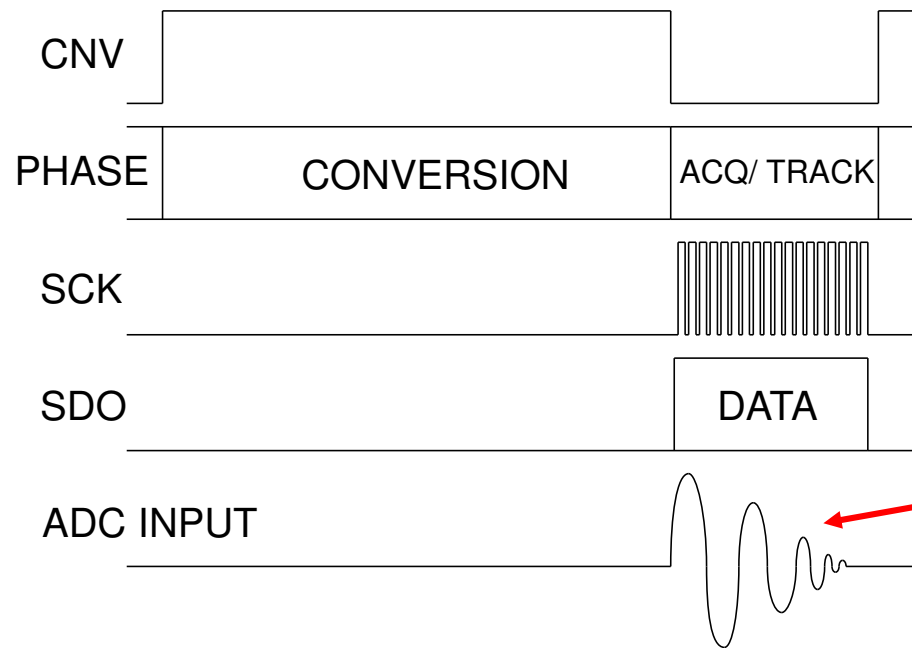


AD400X: Ease of Use Features



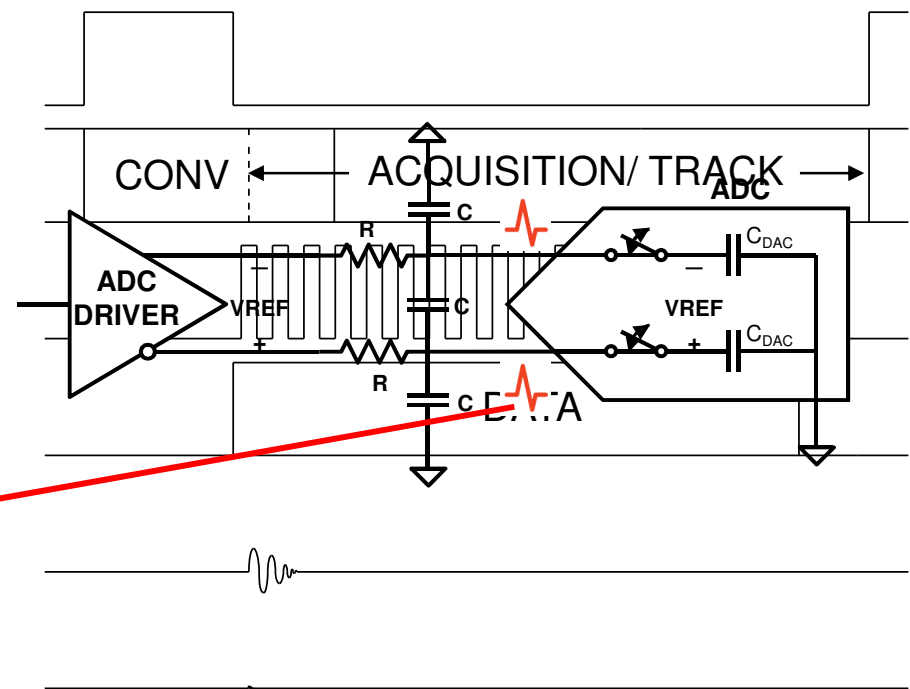
Ease of Drive

Traditional SAR

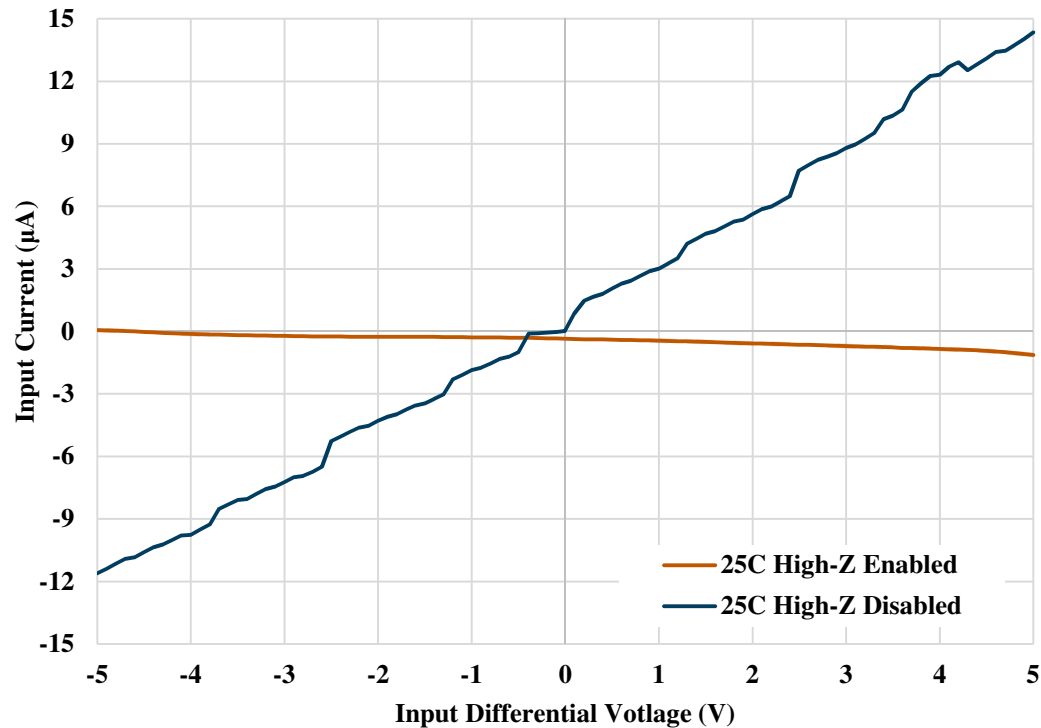


ADC INPUT HIGH-Z ENABLED

AD4003



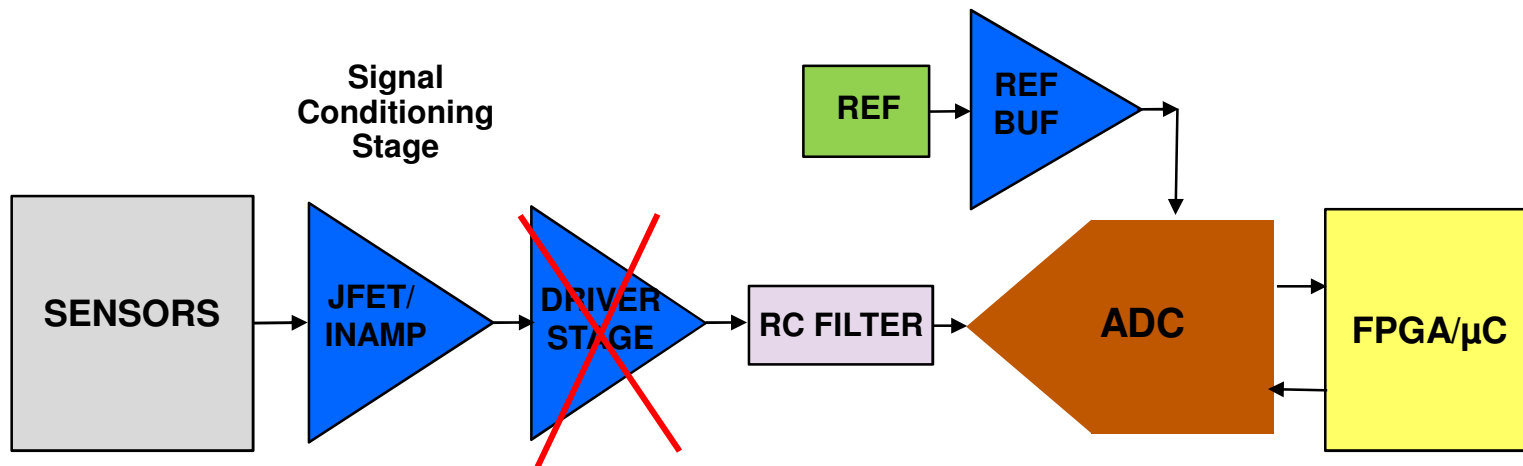
Ease of Drive: High-Z Mode



- ▶ Reducing the input current change versus input voltage change to $\pm 1.5\mu\text{A}$, which is 40x smaller versus previous SAR ADC products (AD7982 and AD7960 $\pm 30\mu\text{A/MSPS}$)
 - Reduces the nonlinearity error source from the external RC filter
 - Improves the signal chain INL and THD performance
- ▶ When high-Z mode is enabled, the ADC consumes $\sim 2\text{ mW/MSPS}$ extra power

Ease of Drive: High-Z Mode Benefits

- ▶ Enables low input current and improved THD with low power/BW amplifiers.
- ▶ ADC can be driven directly with precision amplifiers or signal conditioning stage.
- ▶ Eliminates the need of using dedicated high speed ADC driver when the input frequency of interest is low ($<10\text{kHz}$).

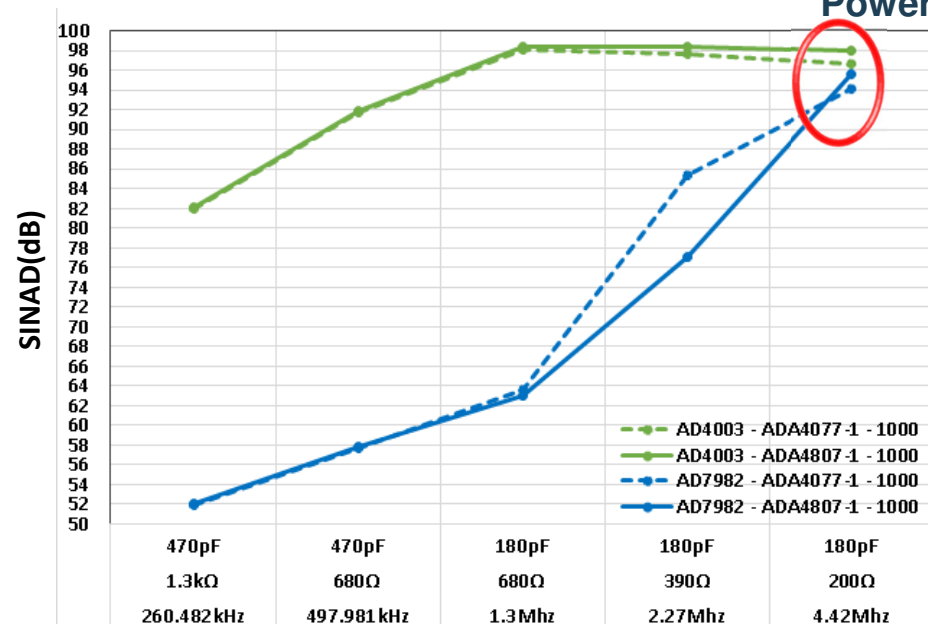


Typical Customer's Signal Chain

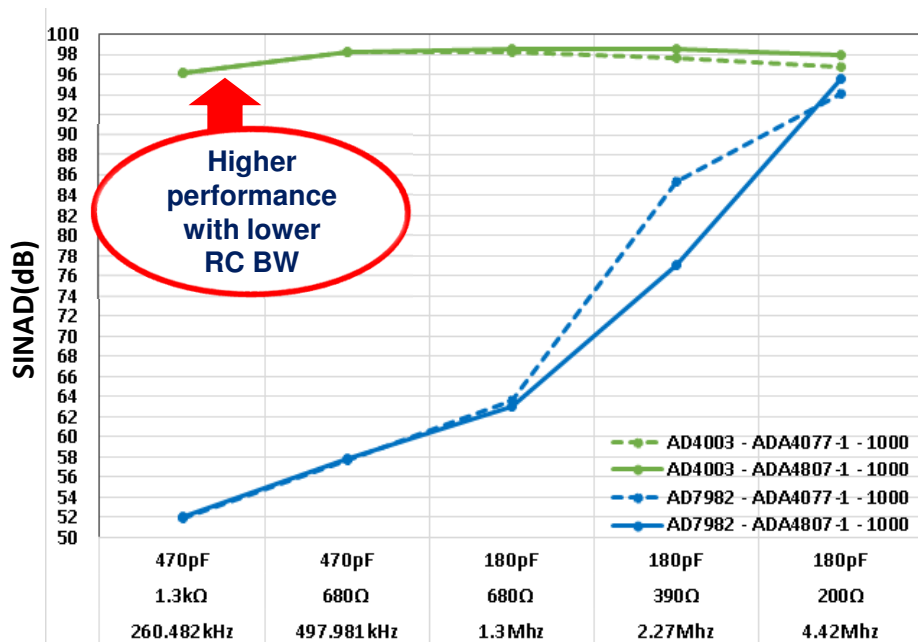
Ease of Drive: AD4003 vs AD7982 Driver Comparison

High-Z Mode Disabled

2.5x Lower
Power



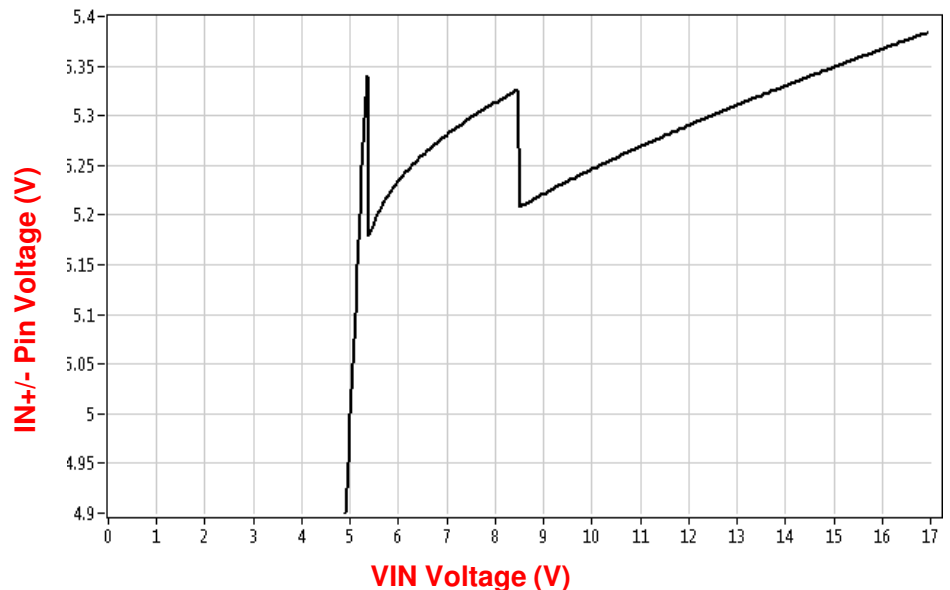
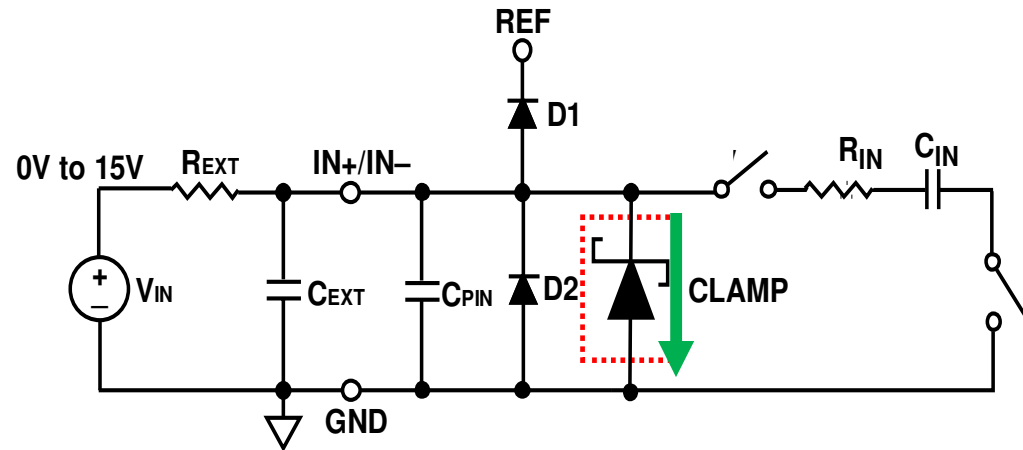
High-Z Mode Enabled



(Fs = 1MSPS, fin = 1kHz)

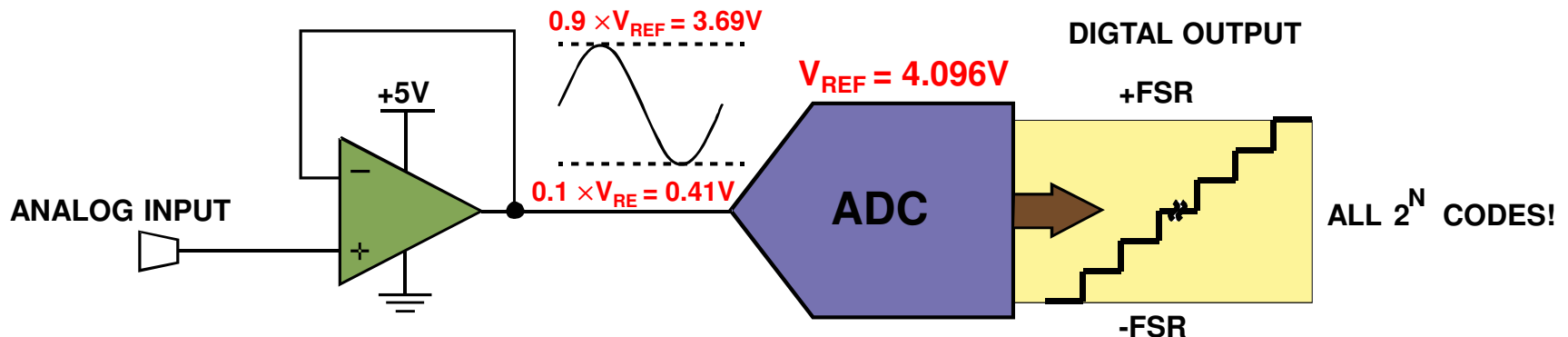
Internal Overvoltage Clamp

- ▶ Eliminates the need for external protection diodes and protects the ADC inputs against DC over voltage.
- ▶ When the clamp turns on, it can sink up to 50mA of current and current will flow through clamp into ground.
- ▶ NO current is pushed into the REF pin causing a disturbance on the reference. This is important if the reference is shared among multiple ADCs.



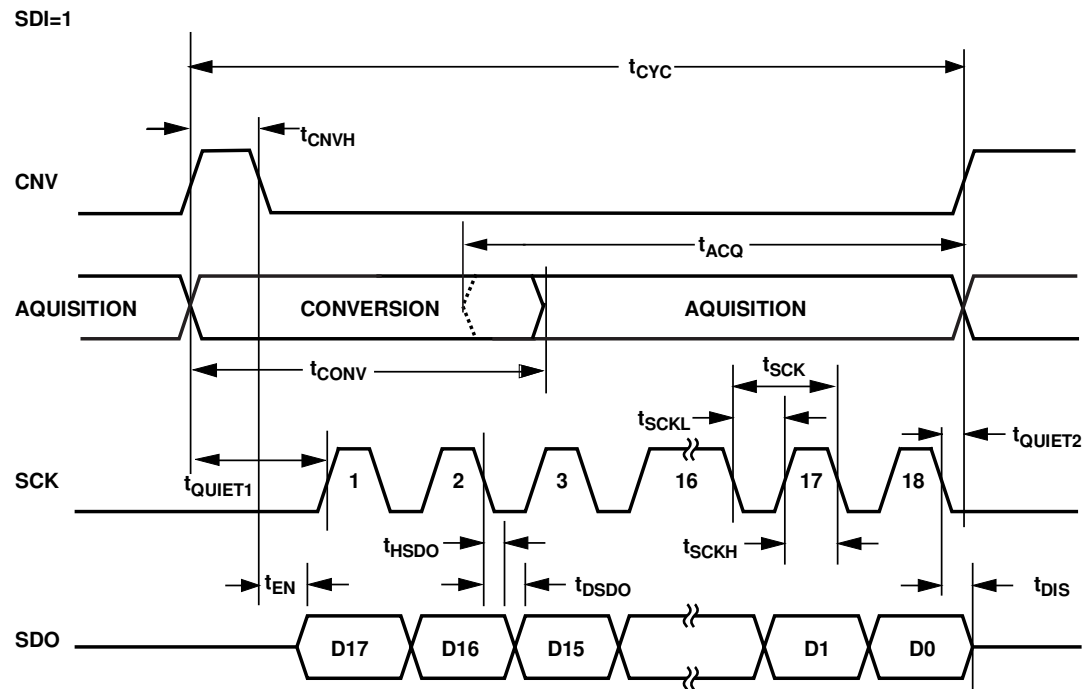
Span Compression

- ▶ Enables single positive supply rail to power the driver amplifier
 - Simplifies the power supply design. Lowers power consumption
- ▶ ADC performs a digital scaling function that maps zero-scale code from 0V to $0.1 \cdot V_{REF}$ and full-scale code from V_{REF} to $0.9 \cdot V_{REF}$.
- ▶ SNR takes about $\sim 1.9\text{dB}$ hit for the reduced input range $\rightarrow 20 \cdot \log(8/10)$



Efficient Digital Interface

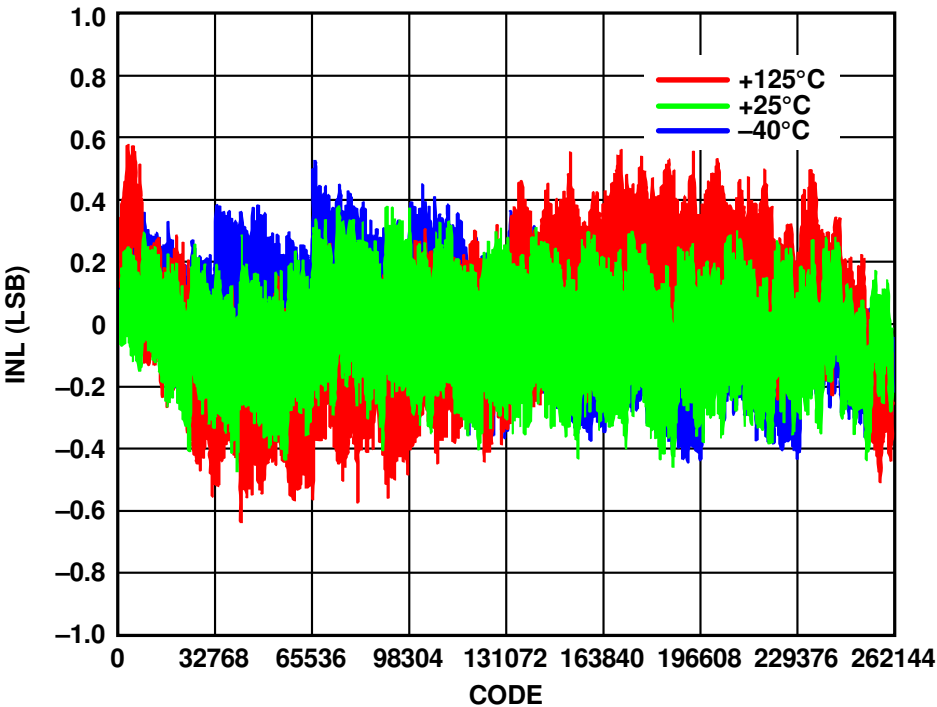
Features	System Benefit
Turbo mode Lower interface clock rates Register programmability and Status bits Option	Broadens selection of processors including lower end processors. Allows 2.5x slower SPI clock rate than AD798x when running at 1MSPS. Simplify isolation solution. Higher throughput with existing components. Error/status checking for functional safety.



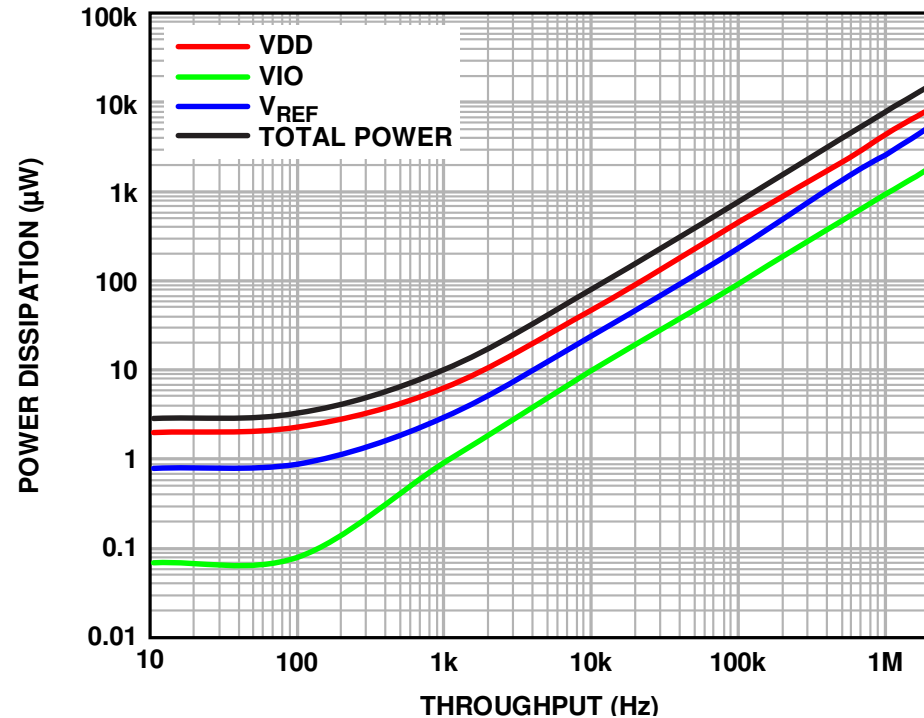
Turbo Mode

Performance Benefits

INL: ± 1.0 LSB (± 3.8 ppm) Max Guaranteed

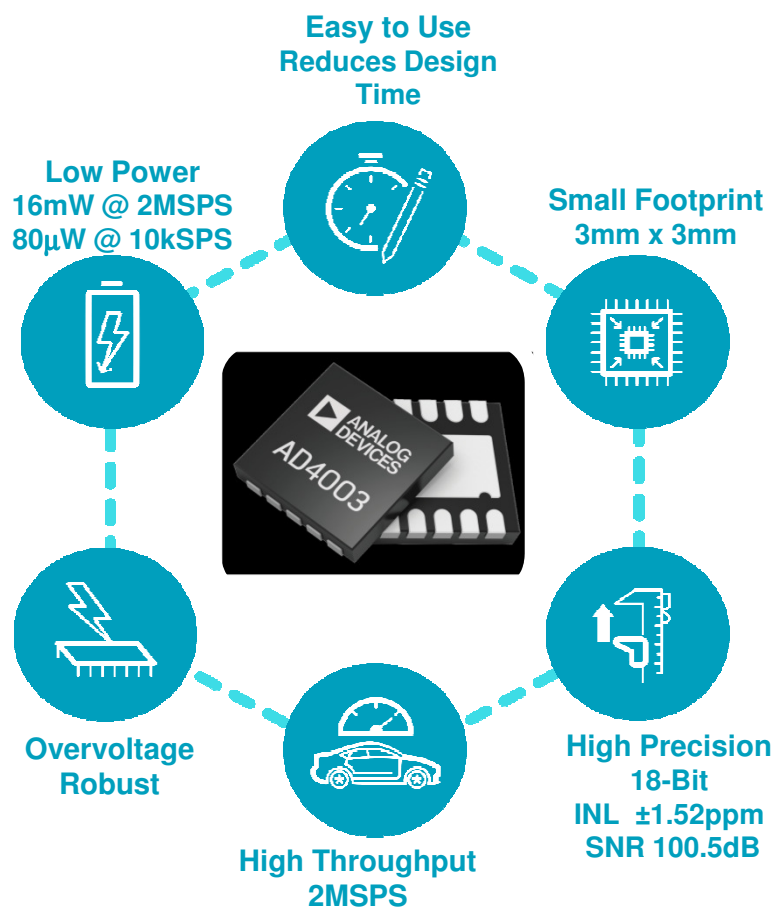


Power: 80 μ W @10kSPS; 8mW @ 1MSPS

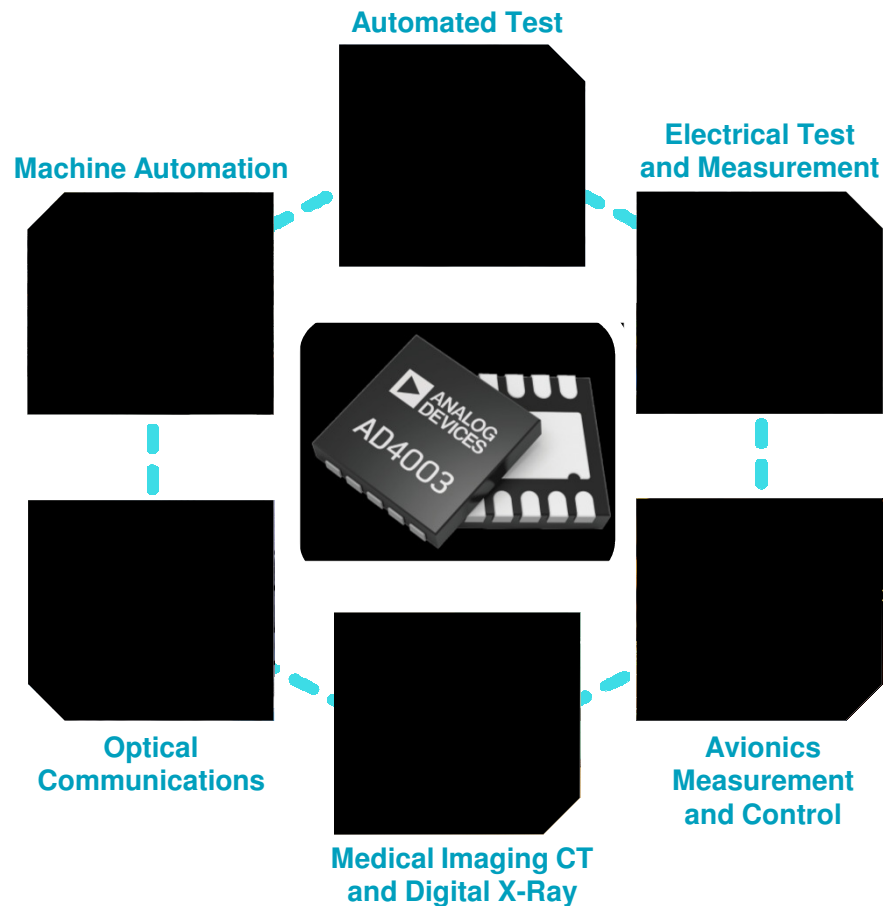


Key Attributes and End Applications

AD4000/3 Key Attributes

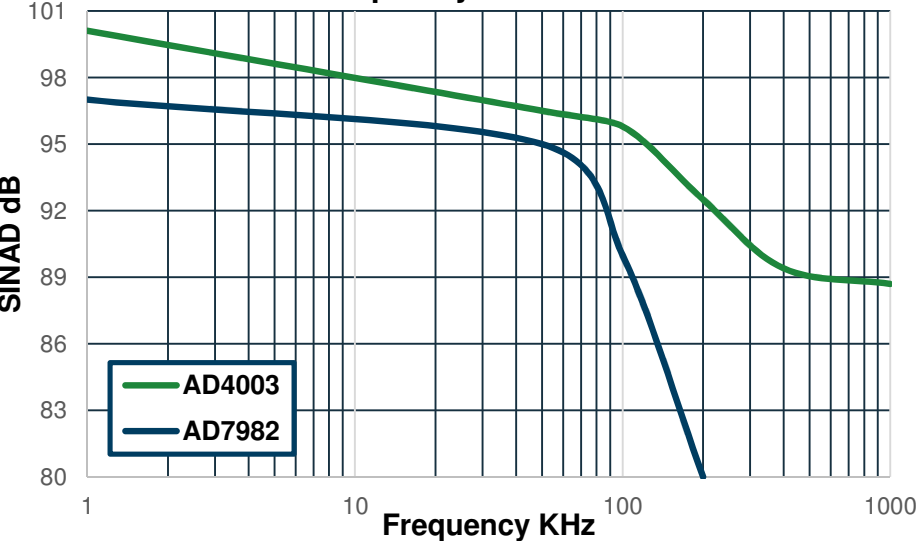


High Precision Data Acquisition Applications



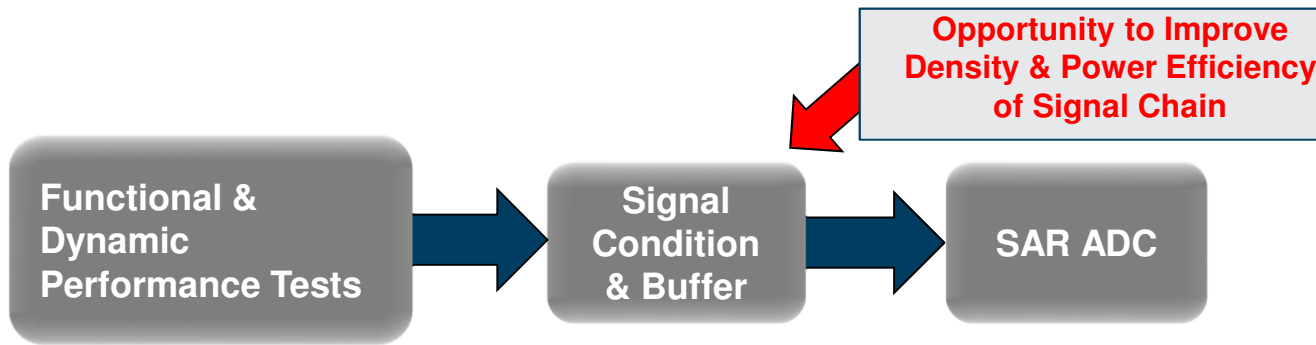
Instrumentation Applications

SINAD vs Frequency for AD4003 and AD7982



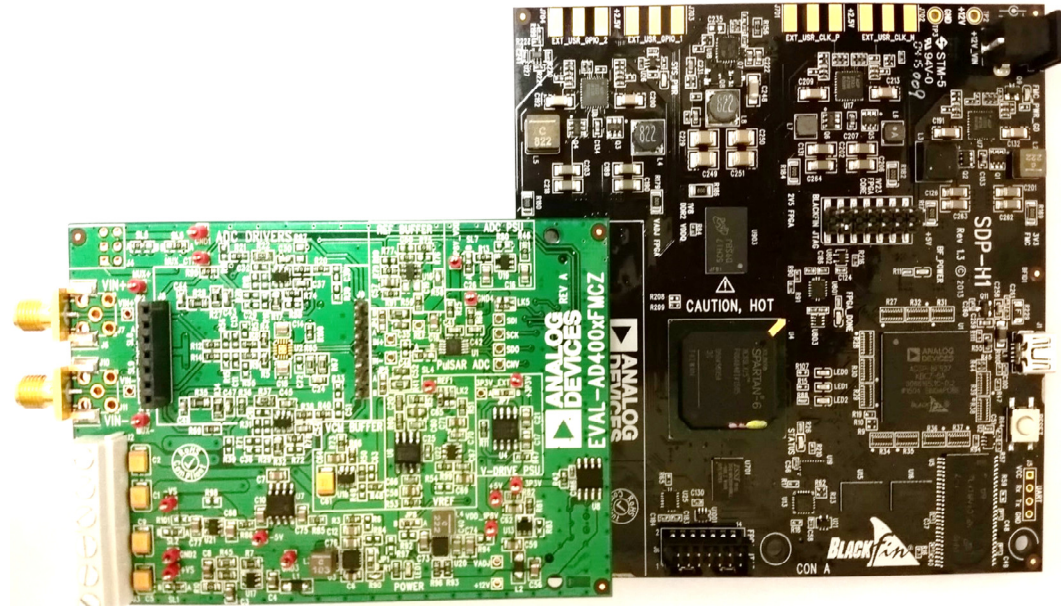
Improvements Realized with the AD400x Family

- ▶ Enables wider bandwidth high precision instrumentation equipment
- ▶ Enables higher performing battery powered instrumentation devices
 - Hi-Z mode allows for lower power conditioning circuitry
 - ADC power scales linearly with throughput
 - Simplify signal chain BOM
 - Small footprint for handheld devices



Go Beyond Silicon: Design Resources

- ▶ Data Sheet
- ▶ EVAL-AD400xFMCZ Boards
 - Needs EVAL-SDP-CH1Z controller board
- ▶ Companion Products
 - ADC Drivers: [ADA4807-1](#), [ADA4805-1](#), [ADA4897-1](#), [ADA4940-1](#)
 - Reference Buffer: [ADA4807-1](#)
 - Instrumentation Amplifier: [AD825x](#)
 - Reference: [ADR45XX](#), [ADR43X](#), [ADR345X](#)
 - Multiplexer: [ADG5207](#), [ADG120x](#)
 - Isolator: [ADuM141E](#)
 - LDO: [ADP7118](#)
- ▶ CN-0385: 18-bit, 2MPS Isolated Multiplexed Data Acquisition System
- ▶ IBIS Model
- ▶ FPGA Code
- ▶ Technical Article on Analog Dialogue (To be published in Dec 2016)
- ▶ Engineer Zone: [Precision ADCs](#)



EVAL-AD400xFMCZ

EVAL-SDP-CH1Z

AD4020: 20-Bit, 1MSPS Precision SAR ADC

Benefits and Features

► Ease of Use

► High Performance

- INL: **± 3 ppm** Max Guaranteed
- DNL: 20-bit No Missing Codes
- Throughput: 1 MSPS
- SNR: 101dB typ @ 1Khz
- THD: -123dB typ @ 1Khz

► True differential analog input range: $\pm V_{REF}$

- 0 V to V_{REF} with V_{REF} between 2.4 V to 5.1 V

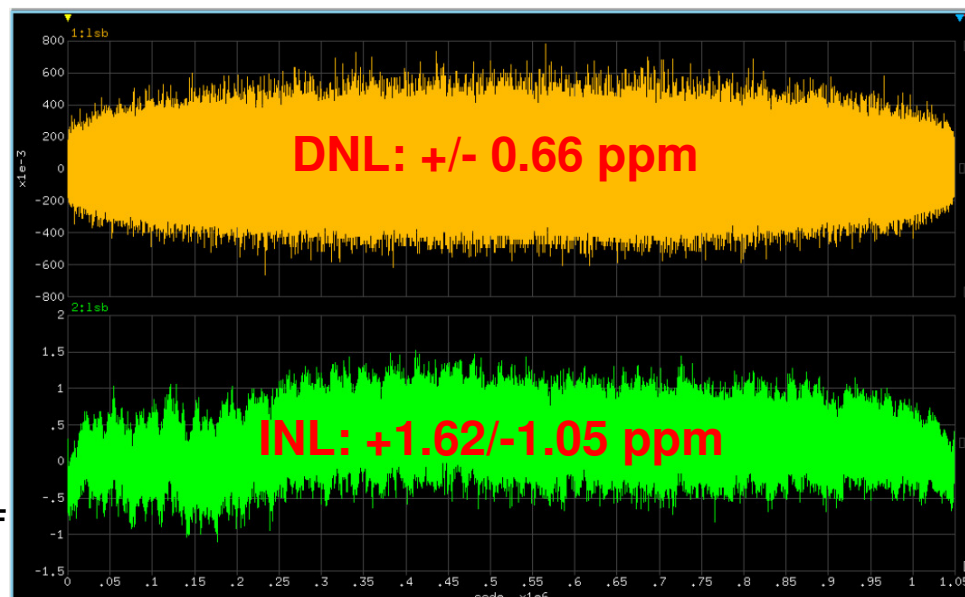
► Low Power

- 12 mW typ @ 1MSPS (Total)

► Small Form Factor

► Guaranteed Operation: - 40°C to +125°C

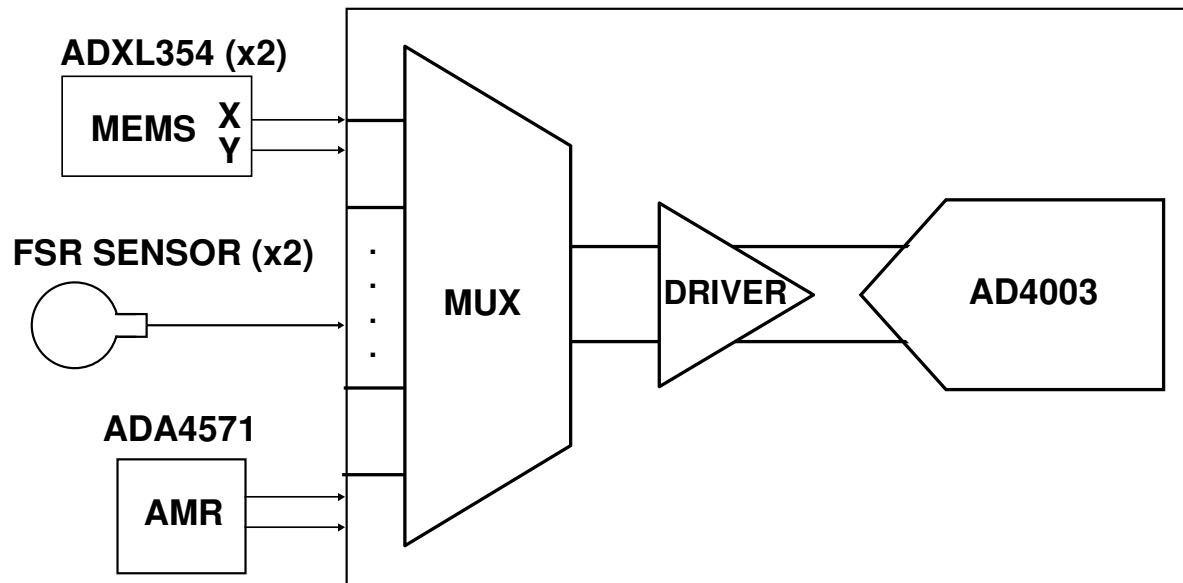
Preliminary Results: Typical Linearity Plot



Resolution	VREF	VDD	Interface	Input	Package
20 Bits	2.4V to 5.1V	1.8V	SPI 1.8V/2.5V/3V/5V	Differential $\pm V_{REF}$	10-Icd MSOP 3x4.9mm 10-Icd LFCSP 3x3mm

Structural Health Monitoring Demo

- AD4003 is used within a high precision data acquisition solution to sequentially digitise multiple sensor types that monitor vitals of railway tracks.
- Accelerometer (ADXL354), AMR Magnetic Sensor (ADA4571), Force/Pressure Sensor
- Results sent to Cloud, displayed on Dashboard



Conclusion

► The AD400x family

- 16/18/20-bits SAR ADCs
 - Pin-for-pin compatible with AD798x/AD769x ADC Family
- Pseudo-differential / Differential analog inputs
 - **AD4000**: 16-bit, 2MSPS Pseudo-Differential Precision SAR ADC (Released)
- Different sample rate grades

► Ease of Use Features

- High input impedance mode and span compression reduces the design challenge associated with the ADC driver stage and increases the flexibility in amplifier selection.
- Low SPI clock rate reduces latency requirements on digital isolators

► High Performance

- Improves measurement accuracy, sensitivity and repeatability
- High throughput improves control loop response time

QUESTIONS