



Mixed Signal Digital Pre-Distortion Evaluation Platform

Preliminary Technical
Data

AD-MSDPD-9434/6641

FEATURES

- High Performance RF & Mixed Signal Transmit and Observation Signal Chains seamlessly integrated on one board.
- Full implementation of 16 bit I/Q to +15~+24 dBm RF output with 10~20dB of fine analog gain control and 300MHz of complex BW
- Observation receiver from RF to bits, 12 bits 500 MSPS
- Exportable ADC option is available.
- SERDES clock cleanup, up to 307.2 MHz
- Full clock synthesis including SERDES Tx clock synthesis
- Full LO synthesis for ZIF or CIF Tx as well as IF sampling Receive
- Optional on-board reference clock for standalone operation
- USB interface with intuitive user interface
- Interfaces for both Altera's HSMC and Xilinx' FMC mezzanine connectors

APPLICATIONS

Transmitter Development for TDD and FDD applications: MC-GSM, WCDMA, CDMA2000, TDSCDMA & LTE

GENERAL DESCRIPTION

The AD-MSDPD-9434/6641 system board provides a turnkey evaluation platform for the development of the linear and mixed signal content for high performance transmit data. The MSDPD board takes baseband I and Q data and generates an RF output signal up to +23dBm which can be passed to an external PA for transmit. Spectral purity is targeted up to MC-GSM class 1 levels of performance when coupled with a suitable digital Predistortion algorithm.

A full observation path is also included accepting the sampled RF output up to +16dBm and mixing this down to a suitable IF frequency which is digitized with a 12 bit 500 MSPS ADC.

The board can accept a SERDES network recovered clock of both n times 30.72 MHz and n times 38.4 MHz up to 307.2 MHz. If no external reference is available, an on-board 30.72 MHz reference is available. Regardless of which reference is used, the board will provide dual loop PLL cleanup, clock synthesis of ADC, DAC, FPGA, and network Transmit clocks.

The board also will synthesis local oscillators for both zero IF

AD-MSDPD-9434/6641 SYSTEM BOARD

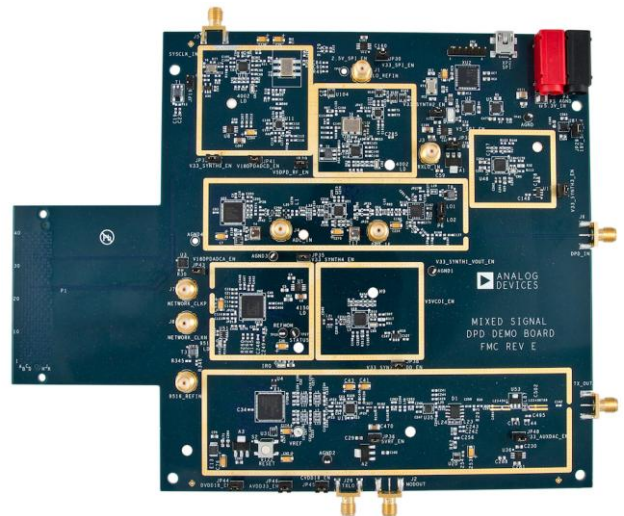


Figure 1. MSDPD System Board

and complex IF transmit as well as the local oscillator for the IF sampling observation path.

Control of the board is via USB using an intuitive user interface or by direct access from the FPGA interface when needed. Power is 5.3 volts up to 3A depending on exact configuration. An internationally compliant 6V, 3A switching power supply and a power supply unit (PSU) adapter board will be shipped with the AD-MSDPD-9434/6641 board. The PSU adapter board interfaces the 6V wall plug to the 5.3V banana jack input required by the AD-MSDPD-9434/6641 board.

The AD-MSDPD-9434/6641 highlights usage of the following leading technology products:

AD9122, ADL5375, ADL5541, ADL5320/21, AD5611, AD9434/AD6641, AD8375, ADL5365/67, AD9516, ADF4002 (2), ADF4350, ADF4351, ADCLK925, ADCLK905

Numerous other parts are showcased including regulators and control loop products.

Rev. PrA

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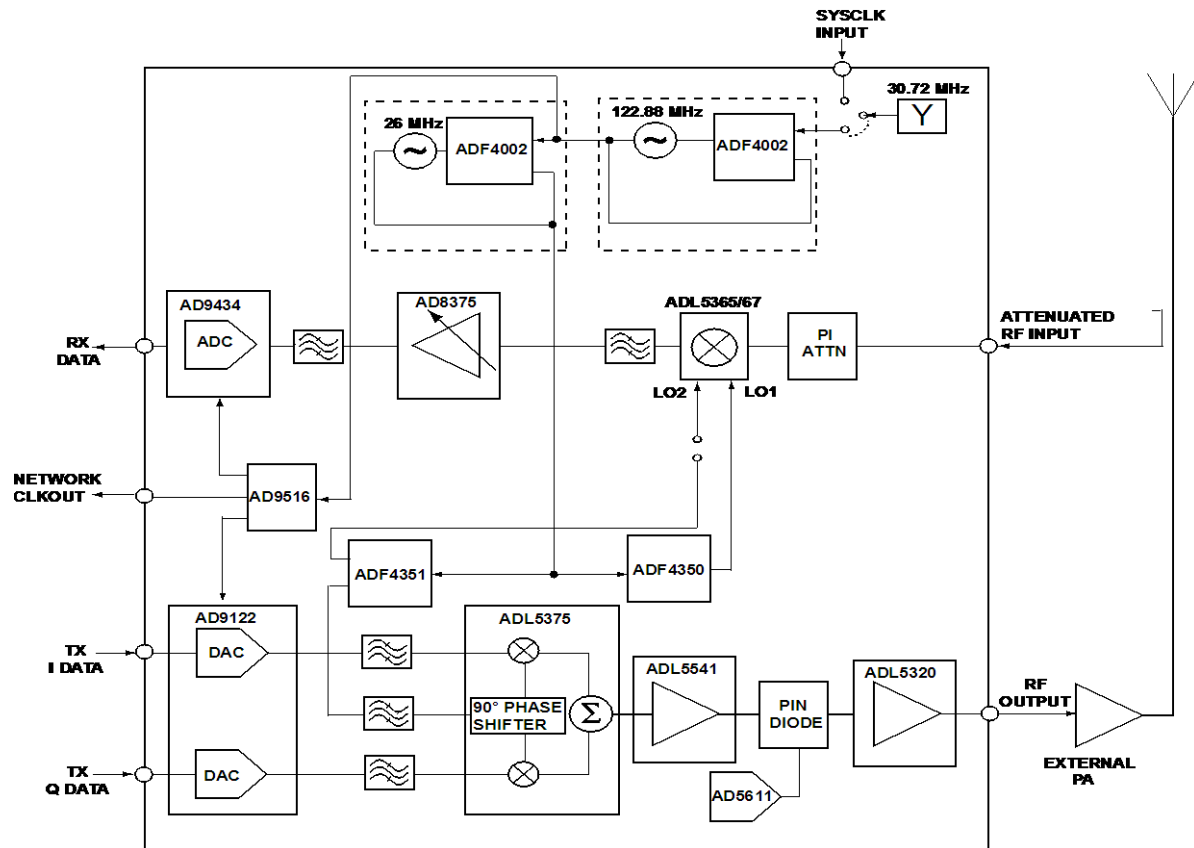


Figure 2. MSDPD Block Diagram

Table 1. Connector Descriptions

Designation	Description
J1	Auxiliary LO Reference Input
J2	Auxiliary Modulator RF Output
J3	Auxiliary Rx LO Input or Auxiliary PLL Output
J4	Auxiliary ADC Input
J5	Master Reference Clock Input
J6	Observation Input
J7	Network Clock Out P
J8	Network Clock Out N
J26	Auxiliary Tx LO Input
TX_OUT	Main Tx Output Connector
DPD_IF	Auxiliary Rx IF Output
9516_REFIN	Auxiliary Clock Reference Input
P1	Xilinx FMC Connector or Altera HSMC Connector
P3	+5.3 V supply input
P4	Power Ground
XP2	Mini USB Connector
XP1	uC Program Header

SPECIFICATIONS

VCC = 5.3 V, Master Reference Clock In=30.72 MHz 0 dBm, RFout=2.14 GHz, Pout=+5 dBm, Zout=50 ohms, Temperature = 25 °C unless otherwise noted.

POWER SPECIFICATIONS

Table 2.

	AD-MSDPD-9434/6641			
Parameter	Min	Typ	Max	Unit
POWER SUPPLIES				
Supply Voltage		5.3		V
Supply Current				
IVCC	1.6	2.5	2.9	A
POWER CONSUMPTION				
Operating Power	8.48	13.25	15.37	W

TRANSMIT SPECIFICATIONS

Table 3.

	AD-MSDPD-9434/6641			
Parameter	Min	Typ	Max	Unit
OVERALL FUNCTION				
Output Frequency Range ¹	700		2700	MHz
Zout		50		Ohms
RESOLUTION (Complex)		16		Bits
DAC Sample Rate ²		737.28		MSPS
DAC IF Output Frequency ³	-200	184.32	+200	MHz
Baseband Bandwidth		294.91		MHz
OUTPUT FREQUENCY = 748MHz				
Max Pout (1-tone, odBFS)		+24.5		dBm
Analog Gain Adjustment		25		dB
Passband Flatness		±1.9		dB
Output Noise Floor		-146		dBm/Hz
Output IMD (2-tone, 2MHz spacing, -3dBFS, Pout=11.5dBm/tone)		-60.0		dBc
Output 1dB Compression Point		24.7		dBm
4-carrier W-CDMA ACLR (Pout = -2.2dBm)				dBc
OUTPUT FREQUENCY = 880MHz				
Max Pout (1-tone, odBFS)		24.0		dBm
Analog Gain Adjustment		21		dB
Passband Flatness		±1.5		dB
Output Noise Floor		-145.8		dBm/Hz
Output IMD (2-tone, 2MHz spacing, -3dBFS, Pout=11.9dBm/tone)		-63.7		dBc
Output 1dB Compression Point		25.1		dBm
4-carrier W-CDMA ACLR (Pout = -6.0dBm)		-67.4		dBc
OUTPUT FREQUENCY = 945				
Max Pout (1-tone, odBFS)		23.5		dBm
Analog Gain Adjustment		19		dB
Passband Flatness		±1.4		dB

AD-MSDPD-9434/6641

Preliminary Technical Data

Output Noise Floor	-145.5	dBm/Hz
Output IMD (2-tone, 2MHz spacing, -3dBFS, Pout=11.3dBm/tone)	-66.5	dBc
Output 1dB Compression Point	25.1	dBm
4-carrier W-CDMA ACLR (Pout = -5.7dBm)	-66.8	dBc
OUTPUT FREQUENCY = 1850MHz		
Max Pout (1-tone, odBFS)	+20.0	dBm
Analog Gain Adjustment	16	dB
Passband Flatness	±0.9	dB
Output Noise Floor	-145	dBm/Hz
Output IMD (2-tone, 2MHz spacing, -3dBFS, Pout=13.5dBm/tone)	-61.2	dBc
Output 1dB Compression Point	24.8	dBm
4-carrier W-CDMA ACLR (Pout = -5.8dBm)	-67.4	dBc
OUTPUT FREQUENCY = 1960MHz		
Max Pout (1-tone, odBFS)	+18.5	dBm
Analog Gain Adjustment	14	dB
Passband Flatness	±1.0	dB
Output Noise Floor	-145	dBm/Hz
Output IMD (2-tone, 2MHz spacing, -3dBFS, Pout=12.8dBm/tone)	-59.1	dBc
Output 1dB Compression Point	24.6	dBm
4-carrier W-CDMA ACLR (Pout = -5.5dBm)	-67.9	dBc
OUTPUT FREQUENCY = 2140MHz		
Max Pout (1-tone, odBFS)	+17.0	dBm
Analog Gain Adjustment	13	dB
Passband Flatness	±1.0	dB
Output Noise Floor	-144.5	dBm/Hz
Output IMD (2-tone, 2MHz spacing, -3dBFS, Pout=12.4dBm/tone)	-68.9	dBc
Output 1dB Compression Point	23.4	dBm
4-carrier W-CDMA ACLR (Pout = -4.7dBm)	-67.8	dBc
OUTPUT FREQUENCY = 2350MHz		
Max Pout (1-tone, odBFS)	+17.0	dBm
Analog Gain Adjustment	12	dB
Passband Flatness	±1.0	dB
Output Noise Floor	-143.7	dBm/Hz
Output IMD (2-tone, 2MHz spacing, -3dBFS, Pout=12.7dBm/tone)	-58.6	dBc
Output 1dB Compression Point	24.1	dBm
4-carrier W-CDMA ACLR (Pout = -4.0dBm)	-68	dBc
OUTPUT FREQUENCY = 2590MHz		
Max Pout (1-tone, odBFS)	+16.5	dBm
Analog Gain Adjustment	10	dB
Passband Flatness	±1.4	dB
Output Noise Floor	-143.5	dBm/Hz
Output IMD (2-tone, 2MHz spacing, -3dBFS, Pout=12.4dBm/tone)	-58.6	dBc
Output 1dB Compression Point	24.0	dBm
4-carrier W-CDMA ACLR (Pout = -2.8dBm)	-67	dBc
OUTPUT FREQUENCY = 2660MHz		
Max Pout (1-tone, odBFS)	+16.0	dBm
Analog Gain Adjustment	10	dB

Passband Flatness	±2.0	dB
Output Noise Floor	-143.2	dBm/Hz
Output IMD (2-tone, 2MHz spacing, -3dBFS, Pout=11.9dBm/tone)	-56.8	dBc
Output 1dB Compression Point	23.5	dBm
4-carrier W-CDMA ACLR (Pout = -3.4dBm)	-66.6	dBc

1. Exact RF output frequency is determined by device selection. See ordering guide for details.
2. Other frequencies are also supported.
3. The board supports zero IF as well as complex IF. The default is complex IF with an IF frequency of 184.32 MHz.

OBSERVATION SPECIFICATIONS

Table 4.

	AD-MSDPD-9434/6641			
Parameter	Min	Typ	Max	Unit

Parameter	AD-MSDPD-9434/6641			Unit
	Min	Typ	Max	
OVERALL FUNCTION				
Resolution (Real)		12		Bits
ADC Sample Rate ¹		491.52		MSPS
ADC IF Input Frequency ²		368.64		MHz
Bandwidth		245.76		MHz
Zin		50		Ohms
Analog Gain Adjustment		24		dB
INPUT FREQUENCY = 748MHz				
Passband Flatness		±1		dB
Maximum Pin				dBm
Input Referred Noise Floor				dBFS/Hz
SFDR (-1dBFS Tone)				dBc
SNRFS (-1dBFS Tone)				dB
Input IMD (-7dBFS/Tone)				dBc
INPUT FREQUENCY = 880MHz				
Passband Flatness		±1		dB
Maximum Pin				dBm
Input Referred Noise Floor				dBFS/Hz
SFDR (-1dBFS Tone)				dBc
SNRFS (-1dBFS Tone)				dB
Input IMD (-7dBFS/Tone)				dBc
INPUT FREQUENCY = 945MHz				
Passband Flatness		±1		dB
Maximum Pin				dBm
Input Referred Noise Floor				dBFS/Hz
SFDR (-1dBFS Tone)				dBc
SNRFS (-1dBFS Tone)				dB
Input IMD (-7dBFS/Tone)				dBc
INPUT FREQUENCY = 1850MHz				
Passband Flatness		±1		dB
Maximum Pin				dBm
Input Referred Noise Floor		-141.5		dBFS/Hz
SFDR (-1dBFS Tone)		68		dBc
SNRFS (-1dBFS Tone)		57.5		dB
Input IMD (-7dBFS/Tone)		-63		dBc
INPUT FREQUENCY = 1960MHz				
Passband Flatness		±1		dB
Maximum Pin				dBm
Input Referred Noise Floor		-141.5		dBFS/Hz
SFDR (-1dBFS Tone)		68		dBc
SNRFS (-1dBFS Tone)		57.5		dB
Input IMD (-7dBFS/Tone)		-64		dBc
INPUT FREQUENCY = 2140MHz				
Passband Flatness		±1		dB
Maximum Pin				dBm
Input Referred Noise Floor		-140		dBFS/Hz
SFDR (-1dBFS Tone)		68		dBc
SNRFS (-1dBFS Tone)		56		dB

	AD-MSDPD-9434/6641			
Parameter	Min	Typ	Max	Unit
Input IMD (-7dBFS/Tone)		-60		dBc
INPUT FREQUENCY = 2350MHz				
Passband Flatness		±1		dB
Maximum Pin				dBm
Input Referred Noise Floor		-141.5		dBFS/Hz
SFDR (-1dBFS Tone)		69		dBc
SNRFS (-1dBFS Tone)		57		dB
Input IMD (-7dBFS/Tone)		-65		dBc
INPUT FREQUENCY = 2590MHz				
Passband Flatness		±1		dB
Maximum Pin				dBm
Input Referred Noise Floor		-141		dBFS/Hz
SFDR (-1dBFS Tone)		68		dBc
SNRFS (-1dBFS Tone)		56.5		dB
Input IMD (-7dBFS/Tone)		-59		dBc
INPUT FREQUENCY = 2660MHz				
Passband Flatness		±1		dB
Maximum Pin				dBm
Input Referred Noise Floor		-141		dBFS/Hz
SFDR (-1dBFS Tone)		67		dBc
SNRFS (-1dBFS Tone)		57		dB
Input IMD (-7dBFS/Tone)		-56		dBc

1. Other frequencies are also supported up to 491.52 MSPS.
2. The default IF is 368.64 MHz but can be changed by application.

CLOCK SPECIFICATIONS

Table 5.

	AD-MSDPD-9434/6641			
Parameter	Min	Typ	Max	Unit
Reference Frequency ¹	30.72		307.2	MHz
Cleanup Clock Reference Frequency ²		122.88		MHz
LO Reference Frequency ³		26.0		MHz
Clock Synthesizer Reference Frequency ⁴		2949.12		MHz
ADC Sample Rate ⁴		491.52		MSPS
DAC Sample Rate ⁴		737.28		MSPS

1. Supported Frequencies include n times 30.72 as well as n times 38.4 MHz.
2. 122.88 MHz is the installed Reference. 61.44 MHz is also supported.
3. 26.0 MHz is the installed Reference. 13.0 MHz is also supported.
4. Other frequencies can also be used.

TYPICAL PERFORMANCE CHARACTERISTICS

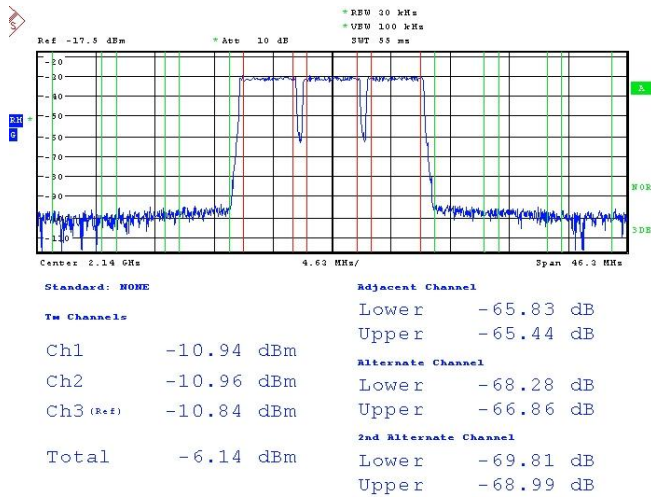


Figure 3. 3 Carrier LTE Output

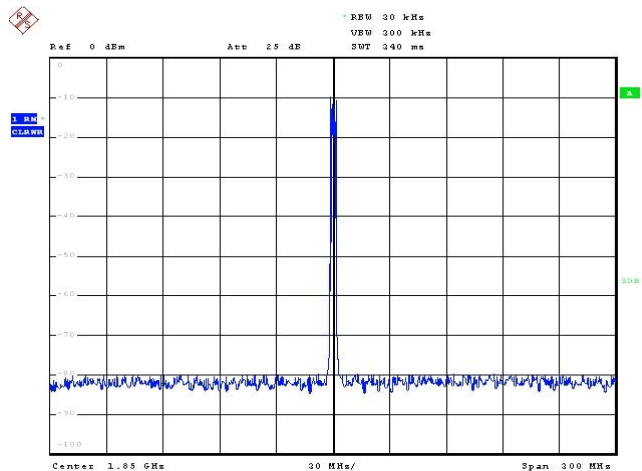


Figure 4. 6 Carrier GSM Wideband Output

Figure 5. 20 MHz LTE Output

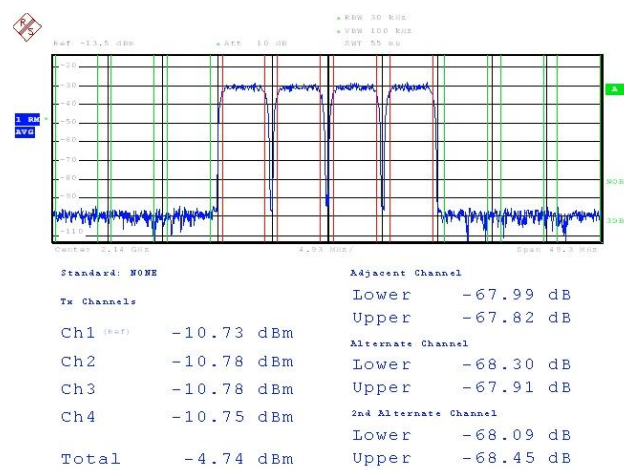


Figure 6. 4 Carrier WCDMA Output

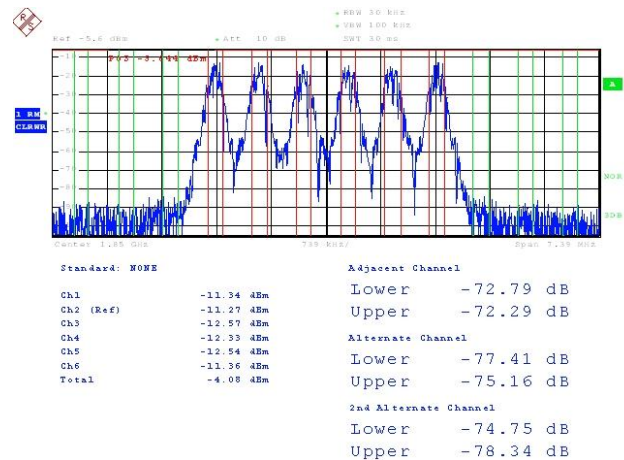


Figure 7. 6 Carrier GSM Output



Figure 8. 4 Carrier WCDMA Loopback Performance

THEORY OF OPERATION

MAIN TX PATH

The transmit path is responsible for taking complex I and Q signals and converting these into an appropriate RF signal. This is accomplished by using the modulation capabilities built into the AD9122 high-speed DAC. The DAC up-samples the data to 737.28 MSPS and applies a frequency translation of 184.32 MHz to the data stream. While zero IF may be used, using complex IF shifts the main signal away from DC where LO feedthrough and images can be easily filtered and otherwise mitigated.

The complex analog output from the DAC feeds an ADL5375 quadrature modulator via an appropriate filter and matching stage where it is translated to the specified RF output frequency. This signal is then passed to an ADL5541 for gain followed by a PIN diode for power control and finally to an ADL5320 to drive the output. RF output power control is accomplished either by adjusting the baseband data or by controlling the voltage on the PIN diode through a nanoDAC AD5611.

RF outputs from 700MHz to 2700 MHz can be synthesized with this board at power levels up to +23 dBm. Analog power control of up to 20 dB can be achieved with analog gain control depending on the RF output. Additional control is achieved with baseband data control

OBSERVATION RX PATH

The observation path consists of an ADL536x mixer, which is responsible for directly mixing the observed RF signal to a suitable IF. The typical IF frequency is 368.64 MHz but can be changed based on application requirements. The IF signal is filtered and then passed to an AD8375 DVGA, which provides 24 dB of gain range. An anti-alias filter is used to remove harmonics and other out of band signals before the signal is digitized with a 12 bit 500 MSPS ADC, AD9434 or the exportable version AD6641.

CLOCK CLEANUP

An ADF4002 with a 122.88 MHz VCXO is utilized to provide clock clean-up facilities. Either the reference input comes from

the onboard 30.72 MHz reference crystal or from an external reference of n times 30.72 MHz external source or n times 38.4 MHz. Because a narrow loop filter and VCXO are used, much of the wideband noise on the reference clock is attenuated. The output of the clock cleanup function is used as a reference for the clock synthesis and LO synthesis.

CLOCK SYNTHESIS

An AD9516 uses the 122.88 MHz reference from the clock cleanup to synthesize the ADC sample clock, the DAC sample clock and all other system clocks including any signaling needed to interface to the FPGA and SERDES Tx signals. The AD9516 includes an on chip VCO that runs nominally at 2949.12 MHz and is divided down to achieve the individual clock signals used. Other VCO frequencies can be used to support other clock rates included those typically used in China.

LO SYNTHESIS

A number of options exist for local oscillator synthesis including the option to use external LO's for both the Tx and Rx path. The on-board synthesis is accomplished by first synthesizing a 26.0 MHz reference from the 122.88 MHz reference clock. This frequency is utilized because of the ease of generating 200 kHz rasters for some air standards. This is not strictly required and could be bypassed if desired but may result in odd frequency steps that would have to be accounted for by shifting the baseband data. While this is neither difficult nor impossible, many customers would rather not shift their baseband data. The 26.0 MHz reference is passed to an ADF4351 PLL with an on-chip VCO, which is used to generate the Tx local oscillator. This product is used because of the superior phase noise characteristics it provides making it suitable for multi-carrier GSM applications. In applications where the Tx and Rx IF frequencies are the same, this local oscillator may be shared. The MSDPD board supports this as an option. A second synthesizer, the ADF4350, is used to provide the Rx LO when Rx IF is different from the Tx IF. This PLL also includes an on-chip VCO. In applications where the ADF4350 is not required for the Rx LO, this synthesizer can be used to synthesize other signals needed elsewhere in the design.

USER INTERFACE

The AD-MSDPD-9434/6641 includes two integrated user interfaces. The primary interface is a simplified GUI that provides simplified access to all key registers on the board. This GUI takes high level input from the user and computes the required low-level register values. This prevents the user from being required to compute complicated equations to determine what values must be written for board operation. In addition, the GUI simplifies analog interfacing by providing controls that simplify alignment of analog functions including LO feedthrough rejection and image rejection.

The secondary interface is a complete interface to the low-level bit maps of each device on the board. This interface is not strictly required but is provided for customers who choose to change the low-level settings to optimize performance for their application. This secondary interface also enables automation with external processes such as Python, MatLAB, and LabVIEW when communications between an external process and the MSDPD controller are required.

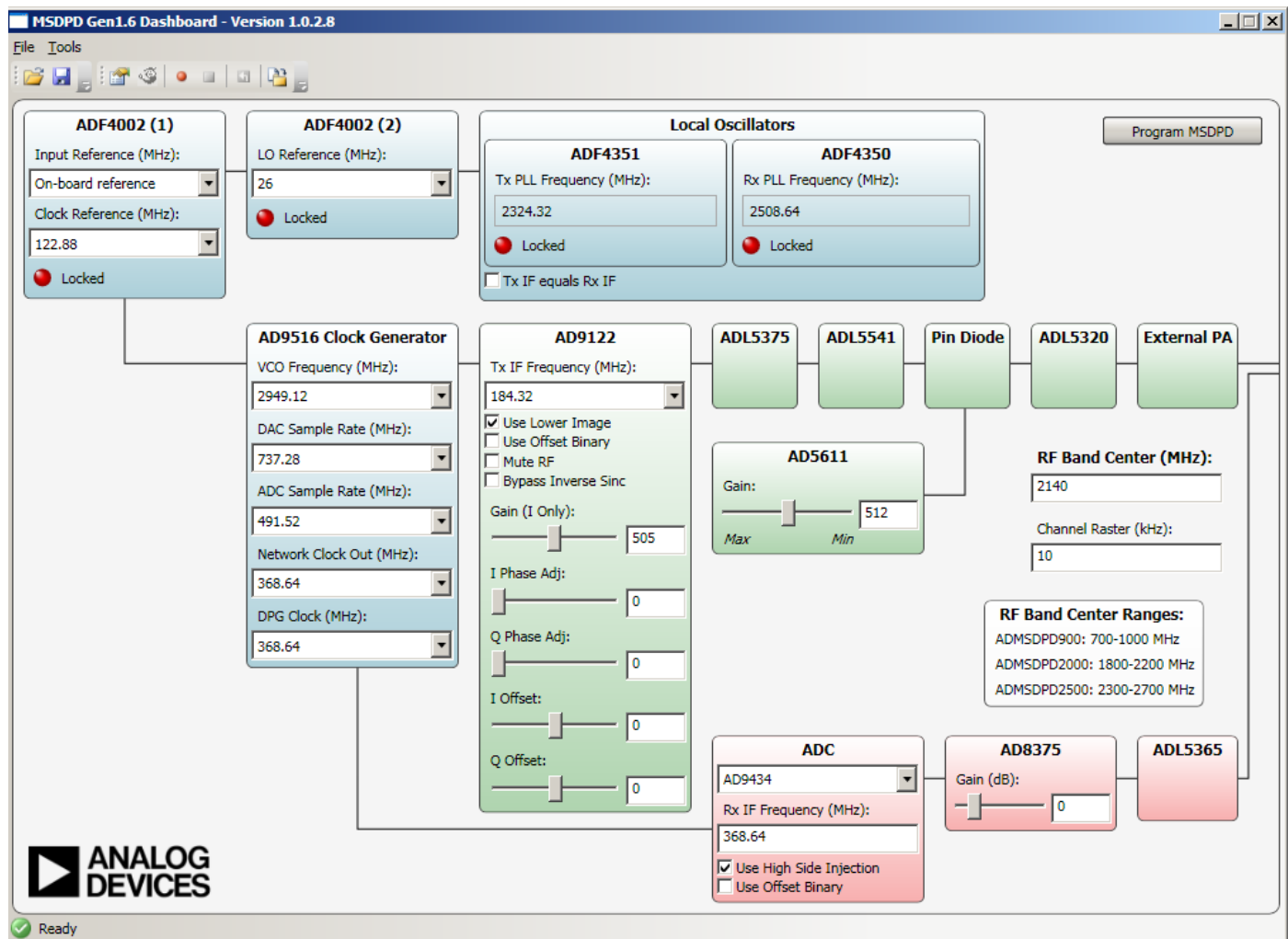


Figure 9. MSDPD Dashboard User Interface

OUTLINE DIMENSIONS

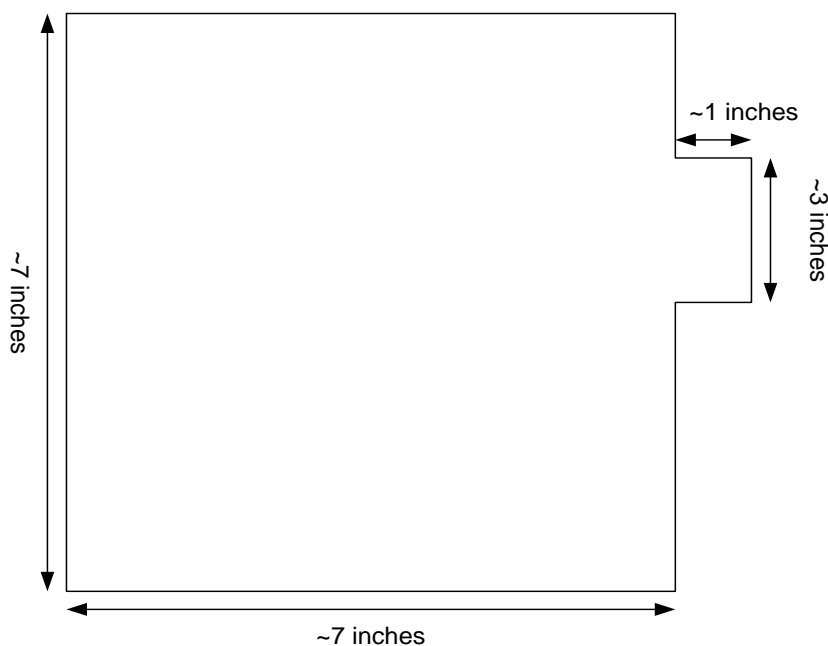


Figure 10. General Dimensions of the MSDPD

ORDERING GUIDE

Model	RF Frequency Range	Package Option
AD-MSDPDA900-9434	700 - 1000 MHz	Altera HSMC Interface
AD-MSDPDA2000-9434	1800 - 2200 MHz	Altera HSMC Interface
AD-MSDPDA900-9434	700 - 1000 MHz	Altera HSMC Interface
AD-MSDPDX900-9434	700 - 1000 MHz	Xilinx FMC Interface
AD-MSDPDX2000-9434	1800 - 2200 MHz	Xilinx FMC Interface
AD-MSDPDX2500-9434	2300 - 2700 MHz	Xilinx FMC Interface
AD-MSDPDX900-6641	700 - 1000 MHz	Xilinx FMC Interface, exportable ADC
AD-MSDPDX2000-6641	1800 - 2200 MHz	Xilinx FMC Interface, exportable ADC
AD-MSDPDX2500-6641	2300 - 2700 MHz	Xilinx FMC Interface, exportable ADC