An IQ Demodulator-Based IF-to-Baseband Receiver with IF and Baseband Variable Gain and Programmable Baseband Filtering

CIRCUIT FUNCTION AND BENEFITS

This circuit shown in Figure 1 is a flexible, frequency agile IF-to-baseband receiver. Variable gain at both IF and baseband is used to adjust the signal level. The ADRF6510 baseband ADC driver also includes a programmable low-pass filter that eliminates out-of-channel blockers and noise.

The bandwidth of this filter can be dynamically adjusted as the bandwidth of the input signal changes. This ensures that the available dynamic range of the ADC that this circuit drives is fully used.

The core of the circuit is an IQ demodulator. The 2×LO based phase-splitting architecture of the ADL5387 allows for operation over a wide frequency range. Precise quadrature balance and low output dc offsets ensure that there is minimal degradation of the error vector magnitude (EVM).

The interfaces between all of the components in this circuit are fully differential. Where dc coupling is required between stages, the bias levels of the adjacent stages are compatible with each other.

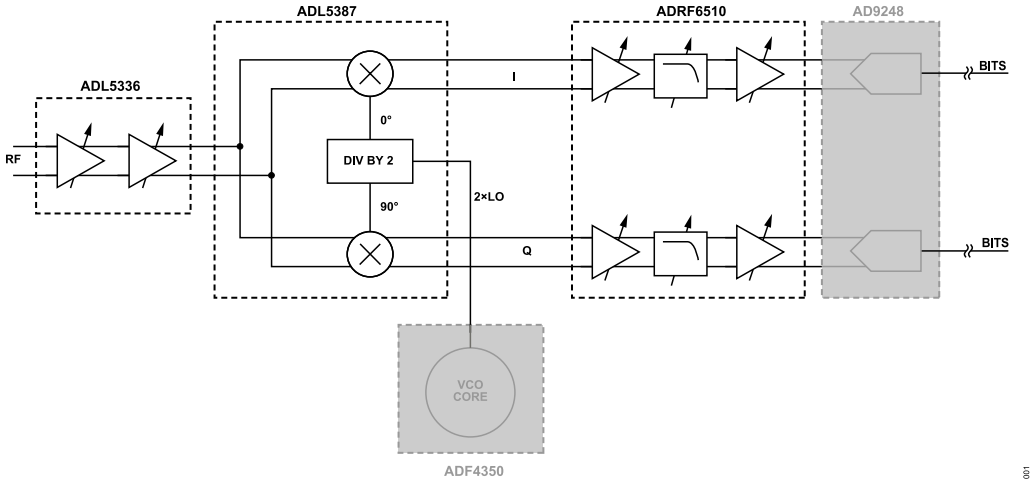

Figure 1. Direct Conversion Receiver Simplified Schematic (All Connections and Decoupling Not Shown)

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4/2012—Revision 0: Initial Version

CIRCUIT DESCRIPTION

RECEIVER ARCHITECTURE

A direct conversion (also known as a homodyne or zero IF) architecture for a receiver is presented in this circuit note. Direct conversion radios perform just one frequency translation compared to a superheterodyne receiver that can perform several frequency translations. One frequency translation is advantageous because it

- Reduces receiver complexity and the number of stages needed; increasing performance and reducing power consumption
- Avoids image rejection issues and unwanted mixing products; one LPF at baseband is all that is needed
- Has high selectivity (adjacent-channel rejection ratio [ACRR])

Figure 1 shows the basic simplified schematic of the system that consists of cascaded IF variable gain amplifiers (VGAs) with integrated automatic gain control (AGC) loops, followed by a quadrature demodulator and by programmable low-pass filters with variable baseband gain. The grayed out components shown in Figure 1 (ADF4350 and AD9248) are included for clarity but were not included during system-level measurements (see the Common Variations section for more information on these devices).

Ideally, the input of the first stage and the output of the last stage should set the dynamic range (signal-to-noise ratio) of the system. Practically, this may not be the case. Having a cascaded VGA before the quadrature demodulator not only adds more gain to the system, but it also helps with overall system noise performance if the noise figure of the VGA is less than that of the quadrature demodulator, and if the VGA still has gain, and it is not attenuating. The noise figures of the subsequent stages are divided by the gain of the initial VGA. Another benefit of having a VGA (vs. just having a fixed gain amplifier) is that an AGC loop can be designed to level the incoming signal to the quadrature demodulator. It is important to have this ability to limit the signal levels applied to the quadrature demodulator and any subsequent stages.

IF VGAS AND AGC LOOPS

The IF VGA and AGC loop functions are accomplished with the ADL5336. It has two cascadable VGAs, each with 24 dB of analog dynamic range and the ability to digitally change the maximum gain on each VGA via a SPI port.

To achieve the signal leveling AGC function, each ADL5336 VGA has a square law detector connected to its output through a programmable attenuator. The detector compares the output of the attenuator to an internal reference of 63 mV rms. If there is a difference between the output of the attenuator and the 63 mV rms reference, an error current is produced and is integrated onto a C_{AGC} capacitor. The AGC loop is closed by connecting the DTO1/DTO2 pin to the GAIN1/GAIN2 pin. For the AGC loop to function properly, pull the MODE pin low, causing a negative VGA gain slope.

Each ADL5336 VGA has an allowable range of input power over which the AGC will level to a particular setpoint. Outside that range, the VGA output either increases or decreases dB-for-dB with the input (assuming the VGA is not in compression or that the signal is not in the noise floor).

IQ DEMODULATOR

From the ADL5336, the signal is routed to the ADL5387, where it is demodulated and the frequency is translated to a zero IF. The ADF4350 synthesizer can provide the required 2×LO signal to the ADL5387 (see the Common Variations section); however, a signal generator was used instead of the ADF4350 for actual testing.

The ADL5387 uses two double-balanced mixers, one for the I channel and one for the Q channel. The LO provided to the mixers is generated using a divide-by-two quadrature phase splitter. This provides the 0° and 90° signals for the I and Q channels. There is about 4.5 dB of conversion gain provided by the ADL5387 from the RF input to the baseband I and Q outputs.

LOW-PASS FILTER, BASEBAND VGA, AND ADC DRIVER

The low-pass filtering, baseband gain, and ADC driver functions are all achieved using the ADRF6510. The signal, now in its separate I and Q paths, is applied to the ADRF6510 where the signal is first amplified by the preamplifier, then low-pass filtered to suppress any unwanted out-of-band signals and/or noise, and finally amplified by the VGA.

Each channel of the ADRF6510 can be broken up into three stages:

- Preamplifier
- Programmable low-pass filter
- VGA and output driver

The preamplifier has a user-selectable gain, via the GNSW pin, of either 6 dB or 12 dB. The low-pass filter can be programmed for a corner frequency of 1 MHz to 30 MHz in 1 MHz steps via the SPI port. The VGA has a 50 dB gain range with a gain slope of 30 mV/dB. The gain of the VGA is controlled via the GAIN pin, and it can range from −5 dB to +45 dB when the GNSW pin is pulled low to +1 dB to +51 dB when the GNSW pin is pulled high. The output driver has the ability to drive 1.5 V p-p differential into a 1 kΩ load while maintaining a HD2 and a HD3 of better than 60 dBc.

The maximum CW signal that can be applied to the low-pass filters, while still maintaining acceptable HD levels in the ADRF6510, is 2 V p-p. In applications where a large out-of-band interferer is present that could overload the input of either the ADL5387 and/or the ADRF6510, the out-of-band interferer (and the in-band desired signal) can be attenuated by the ADL5336 VGA. Once the out of-band interferer is rejected by the low-pass filter of the ADRF6510, the wanted signal can then be amplified with the X-AMP VGAs that follow the filters of the ADRF6510.

From the ADRF6510, the IQ signal can be applied to an appropriate analog-to-digital converter (ADC), such as the AD9248.

MEASUREMENT RESULTS

A 4-QAM, 5 MSPS modulated signal was applied to the input of the ADL5336.

EVM is a measure of the quality of the performance of a digital transmitter or receiver and is a measure of the deviation of the actual constellation points from their ideal locations, due to both magnitude and phase errors. This is shown in Figure 2.

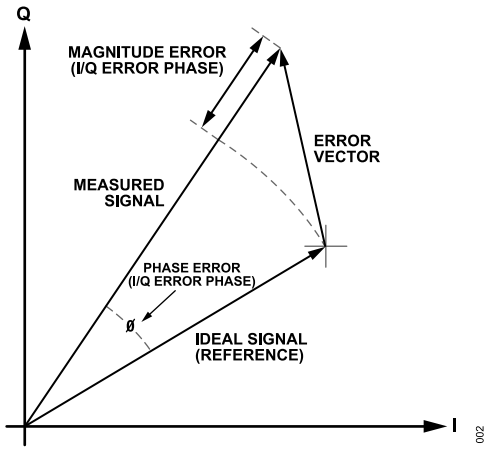

Figure 2. EVM Plot

Figure 3 shows the system EVM vs. the input power to the ADL5336 while the maximum gains on the VGAs are set to 15.2 dB and 19.5 dB for VGA1 and VGA2, respectively. Several AGC setpoint combinations were tested. Figure 4 is also system EVM vs. the input power to the ADL5336; however, the gain of the VGA's was set 9.7 dB and 13.4 dB, respectively. The same AGC setpoint combinations were tested.

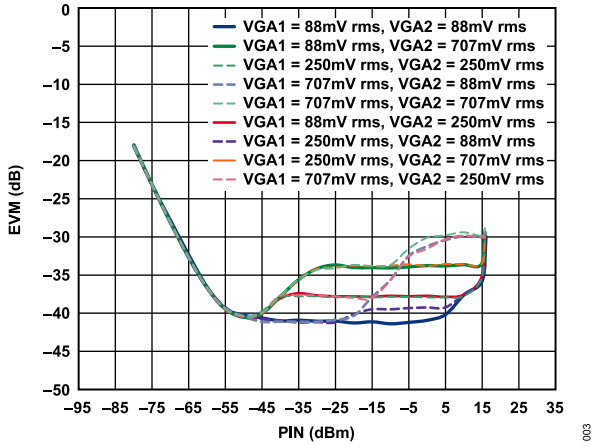

Figure 3. System EVM, Digital VGA Gains = 11

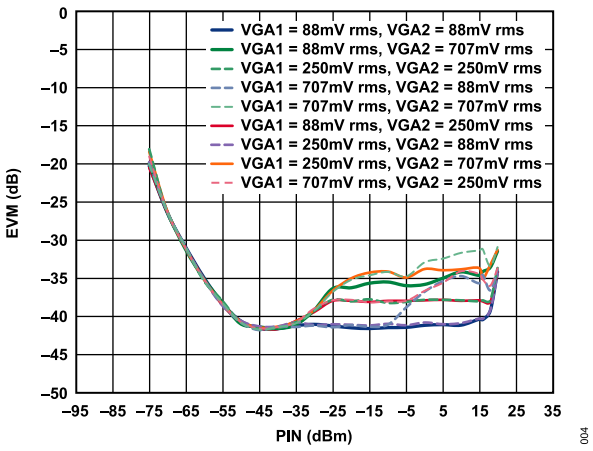

Figure 4. System EVM, Digital VGA Gains = 00

Figure 3 and Figure 4 illustrate the importance of keeping the signal levels applied to the ADRF6510 low enough not to compress the input stage and/or filter. At the highest of AGC setpoints (500 mV rms and 707 mV rms), the input of the ADL5387 IQ demodulator is starting to compress and adds additional degradation to the EVM. The best EVM is achieved when the AGC setpoints are at their lowest (88 mV rms). EVM is already beginning to degrade when the setpoints are 250 mV rms.

Figure 5 compares the EVM between the minimum and the maximum digital gain settings (both VGAs were set to either a gain code of 11 or a gain code of 00) on the ADL5336 VGAs when VGA1 and VGA2 setpoints are 250 mV rms and 88 mV rms, respectively.

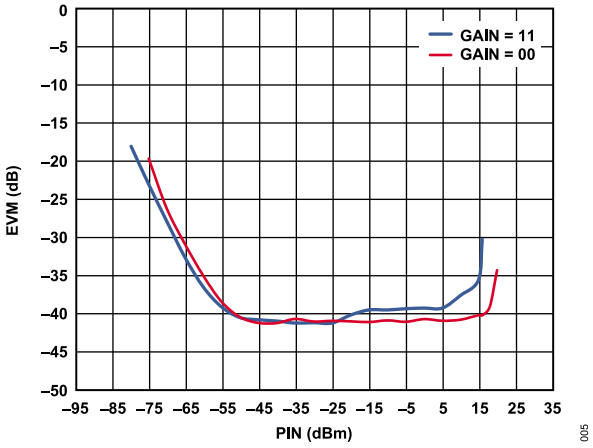

Figure 5. System EVM with VGA1 Setpoint = 250 mV rms and VGA2 Setpoint = 88 mV rms

For the given AGC setpoints, when the maximum gain code was 11, the handoff from VGA2 to VGA1 occurs after VGA2 runs out of the gain range; therefore, the signal level being applied to the ADRF6510 continues to increase (and degrade EVM) until VGA1 reaches its setpoint. Once VGA1 reaches its own setpoint, the EVM levels off again; therefore, the signal level being applied to the ADRF6510 does not change until VGA1 runs out of the gain range at about 5 dBm of input power. When the maximum gain code was set to 00, both VGAs have more attenuation available,

thus allowing VGA2 to shift its dynamic range such that it does not reach its setpoint at as low an input power as when the maximum gain code was 11. This allows VGA2 to keep its setpoint at higher input powers, thus allowing the handoff from VGA2 to VGA1 to take place before VGA2 runs out of gain. This ensures that the signal level applied to the ADRF6510 is maintained at a constant level until the uppermost of the input power range.

Figure 6 compares the EVM between the minimum and the maximum digital gain settings (both VGAs were set to either a gain code of 11 or a gain code of 00) on the ADL5336 VGAs; however, the VGA1 and VGA2 setpoints were 707 mV rms and 88 mV rms, respectively.

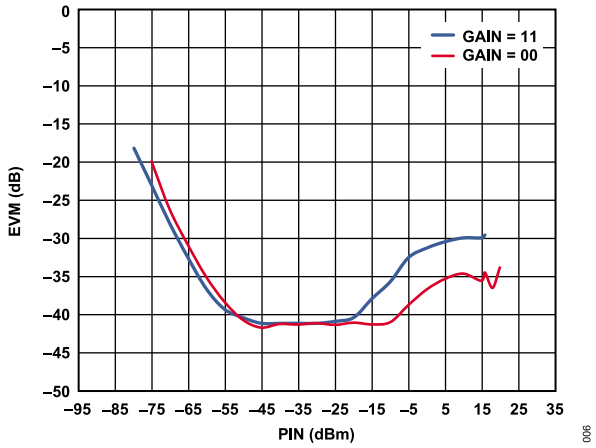

Figure 6. System EVM with VGA1 Setpoint = 707 mV rms and VGA2 Setpoint = 88 mV rms

The same dynamics are occurring in Figure 6 as they were in Figure 5, only they are much more exaggerated. When the maximum gain code is 00, VGA2 reaches its setpoint at around −40 dBm input power. It maintains its setpoint until about −10 dBm, at which point, VGA1 has not reached its setpoint of 707 mV rms. VGA1 does not reach its setpoint until about 0 dBm, and the EVM starts to level off somewhat. When the maximum gain is set to 11, this same behavior happens again; however, VGA2 maintains its setpoint only to about −20 dBm because there is more gain available to attain the prescribed setpoints.

COMMON VARIATIONS

SYSTEM SYNTHESIZER

The signal generator that provides the 2×LO for the ADL5387 can be replaced by a wideband synthesizer, such as the ADF4350, which has an integrated VCO. The ADF4350 belongs to a family of synthesizers that operate over a wide frequency range, from 135 MHz to 4350 MHz, and that has varying phase noise and output power metrics, making it easy to find the device to match the required specifications of the application.

SYSTEM ADC

Adding an ADC to the system to sample the I and Q signals of the ADRF6510 is a natural progression to complete the analog signal chain. A dual ADC, such as the AD9248, provides 14 bits of resolution and is offered in 20 MSPS, 40 MSPS, or 65 MSPS sampling rates. An antialiasing filter is recommended between the output of the ADRF6510 and the AD9248. Refer to the ADRF6510 data sheet for the antialiasing filter design example.

ADRF6510 OUTPUT COMMON-MODE VOLTAGE CONSIDERATIONS

The ADRF6510 output common-mode voltage is adjustable from 1.5 V to 3.0 V without loss of drive capability. Many modern ADCs have input common-mode voltages of less than 1.5 V. Driving the VOCM pin to an output common-mode voltage less than 1.5 V starts to degrade the distortion performance of the ADRF6510; however, it is still functional for less than 1.5 V common-mode voltage levels. To maintain distortion performance, a dc level shifting circuit may be required, or an integrated filter and VGA device with a lower common-mode voltage, such as the ADRF6516, can be used.