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# Analog Dialogue

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ANALOG DEVICES

# Editors' Notes

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Precision instruments that measure physical properties using a photodiode or other current-output sensor often include a transimpedance amplifier (TIA) and a programmable-gain stage to maximize dynamic range. This article shows the benefits and challenges of implementing a single-stage programmable-gain TIA to minimize noise while maintaining high bandwidth and accuracy. (Page 11)

### Choose Resistors to Minimize Errors in Grounded-Load Current Source

Operational amplifiers are often used to make high-quality current sources. In industrial applications, they are widely used to provide 4 mA to 20 mA currents. The improved Howland current source is very popular because it can drive a grounded load. Its accuracy is determined by the amplifier and the resistors. This article shows how to choose the external resistors to minimize errors. (Page 16)

### Voltage Reference Design for Precision Successive-Approximation ADCs

The precision of a high-resolution successive-approximation ADC depends on the accuracy, stability, and drive capability of its voltage reference. The reference sees a dynamic load, so it must be able to handle time- and throughput-dependent currents. The best performance can usually be achieved with an external reference, so this article looks at the challenges and design requirements. (Page 17)

### Complete Sensor-to-Bits Solution Simplifies Industrial Data-Acquisition System Design

At the heart of many industrial automation and process-control systems, programmable logic controllers employ multiple sensors and actuators to measure and control analog process variables such as pressure, temperature, and flow. This article shows how the highly integrated ADAS3022 reduces complexity, facilitating the design of multichannel data-acquisition systems. (Page 21)

### A Tribute to Jerry Fishman

On March 28, 2013, Jerry Fishman, our CEO, colleague, and friend, passed away peacefully after a sudden heart attack. Jerry joined Analog Devices in 1971 as a product marketing engineer. He was promoted to president and COO in 1991 and to CEO in 1996. We celebrate his 42-year career at ADI. (Page 25)

*Scott Wayne* [scott.wayne@analog.com]

## PRODUCT INTRODUCTIONS: VOLUME 47, NUMBER 2

*Data sheets for all ADI products can be found by entering the part number in the search box at www.analog.com.*

### April

**Amplifier**, error, isolated, high-performance ..... **ADuM3190**

**Controller**, digital, for isolated power supplies ..... **ADP1046A**

**DAC**, 14-bit, 32-channel, 50 V to 200 V full-scale ..... **AD5535B**

**DAC**, dual, 12-bit *nano*DAC+,™ 2-ppm/°C reference ..... **AD5697R**

**DACs**, quad, 12-/16-bit *nano*DAC+ ..... **AD5687/AD5689**

**DACs**, dual, 10-bit *nano*DAC,®
2-ppm/°C reference ..... **AD5313R/AD5338R**

**DACs**, dual, 12-/16-bit *nano*DAC+,
2-ppm/°C reference ..... **AD5687R/AD5689R**

### May

**Decoder**, keypad, and I/O port expander ..... **ADP5586**

**Detector**, rms power, 10-MHz to 10-GHz ..... **ADL5906**

**Switch**, power, high-side, logic-level control ..... **ADP196**

### June

**ADC**, pipelined, 14-bit, 170-/250-MSPS, JESD204B ..... **AD9683**

**Amplifier**, difference, precision, very high CMV ..... **AD8479**

**Amplifier**, instrumentation, precision, low-power ..... **AD8422**

**Amplifier**, variable-gain, 18-MHz, low-power ..... **AD8338**

**DAS**, 8-channel, 16-bit, simultaneous sampling ..... **ADAS3023**

**Gain Blocks**, RF/IF, 30-MHz to 6-GHz ..... **ADL5544/ADL5545**

**Microphone**, MEMS, high SPL, analog-output ..... **ADMP411**

**Receiver**, IF, 80-MHz bandwidth ..... **AD6677**

**Regulator**, linear, low-noise, –28 V at –200 mA ..... **ADP7182**

**Switch**, load, high-side, 500-mA, quad signal switch ..... **ADP1190**


## Analog Dialogue

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# Multipliers vs. Modulators

By James Bryant

Although many descriptions of modulation describe it as a multiplication process, the truth is a bit more complex.

First, to be quite clear, if the two inputs of a perfect *multiplier* were fed with a signal, Acos(ωt), and an unmodulated carrier, cos(ωt), we would have a *modulator*. This happens because the two periodic waveforms, $A_s\cos(\omega_s t)$ and $A_c\cos(\omega_c t)$, applied to the inputs of a multiplier (with a scale factor of 1 V for simplicity of analysis), produce an output given by:

$$V_o(t) = \tfrac{1}{2}A_sA_c[\cos((\omega_s + \omega_c)t) + \cos(\omega_s - \omega_c)t))]$$

If the carrier, $A_c\cos(\omega_c t)$, has 1 V amplitude ($A_c = 1$), this further simplifies to:

$$V_o(t) = \tfrac{1}{2}A_s[\cos((\omega_s + \omega_c)t) + \cos((\omega_s - \omega_c)t)]$$

But, in most cases, a modulator is a better circuit to perform this function. A modulator (also called a *mixer* when it is used as a frequency changer) is closely related to a multiplier. The output of a multiplier is the instantaneous product of its inputs. The output of a modulator is the instantaneous product of the *signal* on one of its inputs (known as the *signal* input) and the *sign of the signal* on the other input (known as the *carrier* input). Figure 1 shows two ways of modeling the modulation function: as an amplifier whose gain is switched positive and negative by the output of a comparator on its carrier input, or as a multiplier with a high-gain limiting amplifier between the carrier input and one of its ports. Both architectures have been used to produce modulators, but the switched amplifier version (used in the AD630 balanced modulator) tends to be slower. Most high-speed integrated circuit modulators consist of a translinear multiplier (based on the Gilbert cell) with a limiting amplifier in the carrier path overdriving one of the inputs. This limiting amplifier may provide high gain, allowing a low-level carrier input; or low gain and clean limiting characteristics, thus requiring a comparatively large carrier input for correct operation. Consult the data sheet for specific information.

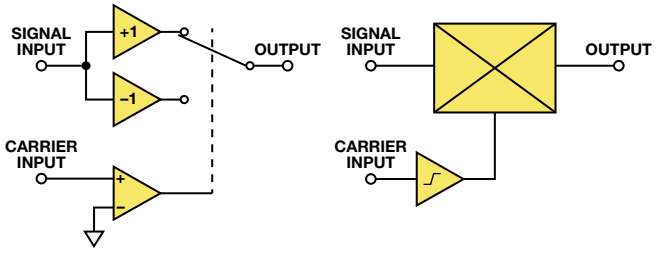


Figure 1. Two ways of modeling the modulation function.

We use modulators rather than multipliers for several reasons. Both ports of a multiplier are linear, so any noise or modulation on the carrier input multiplies the signal input and degrades the output, while amplitude variation on the carrier input of a modulator can mostly be ignored. Second-order mechanisms can cause amplitude noise on the carrier input to affect the output, but these are minimized in the best modulators and will not be discussed here. A simple model of a modulator uses switches driven by the carrier. An (perfect) open switch has infinite resistance and zero thermal noise current, and a (perfect) closed switch has zero resistance and zero thermal noise voltage, so modulators, even though their switches are less than perfect, tend to have less internal noise than multipliers. Also, it is easier to design and manufacture a high-performance, high-frequency modulator than a similar multiplier.

Like analog multipliers, modulators multiply two signals, but, unlike analog multipliers, the multiplication is not linear. Instead, the signal input is multiplied by +1 when the polarity of the carrier input is positive, and by –1 when it is negative. In other words, the signal is multiplied by a square wave at the carrier frequency.

A square wave with a frequency of $\omega_c t$ may be represented by the Fourier series of odd harmonics:

$$K[\cos(\omega_c t) - 1/3\cos(3\omega_c t) + 1/5\cos(5\omega_c t) - 1/7\cos(7\omega_c t) + \ldots]$$

The sum of the series: [+1, –1/3, +1/5, –1/7 + ...] is π/4. Therefore, the value of K is 4/π, such that a balanced modulator acts as a unity gain amplifier when a positive dc signal is applied to its carrier input.

The carrier amplitude is unimportant as long as it is large enough to drive the limiting amplifier, so a modulator driven by a signal, $A_s\cos(\omega_s t)$, and a carrier, $\cos(\omega_c t)$, will produce an output that is the product of the signal and the squared carrier:

$$2A_s/\pi[\cos(\omega_s + \omega_c)t + \cos(\omega_s - \omega_c)t -$$
$$1/3\{\cos(\omega_s + 3\omega_c)t + \cos(\omega_s - 3\omega_c)t\} +$$
$$1/5\{\cos(\omega_s + 5\omega_c)t + \cos(\omega_s - 5\omega_c)t\} -$$
$$1/7\{\cos(\omega_s + 7\omega_c)t + \cos(\omega_s - 7\omega_c)t\} + \ldots]$$

This output contains sum and difference frequencies of the signal and carrier, and of the signal and each of the odd harmonics of the carrier. In an ideal, perfectly balanced modulator, products of even harmonics are not present. In a real modulator, however, residual offsets on the carrier port result in low-level, even harmonic products. In many applications, a low-pass filter (LPF) removes the products of the higher harmonics. Remember that $\cos(A) = \cos(-A)$, so $\cos(\omega_m - N\omega_c)t = \cos(N\omega_c - \omega_m)t$, and we do not have to worry about "negative" frequencies. After filtering, the modulator output is given by:

$$2A_s/\pi[\cos(\omega_s + \omega_c)t + \cos(\omega_s - \omega_c)t]$$

This is the same expression as the output of a multiplier, except for a slightly different gain. In practical systems, the gain is normalized by amplifiers or attenuators, so we won't consider the theoretical gains of various systems here.

In simple cases, it's obviously better to use a modulator than a multiplier, but how do we define simple? When a modulator is used as a mixer, the signal and carrier inputs are simple sine waves at frequencies $f_1$ and $f_c$, and the unfiltered output contains the sum $(f_1 + f_c)$ and difference $(f_1 - f_c)$ frequencies, plus the sum and difference frequencies of the signal and the odd harmonics of the carrier $(f_1 + 3f_c)$, $(f_1 - 3f_c)$, $(f_1 + 5f_c)$, $(f_1 - 5f_c)$, $(f_1 + 7f_c)$, $(f_1 - 7f_c)$... After the LPF, we expect to find just the fundamental products, $(f_1 + f_c)$ and $(f_1 - f_c)$.

If $(f_1 + f_c) > (f_1 - 3f_c)$, however, it will not be possible to separate the fundamental and harmonic products with a simple LPF because one of the harmonic products is at a lower frequency than one of the fundamental products. This is not a simple case, so more analysis is needed.

If we assume that the signal contains a single frequency, $f_1$, or a more complex signal spread across the band from $f_1$ to $f_2$, we can analyze the output spectrum of our modulator, as shown in the following diagrams. Assume a perfectly balanced modulator without signal leak, carrier leak, or distortion, so that the input, carrier, and spurious products do not appear in the output. Inputs are shown in black (or in pale gray in the output diagrams, even though it is not actually present).

Figure 2 shows the inputs—a signal in the $f_1$ to $f_2$ band and a carrier at $f_c$. A multiplier won't have odd carrier harmonics at $1/3(3f_c)$, $1/5(5f_c)$, $1/7(7f_c)$ … , shown as dotted lines for the modulator. Note that the fractions 1/3, 1/5, and 1/7 refer to the amplitudes, not the frequencies.

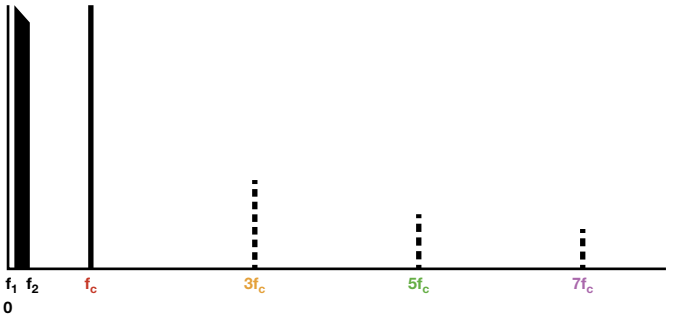


Figure 2. Input spectrum shows signal input, carrier, and odd carrier harmonics.

Figure 3 shows the output of a multiplier, or a modulator, and LPF with a cutoff frequency of $2f_c$.

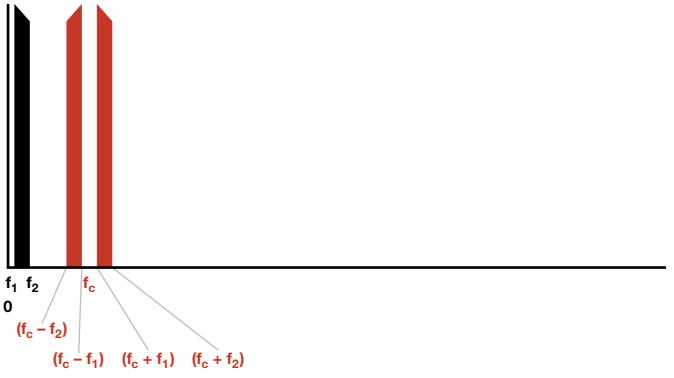


Figure 3. Output spectrum of multiplier, or modulator, plus LPF.

Figure 4 shows the output of an unfiltered modulator (but not harmonic products above $7f_c$).

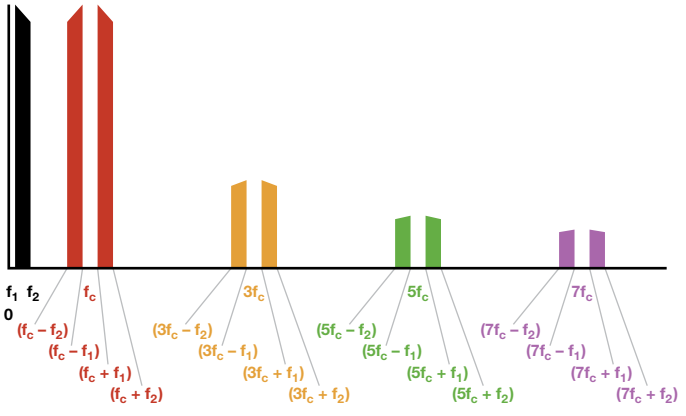


Figure 4. Output spectrum of unfiltered modulator.

If the signal band, $f_1$ to $f_2$, lies within the Nyquist band (dc to $f_c/2$), an LPF with cutoff above $2f_c$ will cause a modulator to have the same output spectrum as a multiplier. At signal frequencies above Nyquist, things become more complex.

Figure 5 shows what happens when the signal band is just below $f_c$. It is still possible to separate the harmonic products from the ones produced by the fundamental, but now it requires an LPF with very steep roll-off.

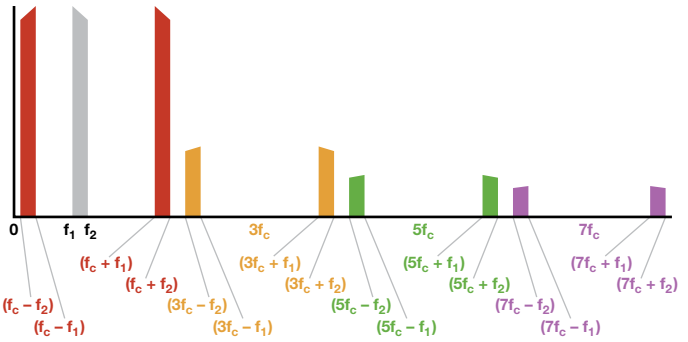


Figure 5. Output spectrum when the signal is greater than $f_c/2$.

Figure 6 shows that as the signal band passes through $f_c$, the harmonic products now overlap $(3f_c - f_1) < (f_c + f_1)$, so the fundamental products can no longer be separated from the harmonic products by an LPF. The required signals must now be selected by a band-pass filter (BPF).

Thus, although modulators are better than linear multipliers for most frequency changing applications, it is important to consider their harmonic products when designing real systems.

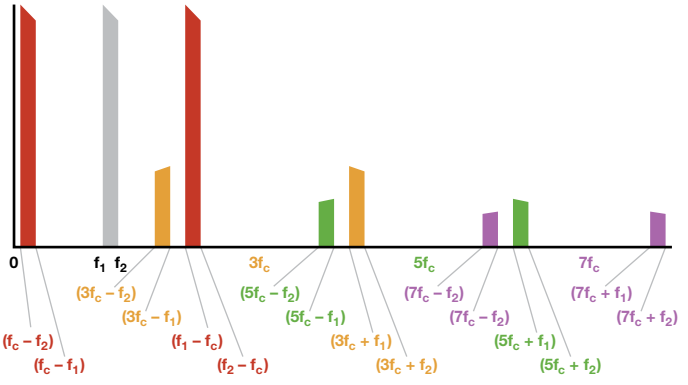


Figure 6. Output spectrum when the signal exceeds $f_c$.

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### *Product Pages*

Mixers/Multipliers
Multipliers/Dividers
Modulators/Demodulators

### *RAQs*

Multipliers and Modulators
Caveat Emptor

### *Tutorials*

MT-079 Tutorial. Analog Multipliers.
MT-080 Tutorial. Mixers and Modulators.


## Author


**James Bryant** [james@jbryant.eu] has been a European applications manager with Analog Devices since 1982. He holds a degree in physics and philosophy from the University of Leeds. He is also a C.Eng., Eur. Eng., MIEE, and an FBIS. In addition to his passion for engineering, James is a radio ham and holds the call sign G4CLF.


# Safeguard Your RS-485 Communication Networks from Harmful EMC Events

By James Scanlon and Koenraad Rutgers

**Idea In Brief**

In real industrial and instrumentation (I&I) applications, RS-485 interface links must work in harsh electromagnetic environments. Large transient voltages caused by lightning strikes, electrostatic discharge, and other electromagnetic phenomenon can damage communications ports. To ensure that these data ports can survive in their final installation environments, they must meet certain electromagnetic compatibility (EMC) regulations.

These requirements include three main transient immunity standards: electrostatic discharge, electrical fast transients, and surge.

Many EMC problems are not simple or obvious, so they must be considered at the start of the product design. Leaving these considerations to the end of the design cycle can lead to overruns in engineering budget and schedule.

This article describes each of these main transient types and presents and demonstrates three different EMC compliant solutions for three different cost/protection levels on RS-485 communication ports.

Analog Devices, Inc., and Bourns, Inc., have partnered to extend their offering of system-oriented solutions by co-developing the industry's first EMC compliant RS-485 interface design tool that provides up to Level 4 protection levels for IEC 61000-4-2 ESD, IEC 61000-4-4 EFT, and IEC 61000-4-5 surge. It gives designers the design options depending on the level of protection required and available budgets. These design tools allow designers to reduce risk of project slippage due to EMC problems by considering them at the start of the design cycle.

## RS-485 Standard

I&I applications require data transmission between multiple systems, often over very long distances. The RS-485 electrical standard is one of the most widely used physical layer specifications in I&I applications, such as industrial automation, process control, motor control, and motion control; remote terminals; building automation, such as heating, ventilation, and air conditioning (HVAC); security systems; and renewable energy.

Some of the key features of the RS-485 that make it ideal for use in I&I communications applications are:

- Long distance links—up to 4000 feet
- Bidirectional communications possible over a single pair of twisted cables
- Differential transmission increases common-mode noise immunity and decreases noise emissions
- Multiple drivers and receivers can be connected on the same bus
- Wide common-mode range (–7 V to +12 V) allows for differences in ground potential between the driver and receiver
- TIA/EIA-485-A allows for data rates of up to 10's of Mbps

TIA/EIA-485-A describes the physical layer of the RS-485 interface and is normally used with a higher-level protocol, such as Profibus, Interbus, Modbus, or BACnet. This allows for robust data transmission over relatively long distances.

In real applications, however, lightning strikes, power induction and direct contact, power source fluctuations, inductive switching, and electrostatic discharge can damage RS-485 transceivers by generating large transient voltages. Designers must ensure that equipment does not only work under ideal conditions but that it will also work in the "real world." To ensure that these designs can survive in electrically harsh environments, various government agencies and regulatory bodies have imposed EMC regulations. Compliance with these regulations gives the end user assurance that designs will operate as desired in these harsh environments.

## Electromagnetic Compatibility

An electromagnetic environment is composed of both radiated and conducted energy, so EMC has two aspects: emission and susceptibility. Thus, EMC has the ability of an electronic system to function satisfactorily in its intended electromagnetic environment without introducing intolerable electromagnetic disturbances to that environment. This article deals with increasing the protection level for EMC susceptibility of RS-485 ports against the three main EMC transients.

The International Electrotechnical Commission (IEC) is the world's leading organization that prepares and publishes international standards for all electrical, electronic, and related technologies. Since 1996, all electronic equipment sold to or within the European Community must meet EMC levels as defined in specifications IEC 61000-4-x.

The IEC 61000 specifications define the set of EMC immunity requirements that apply to electrical and electronic equipment intended for use in residential, commercial, and light industrial environments. This set of specifications includes three types of high voltage transients that electronic designers need to be concerned about for the data communication lines:

- IEC 61000-4-2 electrostatic discharge (ESD)
- IEC 61000-4-4 electrical fast transients (EFT)
- IEC 61000-4-5 surge immunity

Each of these specifications defines a test method to assess the immunity of electronic and electrical equipment against the defined phenomenon. The following sections summarize each of these tests.

## Electrostatic Discharge

ESD is the sudden transfer of electrostatic charge between bodies at different potentials caused by near contact or induced by an electric field. It has the characteristics of high current in a short time period. The primary purpose of the IEC 61000-4-2 test is to determine the immunity of systems to external ESD events outside the system during operation. IEC 61000-4-2 describes testing using two coupling methods. These are known as contact discharge and air-gap discharge. Contact discharge implies a direct contact between the discharge gun and the unit under test. During air discharge testing, the charged electrode of the discharge gun is

moved toward the unit under test until a discharge occurs as an arc across the air gap. The discharge gun does not make direct contact with the unit under test. A number of factors affect the results and repeatability of the air discharge test, including humidity, temperature, barometric pressure, distance, and rate of approach to the unit under test. This method is a better representation of an actual ESD event but is not as repeatable. Therefore, contact discharge is the preferred test method.

During testing, the data port is subjected to at least 10 positive and 10 negative single discharges with a one second interval between each pulse. Selection of the test voltage is dependent on the system end environment. The highest specified test is Level 4, which defines a contact discharge voltage of ±8 kV and an air discharge voltage of ±15 kV.

Figure 1 shows the 8 kV contact discharge current waveform as described in the specification. Some of the key waveform parameters are rise times of less than 1 ns and pulse widths of approximately 60 ns. This equates to a pulse with a total energy in the range of 10's of mJ.

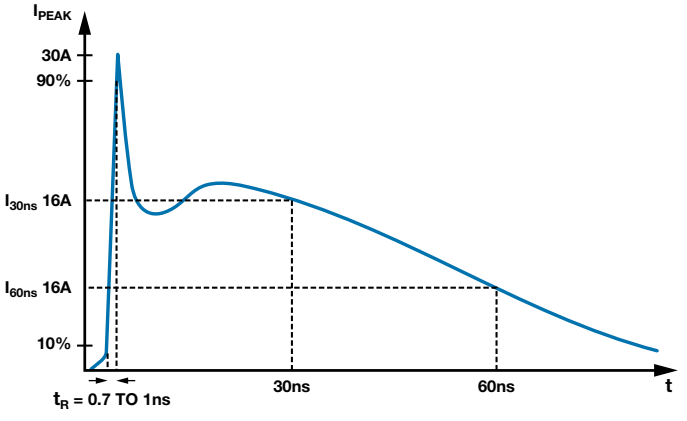


Figure 1. IEC 61000-4-2 ESD waveform (8 kV).

## Electrical Fast Transients

Electrical fast transient testing involves coupling a number of extremely fast transient impulses onto the signal lines to represent transient disturbances associated with external switching circuits that are capacitively coupled onto the communication ports, which may include relay and switch contact bounce or transients originating from the switching of inductive or capacitive loads—all of which are very common in industrial environments. The EFT test defined in IEC 61000-4-4 attempts to simulate the interference resulting from these types of events.

Figure 2 shows the EFT 50 Ω load waveform. The EFT waveform is described in terms of a voltage across 50 Ω impedance from a generator with 50 Ω output impedance. The output waveform consists of a 15 ms burst of 2.5 kHz to 5 kHz high voltage transients repeated at 300 ms intervals. Each individual pulse has a rise time of 5 ns and pulse duration of 50 ns, measured between the 50% point on the rising and falling edges of the waveform. The total energy in a single EFT pulse is similar to that in an ESD pulse. The total energy in a single pulse is typically 4 mJ. Voltages applied to the data ports can be as high as 2 kV.

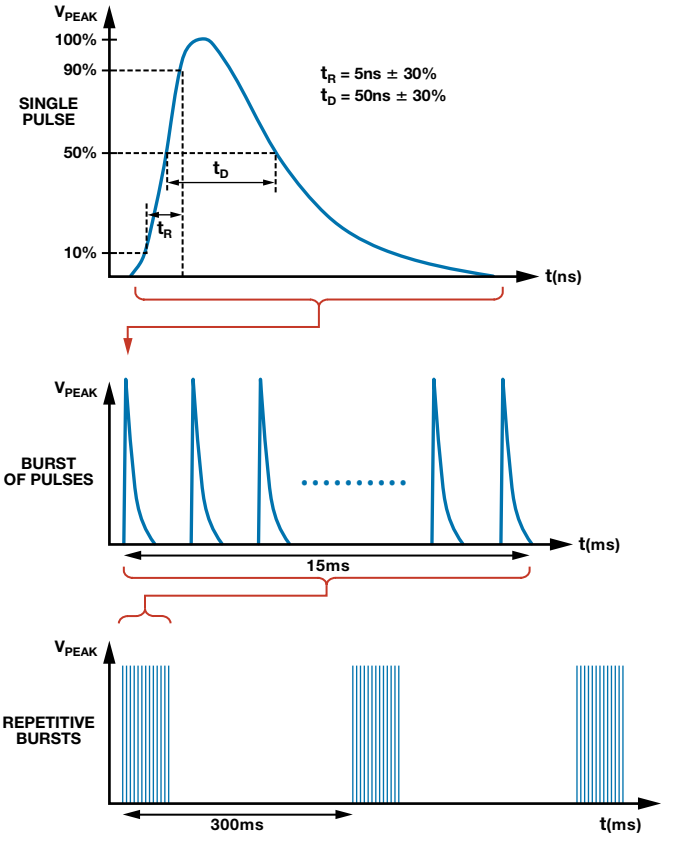


Figure 2. IEC 61000-4-4 EFT 50 Ω load waveforms.

These fast burst transients are coupled onto the communication lines using a capacitive clamp. The EFT is capacitively coupled onto the communication lines by the clamp rather than direct contact. This also reduces the loading caused by the low output impedance of the EFT generator. The coupling capacitance between the clamp and cable depends on cable diameter, shielding, and insulation on the cable.

## Surge Transients

Surge transients are caused by overvoltage from switching or lightning transients. Switching transients can result from power system switching, load changes in power distribution systems, or various system faults such as short circuits. Lightning transients can be a result of high currents and voltages injected into the circuit from nearby lightning strikes. IEC 61000-4-5 defines waveforms, test methods, and test levels for evaluating immunity against these destructive surges.

The waveforms are specified as the outputs of a waveform generator in terms of open-circuit voltage and short-circuit current. Two waveforms are described. The 10/700 µs combination waveform is used to test ports intended for connection to symmetrical communication lines; for example, telephone exchange lines. The 1.2/50 µs combination waveform generator is used in all other cases, in particular short distance signal connections. For RS-485 ports, the 1.2/50 µs waveform is predominantly used and will be discussed in this section. The waveform generator has an effective output impedance of 2 Ω; hence, the surge transient has high currents associated with it.

Figure 3 shows the 1.2/50 µs, surge transient waveform. ESD and EFT have similar rise times, pulse widths, and energy levels; however, the surge pulse has a rise time of 1.25 µs and the pulse width is 50 µs. Additionally, the surge pulse energy can reach up to almost 90 J, which is three to four orders of magnitude larger than the energy in an ESD or EFT pulse. Therefore, the surge transient is considered the most severe of the EMC transients. Due to the similarities between ESD and EFT, the design of the circuit protection can be similar, but due to its high energy, surge must be dealt with differently. This is one of the main issues in developing protection that improves the immunity of data ports to all three transients while remaining cost effective.

Resistors couple the surge transient onto the communication line. Figure 4 shows the coupling network for a half-duplex RS-485 device. The total parallel sum of the resistance is 40 Ω. For the half-duplex device, each resistor is 80 Ω.

During the surge test, five positive and five negative pulses are applied to the data ports with a maximum time interval of one minute between each pulse. The standard states that the device should be set up in normal operating conditions for the duration of the test.

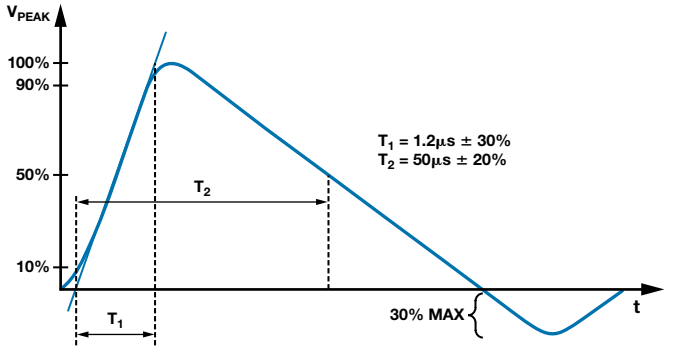


Figure 3. IEC 61000-4-5 surge 1.2/50 µs waveform.

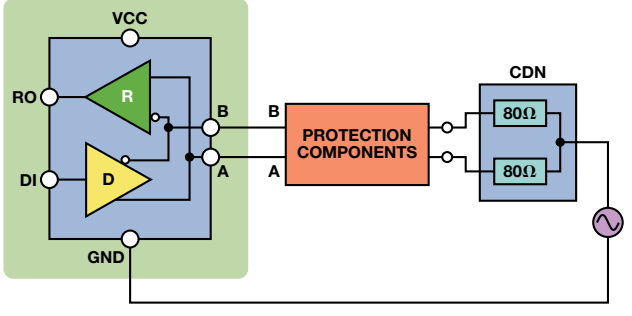


Figure 4. Coupling/decoupling network for a half-duplex RS-485 device.

## Pass/Fail Criteria

When transients are applied to the system under test, the results are categorized into four pass/fail criteria. Following is a list of the pass/fail criteria giving examples of how each one might relate to an RS-485 transceiver:

- Normal performance; no bit errors would occur during or after the transient is applied
- Temporary loss of function or temporary degradation of performance not requiring an operator; bit errors might occur during and for a limited time after the transient is applied
- Temporary loss of function or temporary degradation of performance requiring an operator; a latch-up event may occur that could be removed after a power-on reset with no permanent loss of function or degradation to the device
- Loss of function with permanent damage to equipment; the device fails the test

Criteria A is the most desirable with Criteria D being unacceptable. Permanent damage results in system down time and the expense of repair and replacement. For mission critical systems, Category B and Category C will also be unacceptable, as the system must operate without errors during transient events.

## Transient Protection

When designing circuitry to protect against transients, the designer must consider a few main items:

1. The circuitry must prevent or limit damage caused by the transient and allow the system to return to normal operation with minimal impact on performance.
2. The protection scheme should be robust enough to deal with the type of transients and voltage levels the system would be subjected to in the field.
3. The length of time associated with the transient is an important factor. For long transients, heating effects can cause certain protection schemes to fail.
4. Under normal conditions, the protection circuitry should not interfere with system operation.
5. If the protection circuitry fails during overstress, it should fail in such a way as to protect the system.

Figure 5 shows a typical protection scheme, which can be characterized as having primary and secondary protection. Primary protection, which diverts most of the transient energy away from the system, is typically located at the interface between the system and the environment. It is designed to remove the majority of the energy by diverting the transient to ground.

Secondary protection protects various parts of the system from any transient voltages and currents let through by the primary protection. It is optimized to ensure that it protects against these residual transients while allowing normal operation of these sensitive parts of the system. It is essential that both primary and secondary designs are specified to work together in conjunction with the system I/O to minimize the stress on the protected circuit. These designs typically include a coordinating element such as a resistance or a nonlinear overcurrent protection device between the primary and secondary protection devices to ensure that coordination occurs.

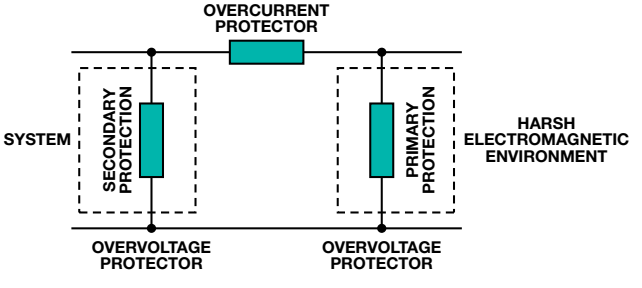


Figure 5. Protection scheme—block diagram.

### RS-485 Transient Suppression Networks

By nature, EMC transient events vary in time, so the dynamic performance and the matching of the dynamic characteristics of the protection components with the input/output stage of the protected device lead to successful EMC design. Component data sheets generally only contain dc data, which is of limited value given that the dynamic breakdowns and I/V characteristics can be quite different from the dc values. Careful design, characterization, and an understanding of the dynamic performance of the input/output stage of the protected device and the protection components are required to ensure that the circuit meets EMC standards.

The circuits shown in Figure 6 illustrate three different fully characterized EMC-compliant solutions. Each solution was certified by an independent external EMC compliance test house, and each provides different cost/protection levels for the Analog Devices ADM3485E 3.3 V RS-485 transceiver with enhanced ESD protection using a selection of Bourns external circuit protection components. The Bourns external circuit protection components used consist of transient voltage suppressors (CDSOT23-SM712), transient blocking unit (TBU-CA065-200-WH), thyristor surge protectors (TISP4240M3BJR-S), and gas discharge tubes (2038-15-SM-RPLF).

Each solution was characterized to ensure that the dynamic I/V performance of the protection components protects the dynamic I/V characteristics of the ADM3485E RS-485 bus pins such that the interaction between the input/output stage of the ADM3485E and the external protection components function together to protect against the transient events.

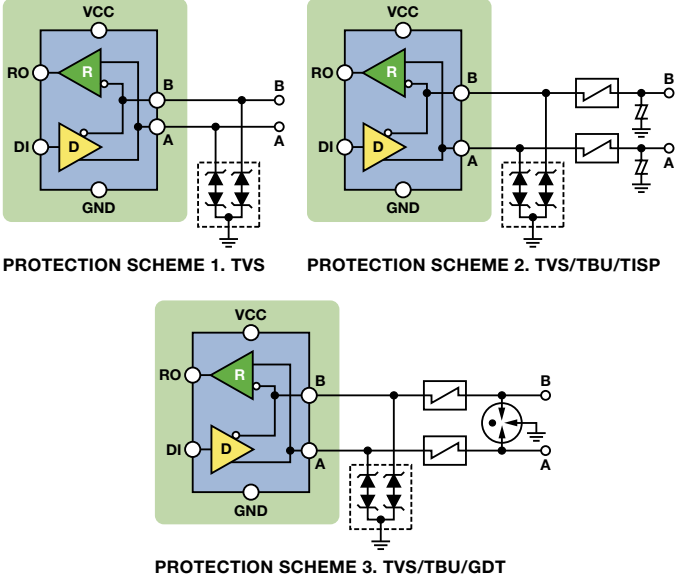


Figure 6. Three EMC-compliant ADM3485E circuits (simplified schematic, all connections not shown).

### Protection Scheme 1

As described earlier, the EFT and ESD transient have similar energy levels, while the surge waveform has energy levels three to four magnitudes greater. Protecting against ESD and EFT is accomplished in a similar manner, but protecting against high levels or surge requires more complex solutions. The first solution described here protects up to Level 4 ESD and EFT and Level 2 surge. The 1.2/50 μs waveform is used in all surge testing described in this article.

This solution uses the Bourns CDSOT23-SM712 transient voltage suppressor (TVS) array, which consists of two bidirectional TVS diodes optimized to protect RS-485 systems with minimal overstress while allowing the full range of RS-485 signal and common-mode excursions (–7 V to +12 V) on the RS-485 transceiver. Table 1 shows the voltage levels protected against for ESD, EFT, and surge transients.

**Table 1. Solution 1 Protection Levels**

| ESD (-4-2) | | EFT (-4-4) | | Surge (-4-5) | |
|---|---|---|---|---|---|
| Level | Voltage (Contact/Air) | Level | Voltage | Level | Voltage |
| 4 | 8 kV/15 kV | 4 | 2 kV | 2 | 1 kV |

A TVS is a silicon-based device. Under normal operating conditions, the TVS has high impedance to ground; ideally, it is an open circuit. The protection is accomplished by clamping the overvoltage from a transient to a voltage limit. This is done by the low impedance avalanche breakdown of a PN junction. When a transient voltage larger than the breakdown voltage of the TVS is generated, the TVS clamps the transient to a predetermined level that is less than the breakdown voltage of the devices that it is protecting. The transients are clamped instantaneously (<1 ns), and the transient current is diverted away from the protected device to ground.

It is important to ensure that the breakdown voltage of the TVS is outside the normal operating range of the pins protected. The unique feature of the CDSOT23-SM712 is that it has asymmetrical breakdown voltages of +13.3 V and –7.5 V to match the transceiver common-mode range of +12 V to –7 V, therefore providing optimum protection while minimizing overvoltage stresses on the ADM3485E RS-485 transceiver.

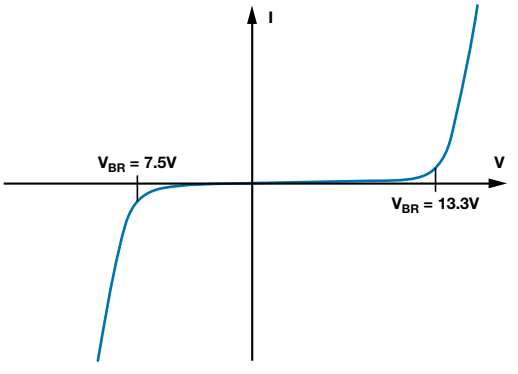


Figure 7. CDSOT23-SM712 I/V characteristic.

### Protection Scheme 2

The previous solution protects up to Level 4 ESD and EFT but only to Level 2 surge. To improve the surge protection level, the protection circuitry gets more complex. The following protection scheme will protect up to Level 4 surge.

The CDSOT23-SM712 is specifically designed for RS-485 data ports. The next two circuits build on the CDSOT23-SM712 to provide higher levels of circuit protection. The CDSOT23-SM712 provides secondary protection while the TISP4240M3BJR-S provides the primary protection. Coordination between the primary and secondary protection devices and overcurrent protection are accomplished using the TBU-CA065-200-WH. Table 2 shows the voltage levels protected against for ESD, EFT, and surge transients with this protection circuit.

**Table 2. Solution 2 Protection Levels**

| ESD (-4-2) | | EFT (-4-4) | | Surge (-4-5) | |
|---|---|---|---|---|---|
| Level | Voltage (Contact/Air) | Level | Voltage | Level | Voltage |
| 4 | 8 kV/15 kV | 4 | 2 kV | 4 | 4 kV |

When a transient is applied to the protection circuit, the TVS will break down, protecting the device by providing a low impedance path to ground. With large voltages and currents, the TVS must also be protected by limiting the current through it. This is done using a transient blocking unit (TBU), which is an active high speed overcurrent protection element. The TBU in this solution is the Bourns TBU-CA065-200-WH.

A TBU blocks current rather than shunting it to ground. As a series component, it reacts to current through the device rather than the voltage across the interface. A TBU is a high speed overcurrent protection component with a preset current limit and a high voltage withstand capability. When an overcurrent occurs and the TVS breaks down due to the transient event, the current in the TBU will rise to the current-limiting level set by the device. At this point, the TBU disconnects the protected circuitry from the surge in less than 1 µs. During the remainder of the transient, the TBU remains in the protected blocking state, with very low current (<1 mA) passing through to the protected circuit. Under normal operating conditions, the TBU exhibits low impedance, so it has minimal impact on normal circuit operation. In blocking mode, it has very high impedance to block transient energy. After the transient event, the TBU automatically resets to its low impedance state and allows resumption of normal system operation.

Like all overcurrent protection technologies, the TBU has a maximum breakdown voltage, so a primary protection device must clamp the voltage and redirect the transient energy to ground. This is commonly done using technologies such as gas discharge tubes or solid-state thyristors, such as the totally integrated surge protector (TISP). The TISP acts as a primary protection device. When its predefined protection voltage is exceeded, it provides a crowbar low impedance path to ground, hence diverting the majority of the transient energy away from the system and other protection devices.

The nonlinear voltage-current characteristic of the TISP limits overvoltage by diverting the resultant current. As a thyristor, a TISP has a discontinuous voltage-current characteristic caused by the switching action between high and low voltage regions. Figure 8 shows the voltage current characteristic of the device. Before the TISP device switches into a low voltage state, with low impedance to ground to shunt the transient energy, a clamping action is caused by the avalanche breakdown region. In limiting an overvoltage, the protected circuitry will be exposed to a high voltage for the brief time period that the TISP device is in the breakdown region before it switches into a low-voltage protected on-state. The TBU will protect the downstream circuitry from high currents resulting from this high voltage. When the diverted current falls below a critical value, the TISP device automatically resets allowing normal system operation to resume.

As described, all three components work together in conjunction with the system I/O to protect the system from high voltage and current transients.

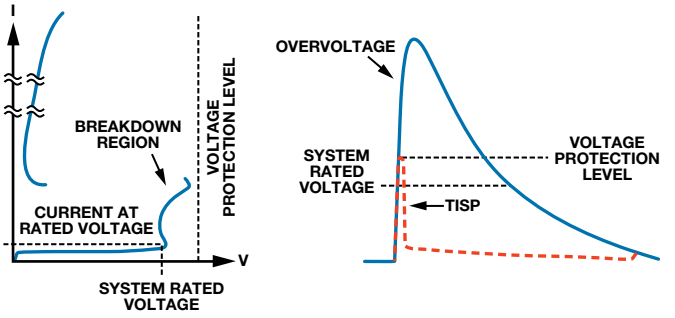


Figure 8. TISP switching characteristic and voltage limiting waveshape.

### Protection Scheme 3

Protection levels above Level 4 surge are often required. This protection scheme will protect RS-485 ports up to and including 6 kV surge transients. It operates in a similar fashion to Protection Scheme 2, but in this circuit, a gas discharge tube (GDT) is used in place of the TISP to protect the TBU, which is, in turn, protecting TVS, the secondary protection device. The GDT will provide protection to higher overvoltage and overcurrent stress than the TISP described in the previous protection scheme. The GDT for this protection scheme is the Bourns 2038-15-SM-RPLF. The TISP is rated at 220 amps versus the GDT rating of 5 kA per conductor. Table 3 shows the protection levels provided by this design.

**Table 3. Solution 3 Protection Levels**

| ESD (-4-2) | | EFT (-4-4) | | Surge (-4-5) | |
|---|---|---|---|---|---|
| Level | Voltage (Contact/Air) | Level | Voltage | Level | Voltage |
| 4 | 8 kV/15 kV | 4 | 2 kV | X | 6 kV |

Predominately used as a primary protection device, a GDT provides a low impedance path to ground to protect against overvoltage transients. When a transient voltage reaches the GDT spark-over voltage, the GDT will switch from a high impedance off-state to arc mode. In arc mode, the GDT becomes a virtual short, providing a crowbar current path to ground and diverting the transient current away from the protected device.

Figure 9 shows the typical characteristics of a GDT. When the voltage across a GDT increases, the gas in the tube starts to ionize due to the charge developed across it. This is known as the glow region. In this region, the increased current flow will create an avalanche effect that will transition the GDT into a virtual short circuit, allowing current to pass through the device. During the short circuit event, the voltage developed across the device is known as the arc voltage. The transition time between the glow and arc region is highly dependent on the physical characteristics of the device.

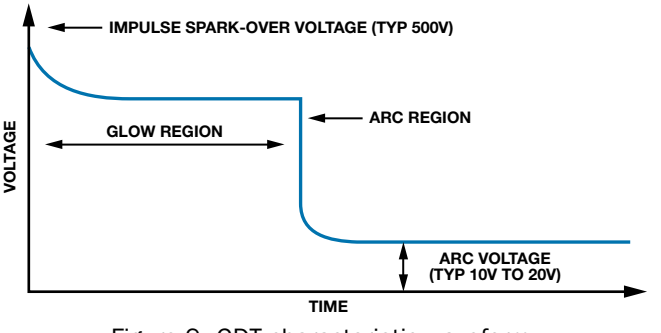


Figure 9. GDT characteristic waveform.

**Table 4. Three ADM3485E EMC-Compliant Solutions**

| | ESD (-4-2) | | EFT (-4-4) | | Surge (-4-5) | |
|---|---|---|---|---|---|---|
| Protection Scheme | Level | Voltage (Contact/Air) | Level | Voltage | Level | Voltage |
| TVS | 4 | 8 kV/15 kV | 4 | 2 kV | 2 | 1 kV |
| TVS/TBU/TISP | 4 | 8 kV/15 kV | 4 | 2 kV | 4 | 4 kV |
| TVS/TBU/GDT | 4 | 8 kV/15 kV | 4 | 2 kV | X | 6 kV |

## Conclusion

This article described the three IEC standards of interest that deal with transient immunity. In real industrial applications, RS-485 communication ports subjected to these transients can be damaged. EMC problems discovered late in a product design cycle may require expensive redesign and can often lead to schedule overruns. EMC problems should, therefore, be considered at the start of the design cycle and not at a later stage where it may be too late to achieve the desired EMC performance.

The key challenge in designing EMC-compliant solutions for RS-485 networks is matching the dynamic performance of the external protection components with the dynamic performance of the input/output structure of the RS-485 device.

This article demonstrated three different EMC-compliant solutions for RS-485 communication ports, giving the designer options depending on the level of protection required. The EVAL-CN0313-SDPZ is the industry's first EMC-compliant RS-485 customer design tool, providing up to Level 4 protection levels for ESD, EFT, and surge. The protection levels offered by the different protection schemes are summarized in Table 4. While these design tools do not replace the due diligence or qualification required at the system level, they allow the designer to reduce risk of project slippage due to EMC problems at the start of the design cycle, hence reducing design time and time to market. For more information, please visit: www.analog.com/RS485emc.

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# Programmable-Gain Transimpedance Amplifiers Maximize Dynamic Range in Spectroscopy Systems

By Luis Orozco

### Introduction

Precision instrumentation systems that measure physical properties using a photodiode or other current-output sensor often include a transimpedance amplifier (TIA) and a programmable-gain stage to maximize dynamic range. This article uses a real-world example to show the benefits and challenges of implementing a single-stage programmable-gain TIA to minimize noise while maintaining high bandwidth and high accuracy.

Transimpedance amplifiers are essential building blocks in any system that measures light. Many chemical analysis instruments, such as ultraviolet-visible (UV-VIS) or Fourier transform-infrared (FT-IR) spectroscopes, rely on photodiodes to accurately identify chemical compounds. These systems must measure a wide range of light intensity. For example, a UV-VIS spectroscope can measure opaque samples, such as used motor oil, or transparent substances, such as ethanol. In addition, some substances have strong absorption bands at certain wavelengths, while remaining almost transparent at other wavelengths. Instrument designers often add several programmable gains to the signal path to increase the dynamic range.

### Photodiodes and Photodiode Amplifiers

Before discussing photodiode amplifiers, let's start with a quick refresher on photodiodes, which are devices that generate voltage or current when light hits their PN junction. Figure 1 shows the equivalent circuit. For a typical device used in spectroscopy, the model includes a light-dependent current source in parallel with a large shunt resistor and a shunt capacitor that can range from less than 50 pF for small devices to more than 5000 pF for very large devices.

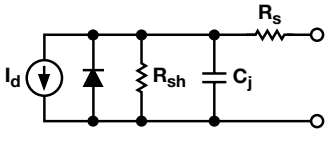


Figure 1. Photodiode model.

Figure 2 shows the transfer function for a typical photodiode. The curve looks very similar to that of a normal diode, but the entire curve moves up and down as the photodiode is exposed to light. Figure 2b shows a close-up of the transfer function around the origin, where no light is present. The output of the photodiode is nonzero as long as the bias voltage is nonzero. This *dark current* is typically specified with a 10-mV reverse bias. Although operating the photodiode with a large reverse bias (photoconductive mode) results in a faster response, operating with zero bias (photovoltaic mode) eliminates the dark current. In practice, the dark current does not disappear completely, even in photovoltaic mode, as the amplifier's input offset voltage will result in a small error across the photodiode's terminals.

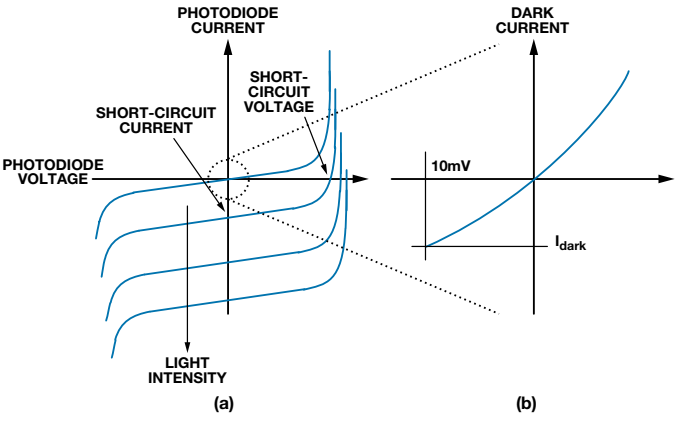


Figure 2. Typical photodiode transfer function.

When operating a photodiode in photovoltaic mode, a transimpedance amplifier (TIA) keeps the bias voltage near 0 V while converting the photodiode current to a voltage. Figure 3 shows the most basic form of a TIA.

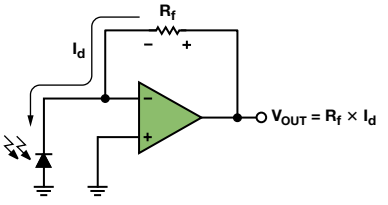


Figure 3. Transimpedance amplifier.

### DC Error Sources

With an ideal op amp, the inverting input of the amplifier will be at virtual ground, and all of the photodiode current will flow through the feedback resistor, $R_f$. With one end of $R_f$ at virtual ground, the output voltage is simply $R_f \times I_d$. In order for this approximation to hold true, the op amp's input bias current and input offset voltage must be small. In addition, a small input offset voltage will minimize the photodiode's dark current. A good amplifier choice is the AD8615, which specifies 1-pA maximum leakage and 100-μV maximum offset at room temperature. In this example, we choose $R_f$ = 1 MΩ to provide the desired output level with the maximum light input.

Unfortunately, designing a photodiode amplifier is not as simple as selecting an op amp for the circuit shown in Figure 3. If we simply connect $R_f$ = 1 MΩ across the feedback path of the op amp, the photodiode's shunt capacitance will cause the op amp to oscillate. To illustrate this, Table 1 shows $C_s$ and $R_{sh}$ for a typical large-area photodiode. Table 2 shows key specifications for the AD8615, whose low input bias current, offset voltage, noise, and capacitance make it a great fit for precision photodiode amplifier applications.

**Table 1. Photodiode Specifications**

| Parameter | Symbol | Value |
|---|---|---|
| Shunt Capacitance | $C_s$ | 150 pF |
| Shunt Resistance | $R_{sh}$ | 600 MΩ |

**Table 2. AD8615 Specifications**

| Parameter | Symbol | Value |
|---|---|---|
| Input Capacitance, Differential | $C_{diff}$ | 2.5 pF |
| Input Capacitance, Common-Mode | $C_{cm}$ | 6.7 pF |
| Total Input Capacitance (for TIA) | $C_i = C_{diff} + C_{cm}$ | 9.2 pF |
| Gain-Bandwidth Product | GBP | 24 MHz |
| Voltage Noise Density | $e_n$ | 7 nV/√Hz at 10 kHz |
| Current Noise Density | $I_n$ | 50 fA/√Hz at 1 kHz |

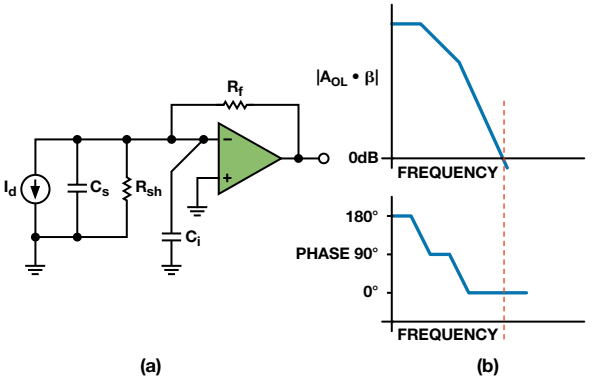


Figure 4. Photodiode amplifier model (a) and open-loop response (b).

### Selecting External Components for Guaranteed Stability

Figure 4a is a good model for the photodiode amplifier. The system's open-loop transfer function has one pole at 28 Hz due to the op amp's open-loop response (from the data sheet) and another pole due to the feedback resistor and the photodiode's parasitic resistance and capacitance. For our selected component values, this pole occurs at 1 kHz, as shown in Equation 1.

$$f_{p2} = \frac{R_f + R_{sh}}{2\pi(C_{sh} + C_i)R_f R_{sh}} = 1 \text{ kHz} \quad (1)$$

Note that $R_{sh}$ is two orders of magnitude larger than $R_f$, so Equation 1 simplifies to

$$f_{p2} \approx \frac{1}{2\pi(C_{sh} + C_i)R_f} = 1 \text{ kHz} \quad (1a)$$

Each pole causes a 90° phase shift in the open-loop transfer function, for a 180° total phase shift well below the frequency where the open-loop amplitude response crosses 0 dB. As shown in Figure 4b, the lack of phase margin makes it almost certain that the circuit will oscillate.

To ensure stable operation, we can add a zero to the transfer function by placing a capacitor in parallel with $R_f$. This zero reduces the slope of the transfer function from 40-dB/decade to 20-dB/decade when crossing 0 dB, and results in positive phase margin. The design should have at least 45° of phase margin to guarantee stability. Higher phase margins trade response time for less ringing. The zero added by the capacitor to the open-loop response becomes a pole in the closed-loop response, so the amplifier's closed-loop response will decrease as the capacitor is increased. Equation 2 shows how to calculate the feedback capacitor for a 45° phase margin.

$$C_f = \sqrt{\frac{C_{sh} + C_i}{2\pi R_f f_u}} \quad (2)$$

where $f_u$ is the op amp's unity-gain frequency.

This value for $C_f$ determines the highest practical bandwidth at which the system can operate. Although it's possible to select a smaller capacitor for lower phase margin and higher bandwidth, the output could ring excessively. Also, all components have tolerances that must be accounted for to guarantee stability under worst-case conditions. For our example, we select $C_f$ = 4.7 pF, resulting in a closed-loop bandwidth of 34 kHz, as is typical of many spectroscopy systems.

Figure 5 shows the open-loop frequency response after adding the feedback capacitor. The phase response dips below 30°, but this occurs several decades away from where the gain goes to 0 dB, so the amplifier will remain stable.

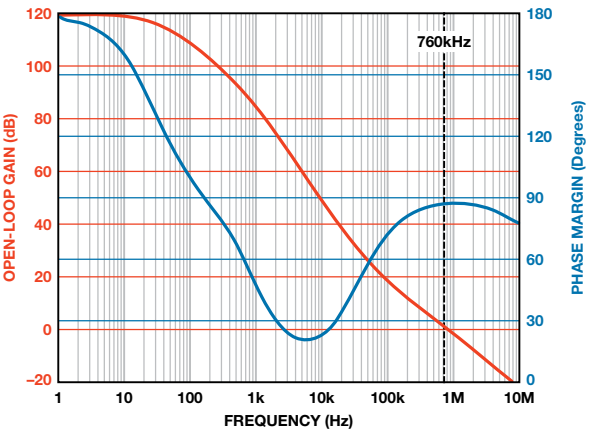


Figure 5. Photodiode amplifier open-loop response with 1.2-pF feedback capacitor.

### Programmable-Gain TIA

One way to make a photodiode amplifier with programmable gain is to use a transimpedance amplifier with a gain that keeps the output in the linear region even for the brightest light inputs. A programmable-gain amplifier stage can then boost the TIA's output under low-light conditions, achieving near unity gain for high-intensity signals, as shown in Figure 6a. A second option is to implement the programmable gain directly in the TIA, eliminating the second stage as shown in Figure 6b.

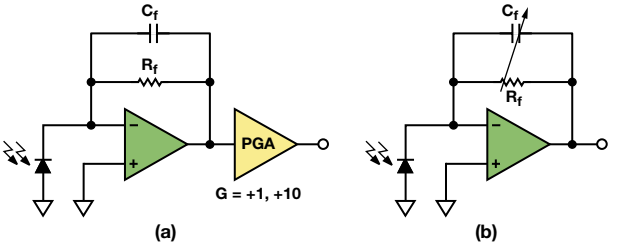


Figure 6. (a) TIA first stage followed by a PGA (b) Programmable-gain TIA

### Calculating TIA Noise

The three main sources of noise in a transimpedance amplifier are the op amp's input voltage noise, its input current noise, and the feedback resistor's Johnson noise. All of these noise sources are typically expressed as noise density. To convert to units of volts rms, take the noise power (square of the voltage noise density) and integrate over frequency. An accurate and much simpler method is to multiply the noise density times the square root of the equivalent noise bandwidth (ENBW). We can model the amplifier's closed-loop bandwidth as a first-order response dominated by the feedback resistor, $R_f$, and the compensation capacitor, $C_f$. Using the specifications from the stability example, the resulting closed-loop bandwidth is

$$f_{3dB} = \frac{1}{2\pi R_f C_f} = \frac{1}{2\pi \times 1\ \text{M}\Omega \times 4.7\ \text{pF}} = 34 \text{ kHz} \quad (3)$$

To convert the 3-dB bandwidth to ENBW in a single-pole system, multiply by π/2:

$$\text{ENBW} = f_{3dB} \times \frac{\pi}{2} = 53 \text{ kHz} \quad (4)$$

Now that we have the ENBW, we can find the rms noise due to the feedback resistor and the op amp's current noise. The resistor's Johnson noise will appear at the output directly, and the op amp's current noise will appear as an output voltage after going through the feedback resistor.

$$\text{Noise}_{Rf} = \sqrt{4kT \times ENBW \times R_f} = \sqrt{4 \times 1.38 \times 10^{-23}\,\frac{m^2 kg}{s^2 K} \times 298K \times \left(34\ kHz \times \frac{\pi}{2}\right) \times 1\ M\Omega} = 30\ \mu V\ rms \quad (5)$$

$$\text{Noise}_{current} = 50\,\frac{fA}{\sqrt{Hz}} \times R_f \times \sqrt{ENBW} = 50\,\frac{fA}{\sqrt{Hz}} \times 1\ M\Omega \times \sqrt{34\ kHz \times \frac{\pi}{2}} = 12\ \mu V\ rms \quad (6)$$

where k is Boltzmann's constant, and T is the temperature in kelvin.

The final contributor is the op amp's voltage noise. The output noise is the input noise multiplied by the noise gain. The best way to think about the noise gain for a transimpedance amplifier is to start with the inverting amplifier shown in Figure 7.

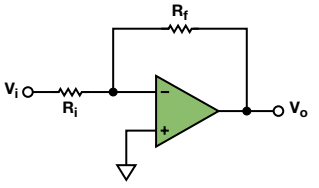


Figure 7. Inverting amplifier noise gain.

For this circuit, the noise gain is

$$\text{Noise gain} = 1 + \frac{R_f}{R_i} \quad (7a)$$

Using the photodiode amplifier model from Figure 4a, the noise gain will be:

$$\text{Noise gain} = 1 + \frac{Z_f}{Z_i} \quad (7b)$$

where $Z_f$ is the parallel combination of the feedback resistor and capacitor, and $Z_{in}$ is the parallel combination of the op amp's input capacitance with the photodiode's shunt capacitance and shunt resistance.

This transfer function contains several poles and zeros, and hand analysis would be tedious. However, using the values from the previous examples, we can make some rough approximations. At frequencies near dc, the resistors will dominate, and the gain will be near 0 dB, as the diode's shunt resistance is two orders of magnitude larger than the feedback resistance. As the frequency increases, the impedance of the capacitors will decrease and start to dominate the gain. Since the total capacitance from the inverting pin of the op amp to ground is much larger than the feedback capacitor, $C_f$, the gain will start to increase with frequency. Fortunately, the increase in gain does not go on indefinitely, since the pole formed by the feedback capacitor and resistor will stop the increase in gain, and eventually the op amp's bandwidth will take over to start rolling off the gain.

Figure 8 shows the amplifier's noise gain behavior over frequency and the location of each pole and zero in the transfer function.

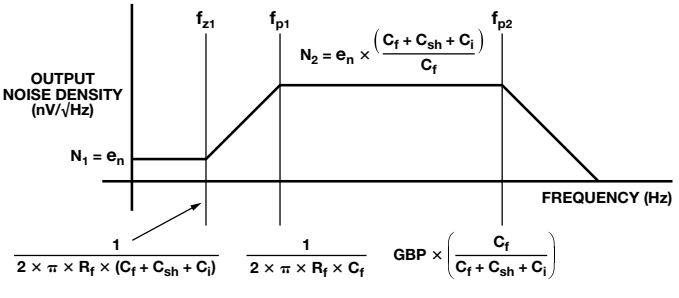


Figure 8. Amplifier noise gain transfer function.

Just as with the resistor noise density, the most accurate way to convert the output noise density of Figure 8 to voltage noise in V rms is to square the noise density, integrate over the entire frequency spectrum, and then calculate the square root. However, inspection of the response shows that a much easier approach introduces only a small error. For most systems, the first zero and pole occur at relatively low frequencies compared to the second pole. For example, using the specifications from Table 1 and Table 2, the circuit has the following poles and zeros:

$$f_{z1} = \frac{1}{2\pi \times 1\ M\Omega \times (4.7\ pF + 150\ pF + 9.2\ pF)} = 971\ Hz \quad (8)$$

$$f_{p1} = \frac{1}{2\pi \times 1\ M\Omega \times (4.7 pF)} = 34\ kHz \quad (9)$$

$$f_{p2} = 24\ MHz \times \left(\frac{4.7\ pF}{4.7\ pF + 150\ pF + 9.2\ pF}\right) = 688\ kHz \quad (10)$$

The noise will peak at

$$N_2 = 7\,\frac{nV}{\sqrt{Hz}} \times \left(\frac{4.7\ pF + 150\ pF + 9.2\ pF}{4.7\ pF}\right) = 244\,\frac{nV}{\sqrt{Hz}} \quad (11)$$

Note that $f_{z1}$ and $f_{p1}$ occur at a relatively low frequency compared to $f_{p2}$. Simply assuming that the output noise is equal to the plateau noise ($N_2$ from Equation 11) all the way from dc to $f_{p2}$ greatly simplifies the math required to calculate the output noise.

With this assumption in mind, the output noise is equal to the input noise density multiplied by the plateau gain and by the ENBW, which is $f_{p2} \times \pi/2$:

$$\text{Op amp noise} \approx \frac{7nV}{\sqrt{Hz}} \times \frac{4.7pF + 159.2\ pF}{4.7pF} \times \sqrt{\frac{\pi}{2} \times 24\ MHz \times \frac{4.7\ pF}{4.7\ pF + 159.2\ pF}} = 254\ \mu V\ rms \quad (12)$$

Now that we have the output referred noise from all three sources, we can combine them to get the overall system output noise. The three noise sources are independent and Gaussian, so we can root-sum-square (RSS) them rather than adding them. When combining terms using RSS, one term will dominate the result if it is more than about three times larger than the others.

$$\text{Total noise} = \sqrt{30\ \mu V^2 + 12\ \mu V^2 + 254\ \mu V^2} = 256\ \mu V\ rms \quad (13)$$

The response of Figure 8 makes it obvious that the noise bandwidth of the op amp is much larger than its signal bandwidth. The additional bandwidth does nothing but contribute to the noise, so we can add a low-pass filter on the output to attenuate the noise at frequencies outside the signal bandwidth. Adding a single-pole RC filter with 34-kHz bandwidth reduces the voltage noise from 254 μV rms to 45 μV rms, and the total noise from 256 μV rms to only 52 μV rms.

### Noise Contributed by Programmable-Gain Stage

If we add a PGA after the transimpedance amplifier, the noise at the output will be the PGA's noise, plus the TIA's noise times the additional gain. For example, if we assume an application that requires gains of 1 and 10, and use a PGA with a total input noise density of 10 nV/√Hz, then the output noise due to the PGA will be either 10 nV/√Hz or 100 nV/√Hz.

To calculate the total noise of the system, we can again root-sum-square the TIA's noise contribution and the PGA's noise contribution as shown in Table 3. For this example, assume that the PGA includes a 34-kHz filter. As we can see, for a gain of 10, the TIA's noise contribution will appear at the PGA's output multiplied by the PGA gain.

**Table 3. Total System Noise for TIA + PGA Architecture**

| | Noise at PGA Input | Output Noise G = 1 | Output Noise G = 10 |
|---|---|---|---|
| **TIA with RC Filter** | 52 µV rms | 52 µV rms | 520 µV rms |
| **PGA with 34-kHz BW** | 2.3 µV rms | 2.3 µV rms | 23.1 µV rms |
| **RSS Noise Total** | | 52 µV rms | 524 µV rms |

As we would expect, the output noise is slightly more than 10 times as large when operating with a gain of 10 than when the PGA is set for a gain of one.

### Noise Advantage of a Single Gain Stage

An alternative approach is to use a transimpedance amplifier with programmable gain, skipping the PGA stage altogether. Figure 9 shows a theoretical circuit with two programmable transimpedance gains of 1 MΩ and 10 MΩ. Each transimpedance resistor needs its own capacitor to compensate for the photodiode's input capacitance. To be consistent with the previous example, we will keep the signal bandwidth at 34 kHz for both gain settings. This means selecting a 0.47-pF capacitor in parallel with the 10-MΩ resistor. In this case, the output voltage noise, when operating with the 1-MΩ resistor, is the same as in Equation 12. When operating with a transimpedance gain of 10 MΩ, the larger resistor results in higher Johnson noise, higher current noise (the current noise is now multiplied by 10 MΩ instead of 1 MΩ), and higher noise gain. Following the same methodology, the three main noise contributors are

$$\text{Noise}_{Rf} = \sqrt{4 \times 1.38 \times 10^{-23} \frac{m^2 kg}{s^2 K} \times 298K \times 34\ kHz \times \frac{\pi}{2} \times 10\ M\Omega} \quad (14)$$

$$= 94\ \mu V\ rms$$

$$\text{Noise}_{current} = 50 \frac{fA}{\sqrt{Hz}} \times 10\ M\Omega \times \sqrt{34\ kHz \times \frac{\pi}{2}} = 115\ \mu V\ rms \quad (15)$$

$$f_{p2} = 24\ MHz \left( \frac{0.47\ pF}{0.47\ pF + 150\ pF + 9.2\ pF} \right) = 71\ kHz \quad (16)$$

$$N_2 = 7 \frac{nV}{\sqrt{Hz}} \left( \frac{0.47\ pF + 150\ pF + 9.2\ pF}{0.47\ pF} \right) = 2378 \frac{nV}{\sqrt{Hz}} \quad (17)$$

$$\text{Op amp noise} = N_2 \sqrt{\frac{\pi}{2} \times 71\ kHz} = 792\ \mu V\ rms \quad (18)$$

and the total output noise is

$$\text{Total noise} = \sqrt{94\ \mu V^2 + 115\ \mu V^2 + 792\ \mu V^2} = 806\ \mu V\ rms \quad (19)$$

Adding a single-pole RC filter with a bandwidth of 34 kHz at the output results in lower noise, for a total system noise of 460 µV rms.

Due to the higher gain, $f_{p2}$ is much closer to the signal bandwidth, so the noise reduction is not as dramatic as when operating with a gain of 1 MΩ.

Table 4 shows a summary of the noise performance for both amplifier architectures. For a transimpedance gain of 10 MΩ, the total noise will be about 12% lower than with the two-stage circuit.

**Table 4. Total System Noise Comparison**

| | Output Noise, Programmable TIA | Output Noise, TIA Followed by PGA |
|---|---|---|
| **Gain = 1** | 52 µV rms | 52 µV rms |
| **Gain = 10** | 460 µV rms | 524 µV rms |

### Programmable-Gain Transimpedance Amplifier

Figure 9 shows a programmable-gain transimpedance amplifier. It's a good concept, but the on resistance and leakage current of the analog switches will introduce errors. The on resistance causes voltage and temperature dependent gain errors and the leakage current causes offset errors, especially at high temperatures.

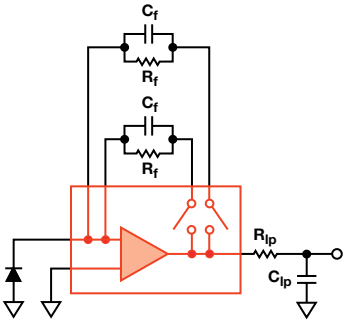


Figure 9. Programmable transimpedance amplifier.

The circuit in Figure 10 avoids these problems by using two switches in every transimpedance leg. Although this requires twice as many switches, the on resistance of the switches on the left is within the feedback loop, so the output voltage depends only on the current through the selected resistor. The switches on the right look like an output impedance and will contribute negligible error if the amplifier drives a high-impedance load, such as an ADC driver.

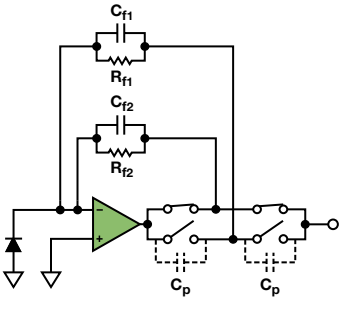


Figure 10. Programmable-gain transimpedance amplifier with Kelvin switching.

The circuit of Figure 10 will work for dc and low frequencies, but the parasitic capacitance across the switches in the off state presents yet another challenge. These parasitic capacitors, labeled $C_p$ in Figure 10, connect the unused feedback path to the output, so they will decrease the overall bandwidth. Figure 11 shows how these capacitors end up connecting to the unselected gain leg, effectively changing the transimpedance gain to be a combination of the selected gain in parallel with an attenuated version of the unselected gain.

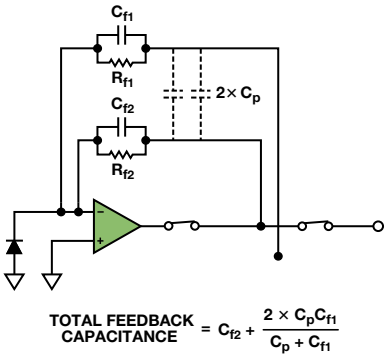


Figure 11. Total feedback capacitance including switch parasitics.

Depending on the desired bandwidth and feedback resistor, the parasitic capacitance could result in a significant difference between the expected and measured behavior of the amplifier. For example, assume the amplifier of Figure 11 uses the same 1 MΩ and 10 MΩ values as in our previous circuit, with their respective capacitors of 4.7 pF and 0.47 pF, and we select the 10 MΩ gain. If each switch has approximately 0.5 pF of feed-through capacitance, Figure 12 shows the difference between the ideal and actual bandwidths, taking into account the parasitic path.

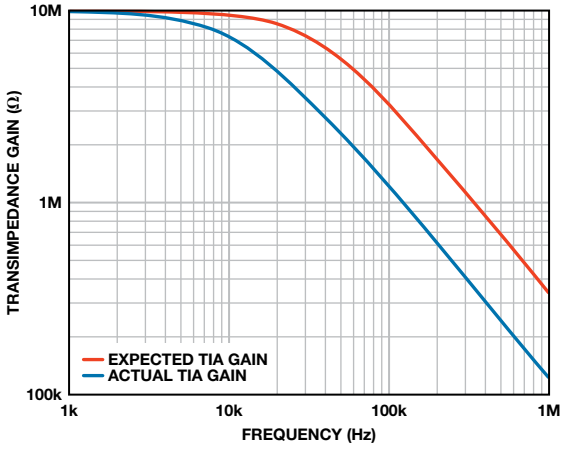


Figure 12. Transimpedance gain with parasitic switch capacitance.

One way to address this problem is to replace each switch with two switches in series. This reduces the parasitic capacitance by half at the expense of additional components. Figure 13 shows this approach.

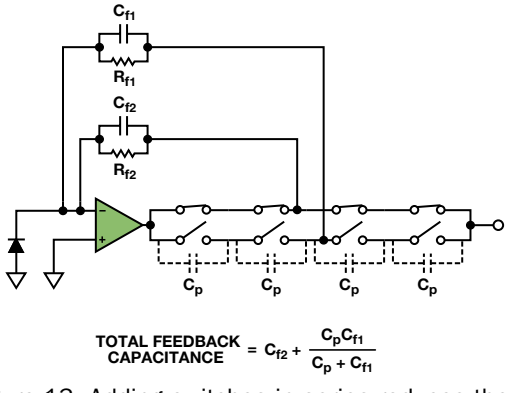


Figure 13. Adding switches in series reduces the total parasitic capacitance.

If the application requires even more bandwidth, a third alternative is to use SPDT switches to connect every unused input to ground. Although the parasitic capacitance from each open switch is still in the circuit, Figure 14b shows how each parasitic capacitor appears to be connected from the output of the op amp to ground or from the end of the unused feedback leg to ground. Capacitance from the amplifier output to ground tends to be associated with instability and ringing, but in this case, the total parasitic capacitance of just a few picofarads will not have a significant effect on the output. The parasitic capacitance that appears from the inverting input to ground will add to the photodiode's shunt capacitance and the op amp's own input capacitance and will represent a negligible increase when compared with the photodiode's large shunt capacitance. Assuming 0.5 pF of feedthrough capacitance for each switch, the op amp would see an additional 2-pF load on its output, which most op amps will drive with no problems.

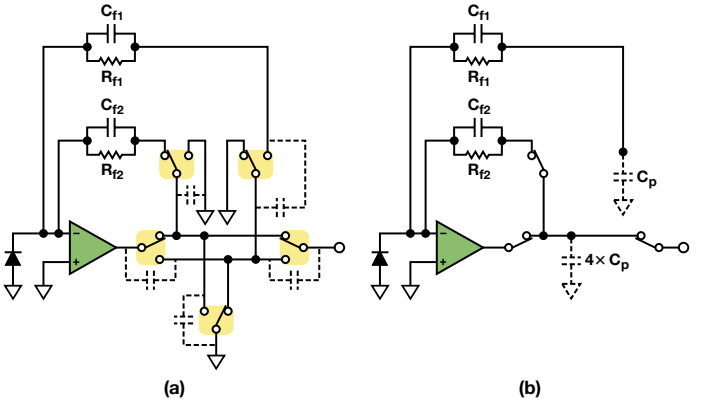


Figure 14. Programmable TIA with SPDT switches.

As with everything, however, the approach of Figure 14 has trade-offs. It's more complex and can be difficult to implement for more than two gains. In addition, the two switches in the feedback loop will introduce dc errors and distortion. Depending on the value of the feedback resistor, the additional bandwidth may be important enough to warrant these small errors. For example, with a 1-MΩ feedback resistor, the on resistance of an ADG633 will contribute about 50 ppm gain error and 5 μV offset error at room temperature. If the application calls for maximum bandwidth, however, this may be a reasonable trade-off.

## Conclusion

Photodiode amplifiers are an essential part of most chemical analysis and material identification signal chains. Having programmable gain allows engineers to design instruments that accurately measure very large dynamic ranges. This article shows how to ensure stability while achieving high bandwidth and low noise. Designing a programmable-gain TIA involves challenges with switch configuration, parasitic capacitance, leakage current, and distortion, but selecting a suitable configuration and making the right trade-offs can lead to excellent performance.

## Author

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# Choose Resistors to Minimize Errors in Grounded-Load Current Source

By David Guo

Operational amplifiers are frequently used to make high-quality current sources in a variety of applications, such as industrial process control, scientific instrumentation, and medical equipment. Single Amplifier Current Sources, published in *Analog Dialogue*, Volume 1, Number 1, 1967, introduces several current source circuits that provide a constant current through floating loads or grounded loads. In industrial applications, such as pressure transmitters and gas detectors, these circuits are widely used to provide 4-mA to 20-mA or 0-mA to 20-mA currents.

The improved Howland current source, shown in Figure 1, is very popular because it can drive a grounded load. The transistor, which allows relatively high currents, can be replaced by a MOSFET to achieve even higher currents. For low cost, low current applications, the transistor can be eliminated, as shown in Difference Amplifier Forms Heart of Precision Current Source, published in *Analog Dialogue*, Volume 43, Number 3, 2009.

The accuracy of this current source is determined by the amplifier and the resistors. This article shows how to choose the external resistors to minimize errors.

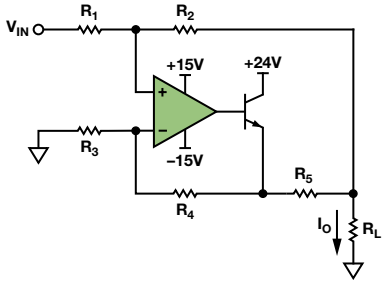


Figure 1. Improved Howland current source drives grounded loads.

Analysis of the improved Howland current source yields the transfer function:

$$I_O = V_{IN} \times \frac{R_2R_3 + R_2R_4 + R_5R_3}{R_3(R_2 + R_5)R_L - R_1R_4R_L + R_1R_3R_5 + R_2R_3R_5} \quad (1)$$

### Tip 1: Set $R_2 + R_5 = R_4$

In Equation 1, the load resistance influences the output current, but if we set $R_1 = R_3$ and $R_2 + R_5 = R_4$, the formula reduces to:

$$I_O = V_{IN} \times \frac{R_4}{R_3R_5} \quad (2)$$

Here, the output current is only a function of $R_3$, $R_4$, and $R_5$. With an ideal amplifier, the resistor tolerances determine the accuracy of output current.

### Tip 2: Set $R_L = n \times R_5$

To decrease the total number of resistors in the component library, set $R_1 = R_2 = R_3 = R_4$. Now, Equation 1 simplifies to:

$$I_O = V_{IN} \times \frac{R_5 + 2R_2}{R_5(R_L + 2R_2)} \quad (3)$$

If $R_5 = R_L$, it further simplifies to:

$$I_O = V_{IN} \times \frac{1}{R_5} \quad (4)$$

Here, the output current depends only on the resistance of $R_5$.

In some cases, the input signal may need to be attenuated. For example, with a 10-V input signal and $R_5 = 100\ \Omega$, the output current would be 100 mA. To get a 20-mA output current, set $R_1 = R_3 = 5R_2 = 5R_4$. Now, Equation 1 reduces to:

$$I_O = V_{IN} \times \frac{5R_5 + 6R_2}{5R_5(R_L + 6R_2)}$$

If $R_L = 5R_5 = 500\ \Omega$, then:

$$I_O = V_{IN} \times \frac{1}{5R_5} \quad (5)$$

### Tip 3: Larger value for $R_1/R_2/R_3/R_4$ improves the current accuracy

In most cases, $R_1 = R_2 = R_3 = R_4$, but $R_L \neq R_5$, so the output current is as shown in Equation 3. With $R_5 = 100\ \Omega$ and $R_L = 500\ \Omega$, for example, Figure 2 shows the relationship between the resistance of $R_1$ and the current accuracy. To achieve 0.5% current accuracy, $R_1$ must be at least 40 kΩ.

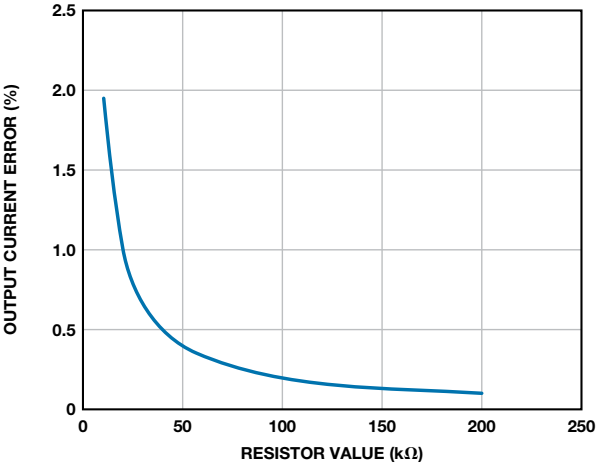


Figure 2. Relationship between R1 and output current accuracy.

### Tip 4: Resistor tolerance affects current accuracy

Real-world resistors are never ideal, with each having a specified tolerance. Figure 3 shows an example circuit, where $R_1 = R_2 = R_3 = R_4 = 100$ kΩ, $R_5 = 100\ \Omega$, and $R_L = 500\ \Omega$. With the input voltage set to 0.1 V, the output current should be 1 mA. Table 1 shows the output current error caused by different resistor tolerances. To obtain 0.5% current accuracy, choose 0.01% tolerance for $R_1/R_2/R_3/R_4$, 0.1% for $R_5$, and 5% for $R_L$. Resistors with 0.01% tolerance are expensive, so a better choice would be to use an integrated difference amplifier, such as the AD8276, which has better resistor matching and is more cost effective.

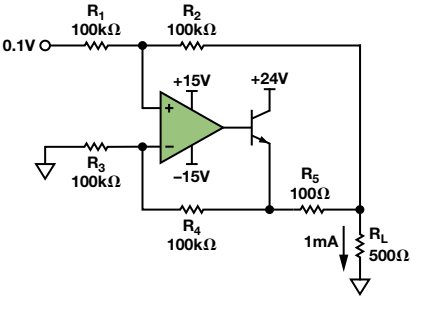


Figure 3. Example circuit for $I_{OUT}$ = 1 mA.

*(continued on Page 20)*

# Voltage Reference Design for Precision Successive-Approximation ADCs

By Alan Walsh

The overall precision of a high-resolution, successive-approximation ADC depends on the accuracy, stability, and drive capability of its voltage reference. The switched capacitors on the ADC's reference input present a dynamic load, so the reference circuit must be able to handle time- and throughput-dependent currents. Some ADCs integrate the reference and reference buffer on chip, but these may not be optimal in terms of power or performance—and the best performance can usually be achieved with an external reference circuit. This article looks at the challenges and requirements involved with the reference circuit design.

### Reference Input

A simplified schematic of a successive-approximation ADC is shown in Figure 1. During the sampling interval, the capacitive DAC is connected to the ADC input, and a charge proportional to the input voltage is stored on its capacitors. When the conversion starts, the DAC is disconnected from the input. The conversion algorithm successively switches each bit to the reference or ground. Charge redistribution on the capacitors causes current to be drawn from or sunk by the reference. This dynamic current load is a function of both the ADC throughput rate and the internal clock that controls the bit trials. The most significant bits (MSBs) hold the most charge and require the most current.

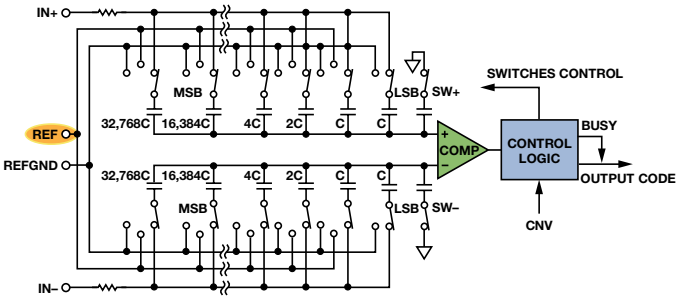


Figure 1. Simplified schematic of a 16-bit successive-approximation ADC.

Figure 2 shows the dynamic current load on the reference input of the AD7980, 16-bit, 1-MSPS, PulSAR® successive-approximation ADC. The measurement was made by observing the voltage drop across a 500-Ω resistor placed between the reference source and the reference pin. The plot shows current spikes of up to 2.5 mA, along with smaller spikes spread over the conversion.

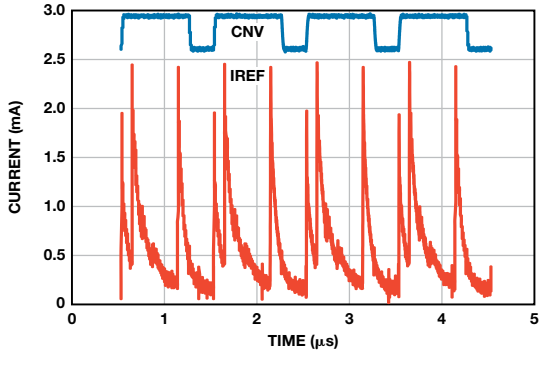


Figure 2. AD7980 dynamic reference current.

To supply this current, while keeping the reference voltage free of noise, place a high value, low ESR reservoir capacitor, typically 10 µF or more, as close as possible to the reference input. A larger capacitor will further smooth the current load and reduce the burden on the reference circuit, but stability becomes an issue with very large capacitors. The reference must be capable of supplying the average current needed to top up the reference capacitor without causing the reference voltage to droop significantly. In ADC data sheets, the average reference input current is typically specified at a particular throughput rate. For example, the AD7980 data sheet specifies the average reference current to be 330 µA typical at 1 MSPS with a 5-V reference. No current is drawn between conversions, so the reference current scales linearly with throughput, dropping to 33 µA at 100 kSPS. The reference—or reference buffer—must have low enough output impedance at the highest frequency of interest to maintain the voltage at the ADC input without a significant current-induced voltage drop.

### Reference Output Drive

Figure 3 shows a typical reference circuit. The voltage reference may integrate a buffer that has sufficient drive current, or a suitable op amp can be used as a buffer. To avoid conversion errors, the average current required at a particular throughput should not cause the reference voltage to droop more than ½ LSB. This error will be most pronounced during a burst conversion, as the reference load will go from zero to the average reference current at that throughput.

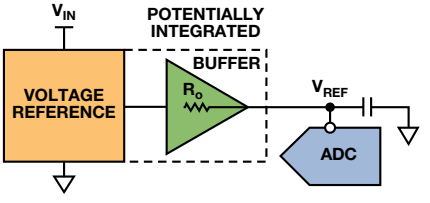


Figure 3. Typical precision successive-approximation ADC reference circuit.

Using the AD7980 16-bit ADC with $I_{REF}$ = 330 µA and $V_{REF}$ = 5 V as an example to determine whether a reference has sufficient drive capability, the maximum allowed output impedance for a ½ LSB voltage drop is

$$R_{o\_max} = \frac{V_{half\_lsb}}{I_{REF}} = \frac{\frac{5\ V}{2^{16+1}}}{330\ \mu A} = 0.115\ \Omega$$

Most voltage references don't specify output impedance, but they do specify load regulation, usually in ppm/mA. To convert to output impedance, multiply by the reference voltage and divide by 1000. For example, the ADR435 ultralow-noise XFET® 5-V reference specifies load regulation of 15 ppm/mA maximum when sourcing current. Converting to ohms gives

$$R_o = \frac{5\ V \times 15\ ppm/mA}{1000} = 0.075\ \Omega$$

So, the ADR435 should be suitable from an output impedance perspective. It can source up to 10 mA, which is more than enough to handle the 330-µA average reference current. When the ADC input voltage exceeds the reference voltage, even momentarily, it can inject current into the reference, so the reference must also be

able to sink some current. Figure 4 shows the diode connection between the ADC and reference inputs that can cause current flow into the reference during an input overrange condition. Unlike some older references, the ADR435 can sink 10 mA.

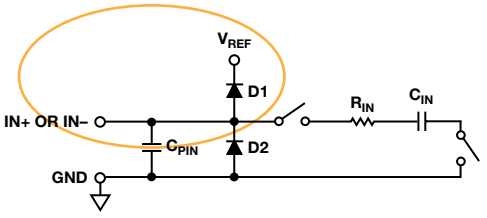


Figure 4. AD7980 analog input structure.

As the reference current requirement scales linearly with throughput, a higher output impedance (lower power) reference may be acceptable at lower throughput rates, or when using ADCs with lower throughput, such as the 500 kSPS AD7988-5 or 100 kSPS AD7988-1 ($I_{REF}$ = 250 µA). The maximum output impedance can be calculated with the reduced reference current. Note that these equations should only be used as guidelines, and the selected reference should be tested for drive capability in hardware.

A reference buffer can be used when the drive of the chosen reference is insufficient, or when a micropower reference is preferred. This can be implemented with a suitable op amp in a unity-gain configuration. The op amp must have low noise and suitable output drive capability, and it must be stable with a large capacitive load. It must also be able to supply the necessary current. Op amp output impedance is not generally specified but can often be determined from output impedance vs. frequency plots, as shown in Figure 5 for the AD8031 80-MHz rail-to-rail op amp.

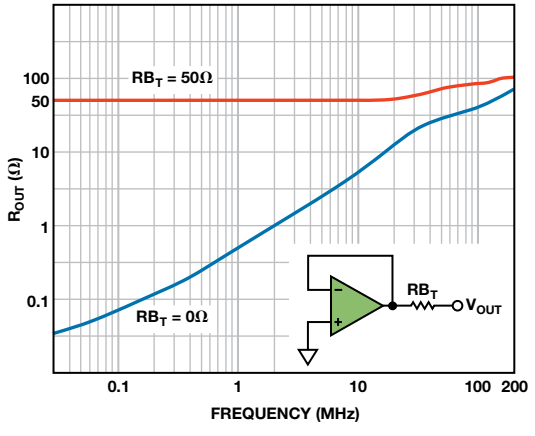


Figure 5. AD8031 $R_{OUT}$ vs. frequency.

The output impedance is less than 0.1 Ω below 100 kHz and less than 0.05 Ω at dc, so this is a good choice in terms of output drive for our example of driving the AD7980 at 1 MSPS. Maintaining low output impedance over a wide frequency range is important for driving the reference input. The reservoir capacitor will never completely smooth out the current draw at the reference input, even with a large capacitor. The frequency content of the current ripple will be a function of the throughput and the input signal bandwidth. The large reservoir capacitor handles the high-frequency throughput-dependent current while the reference buffer must be able to maintain low impedance up to the maximum input signal frequency—or to a frequency where the reservoir capacitor impedance becomes low enough to supply the necessary current. Typical plots in reference data sheets show output impedance vs. frequency and should be taken into consideration when choosing the reference.

The AD8031 is a good choice, as it is stable with capacitive loads greater than 10 µF. Other op amps, such as the ADA4841, will also be stable with large capacitors, as they mainly have to drive a stable dc level, but particular op amps must be tested to determine their behavior when loaded. It is not a good idea to use a series resistor before the capacitor to maintain stability, as this will increase the output impedance.

A reference buffer is very useful for driving multiple ADCs from one reference, as is the case in simultaneous-sampling applications, such as that shown in Figure 6.

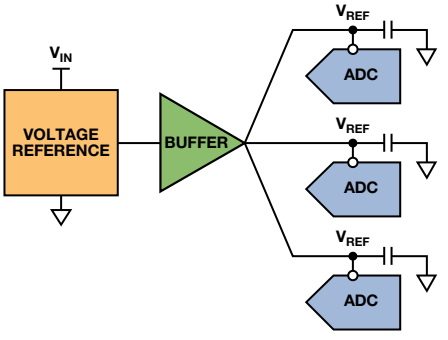


Figure 6. Reference circuit driving multiple ADCs.

Each ADC reference input has its own reservoir capacitor placed as close as possible to the reference input pin. The trace from each reference input is routed back to a star connection at the output of the reference buffer to minimize crosstalk effects. Reference buffers that have low output impedance and high output current capability can drive many ADCs, depending on their current requirements. Note that the buffer must also be stable with the extra capacitance associated with multiple reference capacitors.

### Noise and Temperature Drift

Once the drive capability has been determined, we must ensure that the noise from the reference circuit does not affect the ADC's performance. To preserve the signal-to-noise ratio (SNR) and other specifications, we must keep the noise contribution from the reference to a fraction (ideally 20% or less) of the ADC noise. The AD7980 specifies 91-dB SNR with a 5-V reference. Converting to rms gives

$$\frac{5\text{V}}{2\sqrt{2}} \times 10^{\frac{-91\text{dB}}{20}} = 50\,\mu\text{V rms}$$

Thus, the reference circuit should have less than 10 µV rms noise to have minimal impact on the SNR. The noise specification for references and op amps is typically split into two parts: low-frequency (1/f) noise and wideband noise. Combining the two will give the total noise contribution of the reference circuit. Figure 7 shows a typical noise vs. frequency plot for the ADR431 2.5-V reference.

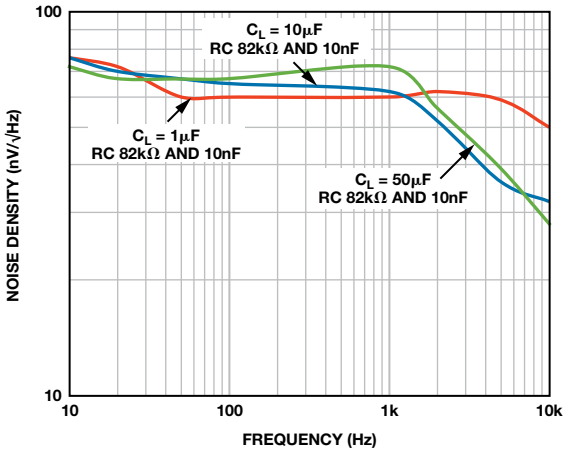


Figure 7. ADR431 noise with compensation network.

The ADR435 compensates its internal op amp to drive large capacitive loads and avoid noise peaking, making it very attractive for use with ADCs. This is explained in greater detail in the data sheet. With a 10 µF capacitor, it specifies 8 µV p-p 1/f (0.1 Hz to 10 Hz) noise and 115 nV/√Hz wideband noise spectral density. The estimated noise bandwidth is 3 kHz. To convert the 1/f noise from peak-to-peak to rms, divide by 6.6 to get

$$\frac{8\,\mu\text{Vp-p}}{6.6} = 1.2\,\mu\text{V rms}$$

Next, calculate the wideband noise contribution using the estimated bandwidth with a 10 µF capacitor. The effective bandwidth will be given by

$$\frac{\pi}{2} \times 3\,\text{kHz} = 4.7\,\text{kHz}$$

Use this effective bandwidth to calculate the rms wideband noise

$$115\,\text{nV}/\sqrt{\text{Hz}} \times \sqrt{4.7\,\text{kHz}} = 7.9\,\mu\text{V rms}$$

The total rms noise is the root sum square of the low-frequency noise and the wideband noise

$$\sqrt{(1.2\,\mu\text{V rms})^2 + (7.9\,\mu\text{V rms})^2} = 8\,\mu\text{V rms}$$

This is less than 10 µV rms, so it won't significantly impact the ADC's SNR. These calculations can be used to estimate the noise contribution of the reference to determine its suitability, but this will need to be verified on the bench with real hardware.

The same analysis can be used to calculate the noise contribution if a buffer is used after the reference. The AD8031, for example, has 15 nV/√Hz noise spectral density. With a 10-µF capacitor on its output, its measured bandwidth is reduced to about 16 kHz. Using this bandwidth and noise density, and ignoring the 1/f noise, the noise contribution will be 2.4 µV rms. The reference buffer noise can be root sum squared with the reference noise to arrive at a total noise estimate. Generally the reference buffer should have a noise density much less than that of the reference.

When using a reference buffer, it is possible to band limit the noise from the reference even further by adding an RC filter with a very low cutoff frequency to the output of the reference, as shown in Figure 8. This can be useful, considering the reference is usually the dominant source of noise.

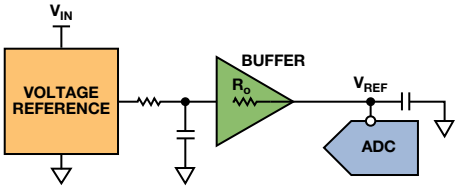


Figure 8. Voltage reference with RC filtering.

Some other important considerations for choosing a reference are initial accuracy and temperature drift. The initial accuracy is specified in percent or mV. Many systems allow for calibration, so initial accuracy is not as important as drift, which is typically specified in ppm/°C or µV/°C. Most good references have less than 10 ppm/°C drift, and the ADR45xx family drives drift down to a couple of ppm/°C. This drift must be incorporated into the system's error budget.

### Troubleshooting Reference Issues

A poorly designed reference circuit can cause serious conversion errors. The most common manifestation of a reference issue is repeated or "stuck" codes from the ADC. This happens when noise on the reference input is large enough to cause the ADC to make an incorrect bit decision. This may show up as the same code being repeated many times, even though the input is changing, or a repeated string of ones or zeros in the less significant bits, as shown in Figure 9. The areas circled in red show where the ADC gets stuck, repeatedly returning the same code. The problem generally gets worse near full scale because the reference noise has a greater impact on the more significant bit decisions. Once an incorrect bit decision has been made, the remaining bits become filled with ones or zeros.

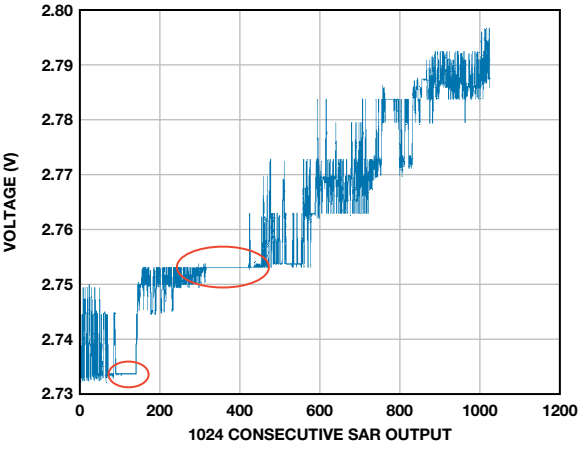


Figure 9. "Stuck" codes in ADC transfer function.

The most common reasons for these "stuck" bits are the size and placement of the reference capacitor, insufficient drive strength of the reference/reference buffer, or poor selection of the reference/reference buffer, resulting in excess noise.

It is critical to place the reservoir capacitor close to the ADC's reference input pin, using wide traces to connect it, as shown in Figure 10. The capacitor should have a low impedance path to ground using multiple vias to the ground plane. If the reference has a dedicated ground, the capacitor should be connected close to that pin using wide traces. Because the capacitor acts as a charge reservoir, it needs to be large enough to limit droop and must have low ESR. Ceramic capacitors with X5R dielectric are a good choice. Typical values are in the 10 µF to 47 µF range, but smaller values can sometimes be tolerated depending on the current requirements of the ADC.

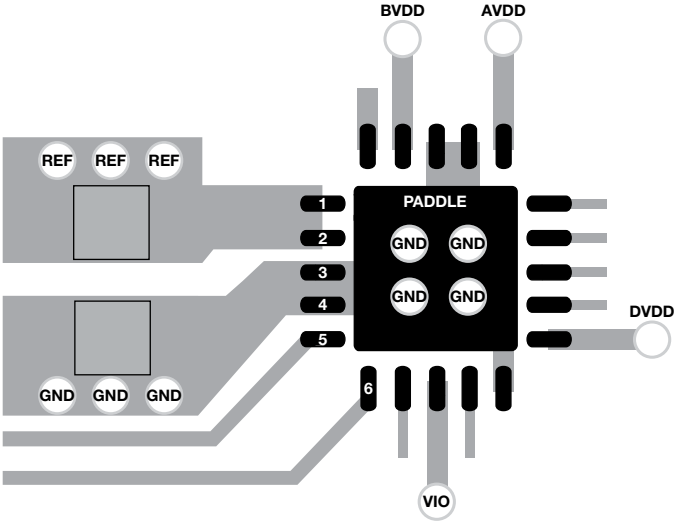


Figure 10. Typical reference capacitor layout.

Insufficient drive strength is another issue, especially if low-power references or micropower reference buffers are used, as these typically have much higher output impedances that increase dramatically with frequency. This is particularly true when using higher throughput ADCs, as the current requirement is higher than at lower throughputs.

Excessive noise from either the reference or reference buffer, relative to the LSB size of the converter, can also result in stuck codes, so the voltage noise of the reference circuit must remain a small fraction of the LSB voltage.

## Conclusion

This article showed how to design a reference circuit for precision successive-approximation ADCs and highlighted how to identify some of their common problems. The calculations presented are a means to estimate the reference circuit drive strength and noise requirements so that a greater probability of success can be realized when testing the circuit in hardware.

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## Author


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*(continued from Page 16)*

**Table 1. Worst-Case Output Current Error (%) vs. Resistor Tolerance (%)**

| Resistor Tolerance/ Resistors Varied | 5 | 1 | 0.5 | 0.1 | 0.05 | 0.01 | 0 |
|---|---|---|---|---|---|---|---|
| $R_1/R_2/R_3/R_4$ | 110.11 | 10.98 | 5.07 | 1.18 | 0.69 | 0.30 | 0.20 |
| $R_5$ | 5.05 | 1.19 | 0.70 | 0.30 | 0.25 | 0.21 | 0.20 |
| $R_L$ | 0.21 | 0.20 | 0.20 | 0.20 | 0.20 | 0.20 | 0.20 |

## Conclusion

When designing an improved Howland current source, choose external resistors to make the output current independent of the load resistance. Resistor tolerance influences the accuracy, and a trade-off between accuracy and cost must be made. The amplifier's offset voltage and offset current will also affect the accuracy. Consult the data sheet to check if the amplifier can meet the circuit requirements. Multisim can be used to simulate how these specifications influence the accuracy. An integrated difference amplifier—with its low offset voltage, offset voltage drift, gain error, and gain drift—can cost effectively implement accurate, stable current sources.

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# Complete Sensor-to-Bits Solution Simplifies Industrial Data-Acquisition System Design

By Maithil Pachchigar

### Introduction

At the heart of many industrial automation and process-control systems, programmable logic controllers (PLCs) monitor and control complex system variables. Employing multiple sensors and actuators, PLC-based systems measure and control analog process variables such as pressure, temperature, and flow. PLCs are found in diverse applications—such as factories, oil refineries, medical equipment, and aerospace systems—that require high accuracy and robust, long-term operation. In addition, the competitive marketplace demands lower cost and shorter design times.

Thus, designers of industrial equipment and critical infrastructure encounter significant challenges in meeting their customers' stringent accuracy, noise, drift, speed, and safety requirements. Using a PLC as an example, this article shows how the versatile, low cost, highly integrated ADAS3022 reduces complexity, solving many challenges encountered in the design of multichannel data-acquisition systems by replacing the analog front-end (AFE) stages. Ideally suited for precision industrial, instrumentation, power-line, and medical data-acquisition cards with multiple input ranges, this high-performance device reduces cost and time to market while offering a small, easy-to-use footprint and true 16-bit precision at 1 MSPS.

### PLC Application Example

Figure 1 shows a simplified signal chain for a PLC used in industrial automation and process-control systems. The PLC typically comprises analog and digital input/output (I/O) modules, a central processing unit (CPU), and power-management circuitry.

In industrial applications, analog input modules acquire and monitor signals from remote sensors located in harsh environments characterized by extreme temperature and humidity, vibration, and explosive chemicals. Typical signals include single-ended or differential voltages with 5 V, 10 V, ±5 V, and ±10 V full-scale ranges, or current loops with 0 mA to 20 mA, 4 mA to 20 mA, and ±20 mA ranges. When long cables with substantial electromagnetic interference (EMI) are encountered, current loops are often used due to their inherently high noise immunity.

Analog output modules typically control actuators, such as relays, solenoids, and valves, to complete the automated-control system. They typically provide output voltages with 5 V, 10 V, ±5 V, and ±10 V full-scale ranges and 4 mA to 20 mA current-loop outputs.

Typical analog I/O modules include 2, 4, 8, or 16 channels. To meet stringent industry standards, these modules require protection against overvoltage, overcurrent, and EMI surges. Most PLCs include digital isolation between the ADC and the CPU and between the CPU and the DAC. High-end PLCs may also incorporate channel-to-channel isolation, as specified by the International Electrotechnical Commission (IEC) standards. Many I/O modules include per-channel software-programmable single-ended or differential input ranges, bandwidth, and throughput rate.

In modern PLCs, the CPU performs numerous control tasks in an automated manner, employing real-time access to information to make intelligent decisions. The CPU may embody advanced software and algorithms, and Web connectivity for diagnostic error checking and fault detection. Commonly used communication interfaces include RS-232, RS-485, industrial Ethernet, SPI, and UART.

### Discrete Implementation of Data-Acquisition System

Industrial designers can build analog modules for PLCs or similar data-acquisition systems with discrete high-performance components, as shown in Figure 2. Key design considerations include input signal configuration and overall system speed, accuracy, and precision. The signal chain presented here utilizes the ADG1208/ADG1209 low-leakage multiplexer, AD8251 fast-settling programmable-gain instrumentation amplifier (PGIA), AD8475 high-speed funnel amplifier, AD7982 differential-input 18-bit PulSAR® ADC, and ADR4550 ultralow-noise voltage reference. This solution provides four different gain ranges, but with maximum input signals of ±10 V, designers will have to worry about the multiplexer's switching and settling times, as well as other analog signal conditioning challenges. In addition, achieving true 16-bit performance at 1 MSPS can be a major challenge, even when using these high-performance components.

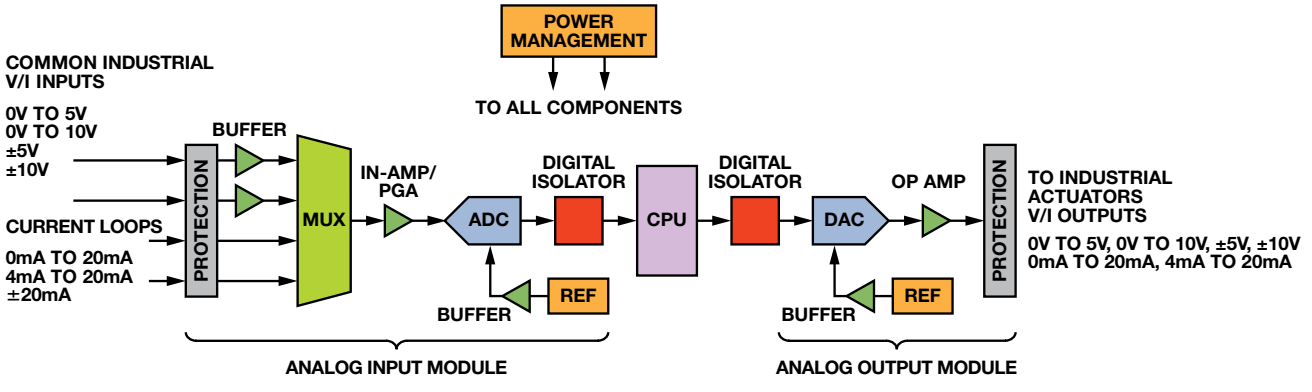


Figure 1. Typical PLC signal chain.

The AD7982 specifies a 290-ns transient response from a full-scale step. Thus, to guarantee the specified performance while converting at 1 MSPS, the PGIA and funnel amp must settle in less than 710 ns. The AD8251 specifies 785-ns settling time to 16 bits (0.001%) for a 10-V step, however, so the maximum throughput that can be guaranteed for this signal chain will be less than 1 MSPS.

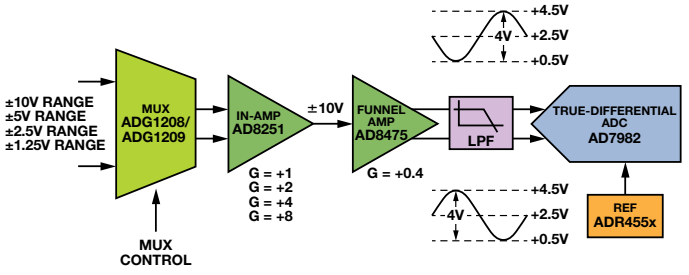


Figure 2. Analog input signal chain using discrete components.

**Integrated Solution Simplifies Data-Acquisition System Design**

Manufactured in *i*CMOS®, a proprietary, high-voltage industrial process technology, the 16-bit, 1-MSPS ADAS3022 data-acquisition IC integrates an 8-channel, low-leakage multiplexer; a high-impedance PGIA with high common-mode rejection; a precision, low-drift 4.096-V reference and buffer; and a 16-bit successive-approximation ADC, as shown in Figure 3.

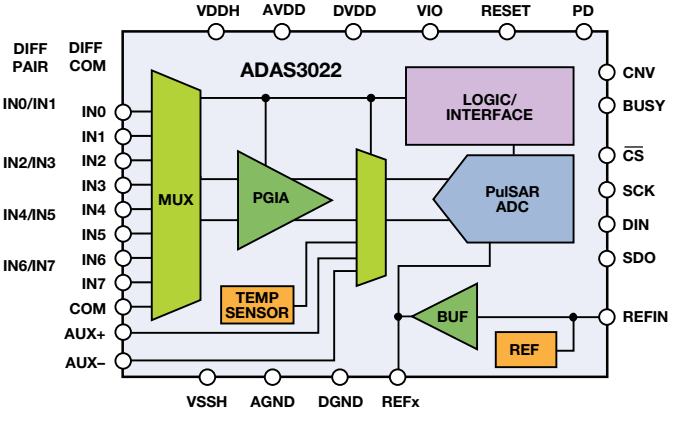


Figure 3. Functional block diagram of ADAS3022.

This complete sensor-to-bits solution utilizes only one-third of the board space of discrete implementations, helping engineers to simplify their designs while reducing the size, time to market, and cost of advanced industrial data-acquisition systems. Eliminating the necessity to buffer, level shift, amplify, attenuate, or otherwise condition the input signal, and the concerns regarding common-mode rejection, noise, and settling time, it alleviates many of the challenges associated with designing a precision 16-bit, 1-MSPS data-acquisition system. It delivers the best-in-class 16-bit accuracy (±0.6-LSB typical INL), low offset voltage, low drift overtemperature, and optimized noise performance at 1 MSPS (91-dB typical SNR), as shown in Figure 4. The device is specified over the –40°C to +85°C industrial temperature range.

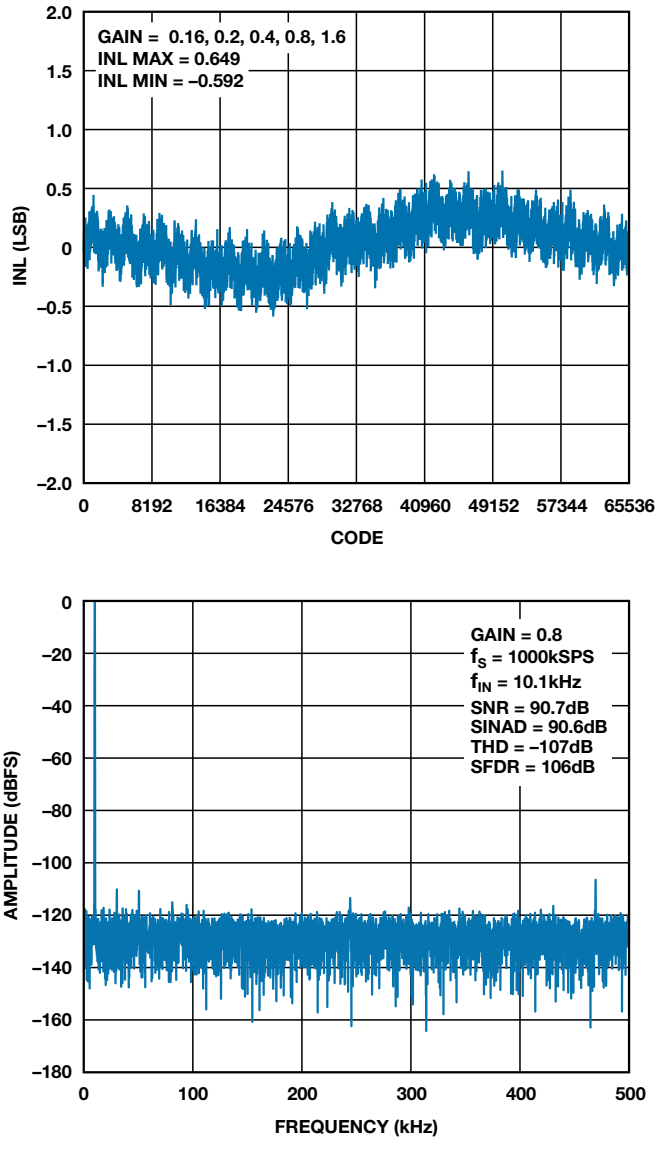


Figure 4. INL and FFT performance of the ADAS3022.

The PGIA has a large common-mode input range, true high-impedance inputs (>500 MΩ), and a wide dynamic range, allowing it to accommodate 4-mA to 20-mA current loops, accurately measure small sensor signals, and reject interference from ac power lines, electric motors, and other sources (90-dB minimum CMR).

An auxiliary differential input channel can accommodate ±4.096V input signals. It bypasses the multiplexer and PGIA stages, allowing direct interface to the 16-bit SAR ADC. An on-chip temperature sensor can monitor the local temperature.

This high level of integration saves board space and lowers the overall parts' cost, making the ADAS3022 ideal for space-constrained applications, such as automatic test equipment, power-line monitoring, industrial automation, process control, patient monitoring, and other industrial and instrumentation systems that operate with ±10-V industrial signal levels.

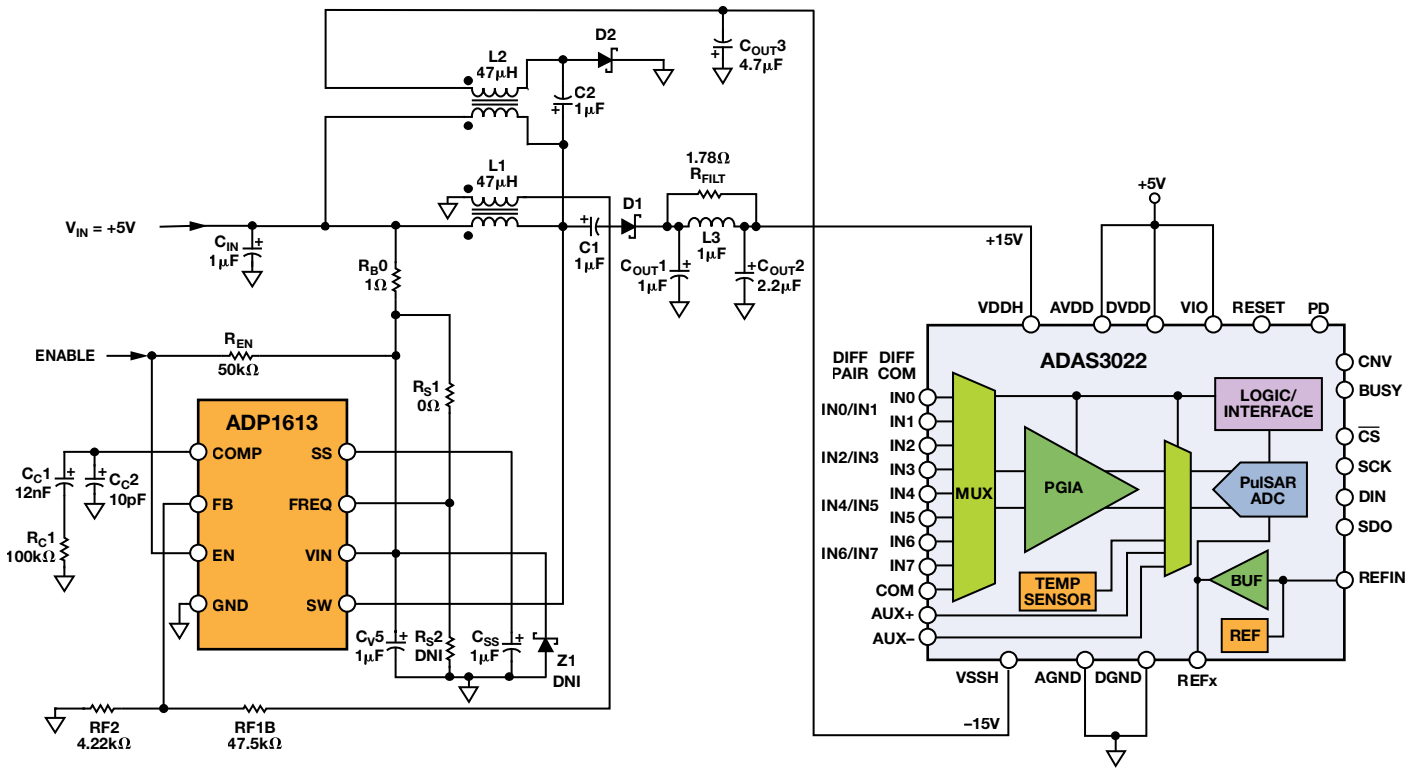


Figure 5. Complete 5-V, single-supply, 8-channel data-acquisition solution with integrated PGA.

Figure 5 shows a complete 8-channel data-acquisition system (DAS). The ADAS3022 operates with ±15-V and +5-V analog and digital supplies, and a 1.8-V to 5-V logic I/O supply. The ADP1613 high-efficiency, low-ripple dc-to-dc boost converter allows the DAS to operate with a single 5-V supply. Configured as a single-ended, primary inductance Ćuk (SEPIC) topology using the ADIsimPower™ design tool, the ADP1613 furnishes the ±15-V bipolar supplies required for the multiplexer and PGIA without compromising performance.

The noise performance of the ADAS3022 and the discrete signal chain are compared in Table 1, which uses the input signal amplitude, gain, equivalent noise bandwidth (ENBW), and input-referred (RTI) noise of each component to calculate the total noise of the complete signal chain.

**Table 1. Noise Performance for the ADAS3022 and the Discrete Signal Chain**

| | ADG1209 | AD8251 | AD8475 | AD7982 | | Total Noise | | ADAS3022 | Input Signal |
|---|---|---|---|---|---|---|---|---|---|
| Noise | RTI | RTI | RTI | RTI | SNR | $RTI_{Total}$ | SNR | SNR | |
| | (µV rms) | (µV rms) | (µV rms) | (µV rms) | (dB) | (µV rms) | (dB) | (dB) | (V rms) |
| Gain = 1 (±10 V) | 6.56 | 124 | 77.5 | 148 | 95.5 | 208 | 90.6 | 91.5 | 7.07 |
| Gain = 2 (±5 V) | 6.56 | 83.7 | 38.8 | 74.2 | 95.5 | 119 | 89.5 | 91.0 | 3.54 |
| Gain = 4 (±2.5 V) | 6.56 | 68.2 | 19.4 | 37.1 | 95.5 | 80.3 | 86.8 | 89.7 | 1.77 |
| Gain = 8 (±1.25 V) | 6.56 | 55.8 | 9.69 | 18.5 | 95.5 | 60.0 | 83.4 | 86.8 | 0.88 |

The single-pole low-pass filter (LPF) between the AD8475 and AD7982 (Figure 2) attenuates the kick coming from the switched-capacitor input of the AD7982 and limits the amount of high-frequency noise. The –3-dB bandwidth ($f_{-3dB}$) of the LPF is 6.1 MHz (R = 20 Ω, C = 1.3 nF), allowing fast settling of the input signals while converting at 1 MSPS. The ENBW of the LPF can be calculated as

$$ENBW = \pi/2 \times f_{-3dB} = 9.6 \text{ MHz}.$$

Note that this calculation ignores the noise from the voltage reference and LPF as it does not significantly affect the total noise, which is dominated by the PGIA.

Consider an example using the ±5-V input range. In this case, the AD8251 is set for a gain of 2. The funnel amplifier is set to a fixed gain of 0.4 for all four input ranges, so a 0.5-V to 4.5-V differential signal (4 V p-p) will be applied to the AD7982. The RTI noise of the ADG1208 is derived from the Johnson/Nyquist noise equation ($e_n^2 = 4K_BTR_{ON}$, where $K_B = 1.38 \times 10^{-23}$ J/K, T = 300K, and $R_{ON}$ = 270 Ω). The RTI noise of the AD8251 is derived from its 27-nV/√Hz noise density as specified in the data sheet for a gain of 2. Similarly, the RTI noise of the AD8475 is derived from its 10-nV/√Hz noise density using a gain of 0.8 (2 × 0.4). In each calculation, ENBW = 9.6 MHz. The RTI noise of the AD7982 is calculated from its 95.5-dB SNR as specified in the data sheet using a gain of 0.8. The total RTI noise of the entire signal chain is calculated based on the root-sum-square (rss) of the RTI noise from the discrete components. The total SNR of 89.5 dB can be computed from the equation $SNR = 20 \log(V_{IN} \text{ rms}/RTI_{Total})$.

Although the theoretical noise estimate (SNR) and the overall performance of the discrete signal chain is comparable to that of the ADAS3022, especially at lower gains (G = 1 and G = 2) and lower throughput rates (much less than 1 MSPS), it's not an ideal solution. The ADAS3022 can reduce cost by about 50% and board space by about 67%, as compared to the discrete solution, and it can also accept three additional input ranges (±0.64 V, ±20.48 V, and ±24.576 V) that the discrete solution cannot offer.

## Conclusion

The next generation of industrial PLC modules will demand high accuracy, reliable operation, and functional flexibility, all in a small, low-cost form factor. The ADAS3022, with industry-leading integration and performance, supports a wide range of voltage and current inputs to handle a variety of sensors in industrial automation and process control. An ideal fit for PLC analog input modules and other data-acquisition cards, the ADAS3022 will enable industrial manufacturers to differentiate their systems while meeting stringent user requirements.

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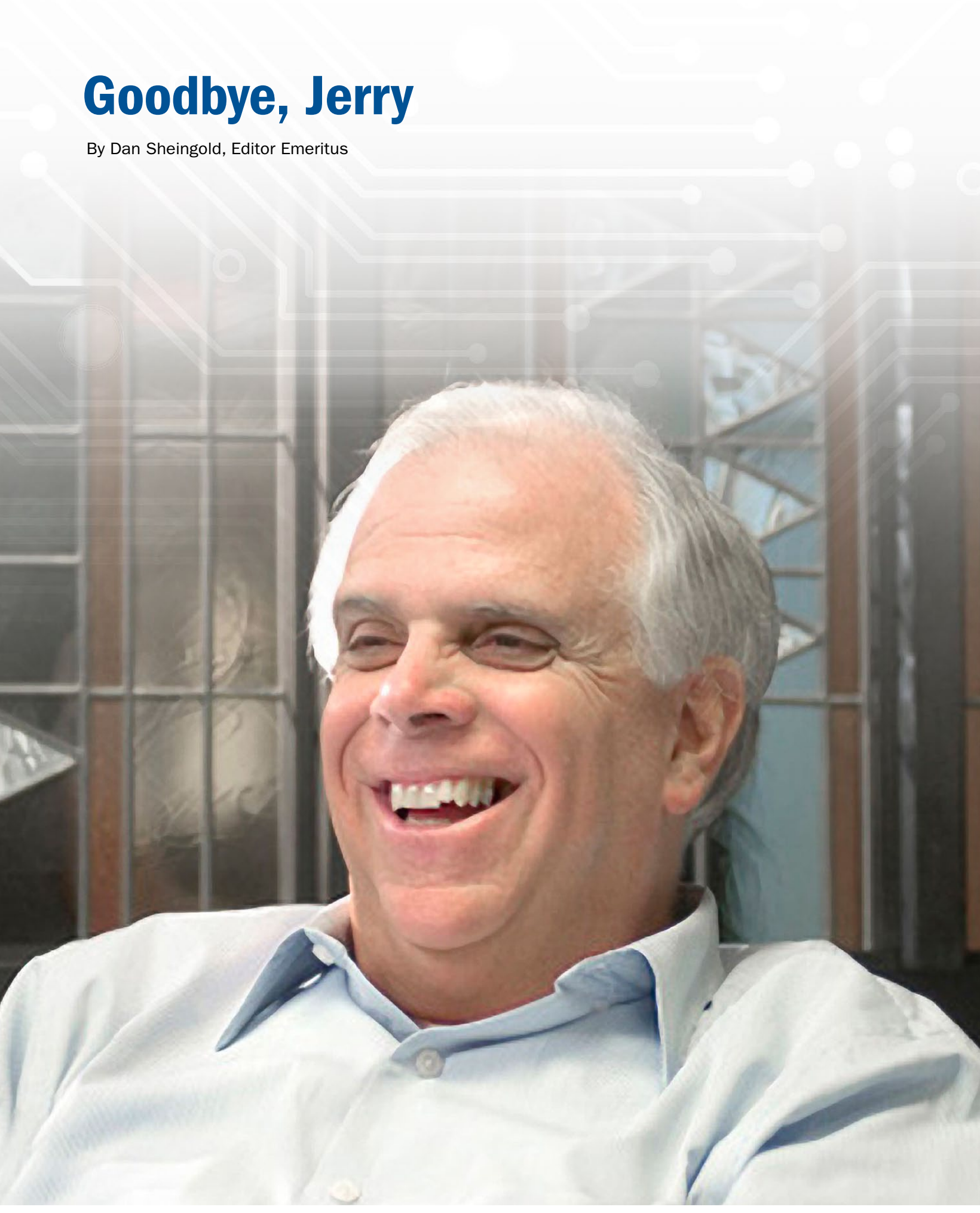
# Goodbye, Jerry

By Dan Sheingold, Editor Emeritus



Jerry Fishman's career at Analog Devices (ADI) began in 1971, in Wilmington, MA, as a marketing engineer at Nova Devices, a startup semiconductor company that later became Analog Devices Semiconductor (ADS). Until his death from a sudden heart attack, Jerry had been ADI's chief executive officer (CEO) for 17 years. During the intervening years, his many promotions included: director of marketing, ADS; general manager, ADS; executive vice president, domestic; president and chief operating officer (COO); and CEO.

Jerald G. Fishman grew up in New York City and attended Bronx High School of Science. He earned a BSEE from City College of New York in 1967, an MSEE from Northeastern University in 1970, an MBA from Boston University in 1972, and a JD (Juris Doctor) from Suffolk University Law School in 1976. He was awarded an honorary Doctor of Science degree from Brown University in 2009.

Jerry's family was the light of his life. Married for over 35 years, he and his wife derived their greatest joy from spending time with their son and daughter. Every phone call from his family was a welcome diversion that brought a smile to his face. A transplanted Bostonian, Jerry became a Red Sox fan despite his New York upbringing.

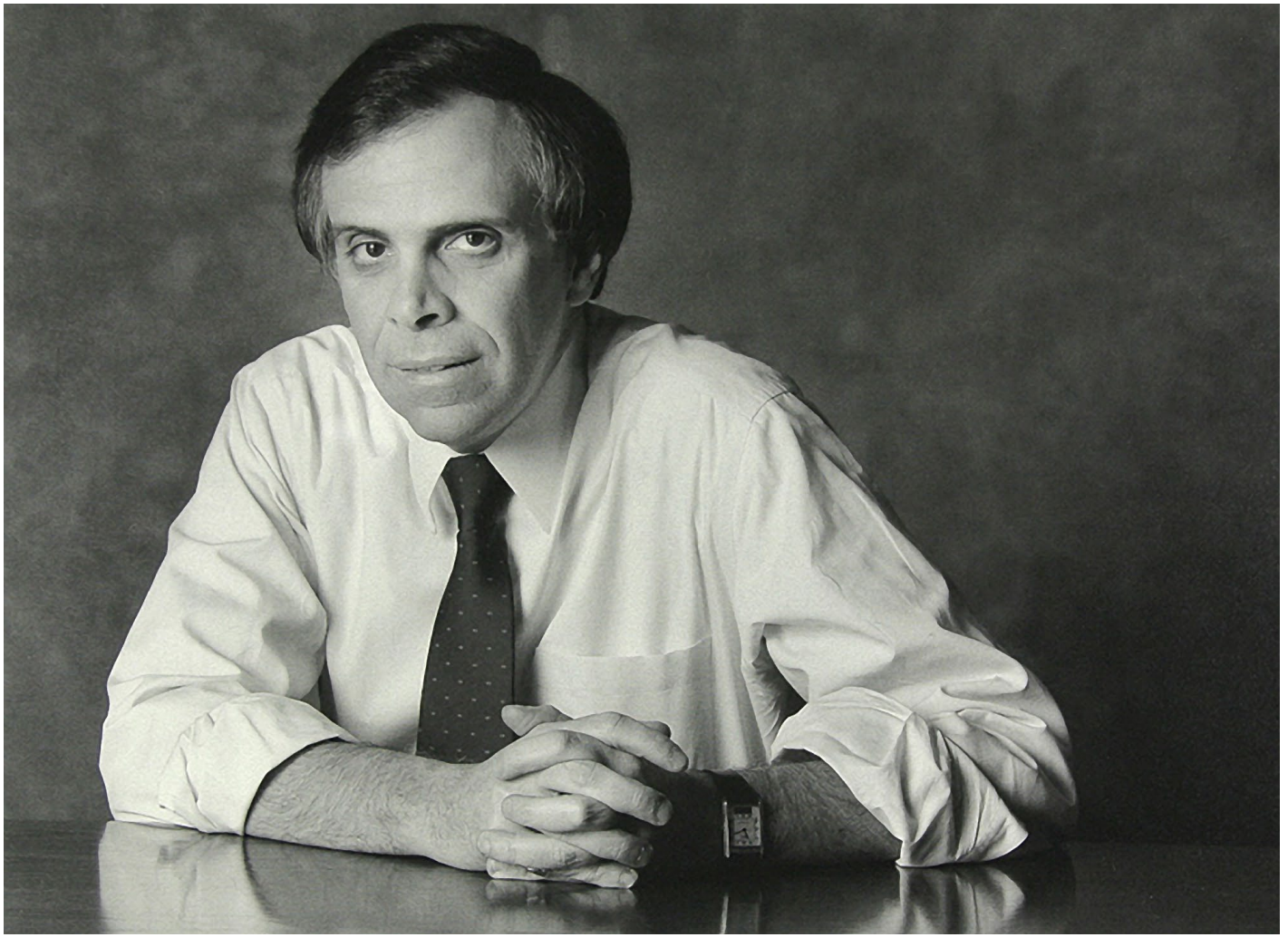
**Analog Semiconductors: "To Be or Not to Be?"**

Jerry joined ADI in its sixth year, just as ADI was entering the semiconductor business and firing up its very own fab. So, Jerry's professional history and that of ADI as a semiconductor manufacturer are tightly interwoven.

ADI's profits were generated by the lucrative module business, so the semiconductor business—with its large capital investments and low average selling prices—needed a strong, outspoken advocate. Jerry Fishman filled this role, and company founder Ray Stata believed so strongly in an IC future that he invested his own money to get Nova Devices going and, a few years later, turned it—and its growing profitability—over to ADI.

It's one thing to design novel products that the world needs, but another to manufacture them reliably and at low cost, to convince the world that they are needed, and to sell them against the inevitable competition. Jerry had an excellent head for business and was very good at asking fellow employees and managers—irrespective of rank—direct, often impolite questions (using colorful language—it was the 70s!) and insisting on accurate information. He was a master of persuasion and the use of humor. Is it any wonder that, in the years that followed, he consistently exceeded objectives, rose quickly to the attention of company management, and gained a string of promotions based on promise and performance?

Jerry was only the second CEO in ADI's history. Under his tenure, he built ADI into a multibillion dollar company that drew the attention and respect of customers, competitors, and investors. Part of Jerry's legacy was the outstanding senior management team that he built and mentored. Losing him was a major misfortune, but his team building paid off, as his heir apparent was already in place. Vincent Roche, an ADI long-timer who has worked closely with Jerry for years, was appointed as CEO in May 2013.



**Remembering Jerry**

From the early years at ADI, Jerry's intelligence and business sense were evident to all, as was his tough demeanor, a result of growing up in Queens, New York, having been a newsboy for the *New York Post,* and taking those long 1½-hour subway rides to high school in the Bronx. His managers could see that here was a potential diamond in the rough, an analytical mind that was firmly yoked to practical results and awareness of the effects of today's decisions on future results.

Doug Grant, an articulate *Planet Analog* blogger who spent many years at ADI, put it this way: "There was no mistaking where you stood with him, both on a personal and a professional level. He had a rare combination of book learning and street smarts that served him well throughout his career. He gave his best and he demanded the best from his colleagues."

Bill Schweber, another former ADI employee, adds, "Our industry has its share of colorful, high-profile, even flamboyant leaders. By his own choice, Jerry was a lower-key type, preferring to work mostly 'inside' to make sure the wheels turned smoothly and the corporate vehicle stayed on the desired course—but he also knew when to take risks and when to cut losses."

Tam Harbert, a freelance journalist who wrote for *Electronic Business,* caught the essence of the relationship between Ray Stata's vision and Jerry's down to earth ability to get it done—and what they had in common. Following his death, she blogged: "He was an intimidating presence. Jerry Fishman … was not an easy interview. But, *Electronic Business Magazine* had chosen him as its CEO of the Year … and as national editor, it was my job to profile him and his company … I expected it to be a boring assignment. But it turned out that ADI and Fishman had quite a story to tell."

Dave Kress remembers Jerry's interview for a magazine article: "We were touting our thin film prowess, and the editor asked him for some details about the process. Did he say, 'We use a 1-mil laser spot size and adjust the power to be sure that we vaporize the kerf without leaving a partially conductive edge that could drift?' No. He said, 'We line the resistors up in the microscope and blow the socks off of them.'"

Ray Stata, ADI's co-founder and chairman of the board, wrote: "Jerry dedicated his entire career to building ADI into a great company ... [his] commitment to ADI occupied a central part of his life and his passion for success was infectious. Jerry not only developed enormous respect from both inside and outside the company as one of our industry's greatest leaders, but also from those like me who knew him well. He engendered a sense of loyalty and affection through his candor, openness, and integrity, and through his unique sense of humor. We shall miss him deeply."

Tam Harbert quotes Jerry in 2004, "In technology companies, it's all about transitions. Transitions in leadership, transitions in technology, transitions in markets. It's how you manage across the transitions, I think, that more than anything separates the companies that last from those who don't."

Vincent Roche, president and CEO of ADI, wrote: "On a personal level, Jerry was a great source of encouragement and mentorship to me over the many years I worked closely with him, and for that I am fortunate and honored."

Dan Sheingold: "Jerry passed away about two months after I retired and became emeritus. I'm glad to have spent more than 40 years in the same company with Jerry and had the privilege and delight (and prosperity) of watching his progress from a brash young marketing engineer to respected head of a great company. Jerry, rest in peace."

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