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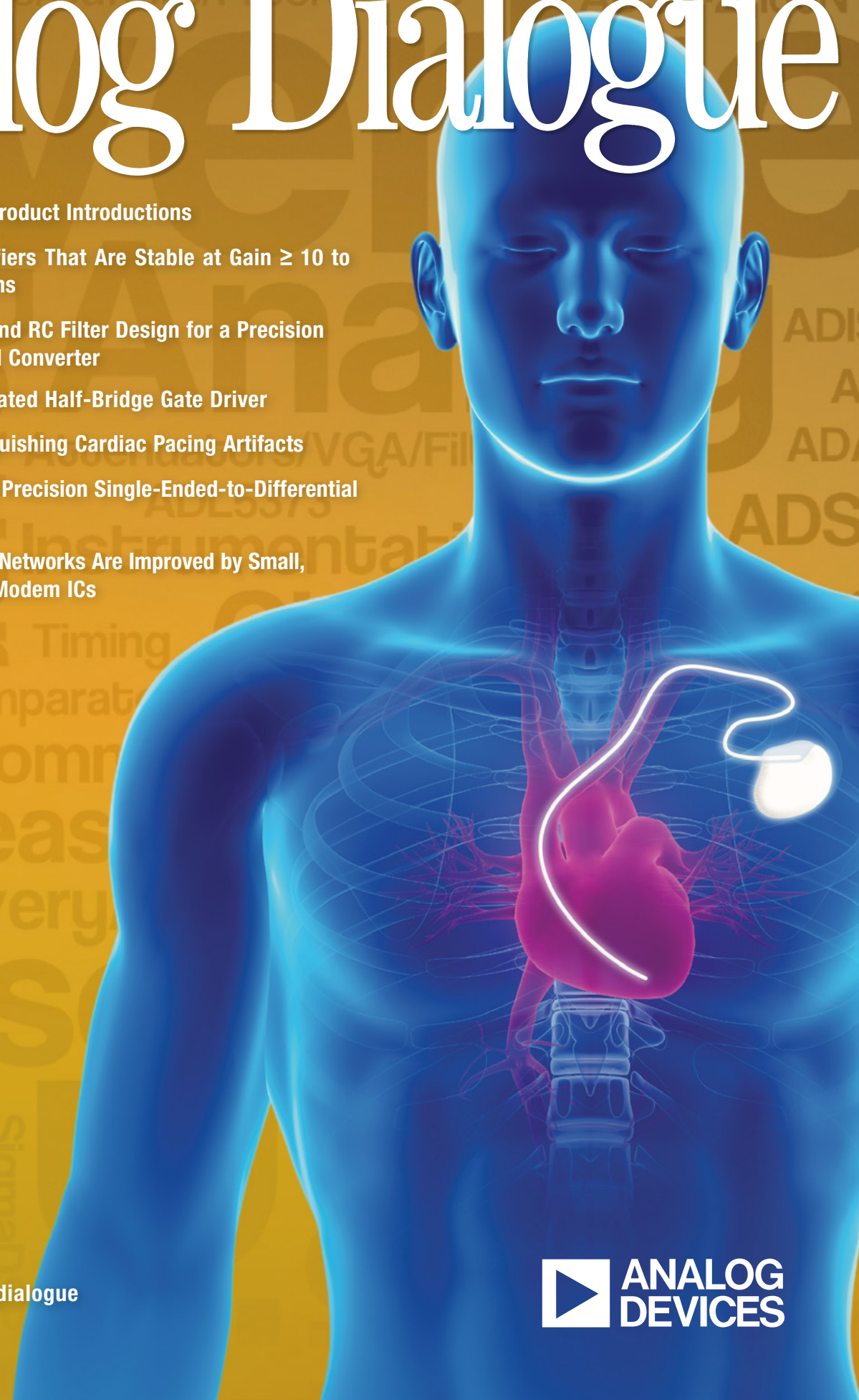

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ANALOG DEVICES

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This article shows how compensating an amplifier that is normally stable with a gain higher than +9 to operate with a gain as low as +2 provides higher slew rate and faster settling time than an equivalent internally compensated amplifier. The two methods presented here trade complexity for total wideband noise. The ADA4895-2 dual high-speed, low-power operational amplifier is used as an example. Page 3.

Front-End Amplifier and RC Filter Design for a Precision SAR Analog-to-Digital Converter

Successive-approximation ADCs offer high resolution, excellent accuracy, and low power consumption. Once a particular precision ADC has been chosen, system designers must determine the support circuitry needed to obtain the best results. The three principal areas to consider are the *front end*, the *voltage reference*, and the *digital interface*. This article focuses on the front end. Page 5.

Implementing an Isolated Half-Bridge Gate Driver

Many applications, ranging from isolated dc-to-dc power supplies to solar inverters, use isolated half-bridge gate drivers to control large amounts of power with high efficiency, power density, isolation voltage, and long-term reliability. This article discusses details of these design concepts to illustrate the ability of isolated half-bridge gate driver ICs to provide high performance in a small package. Page 10.

Detecting and Distinguishing Cardiac Pacing Artifacts

When heart patients undergo ECG testing, the cardiologist must be able to detect the presence and effects of a pacemaker. The electrical signature of the pacing signal consists of small, narrow pulses. Buried in noise and larger cardiac signals, these artifacts can be difficult to detect. This article describes the nature of pacing artifacts and introduces a device and method for detecting them. Page 13.

Versatile, Low-Power, Precision Single-Ended-to-Differential Converter

Many applications, including driving modern ADCs, transmitting signals over twisted-pair cables, and conditioning high-fidelity audio signals, require differential signaling, which achieves higher signal-to-noise ratios, increased common-mode noise immunity, and lower second-harmonic distortion. This article offers a circuit block that can convert single-ended signals to differential signals. Page 19.

HART Communication Networks Are Improved by Small, Flexible, Low-Power Modem ICs

Measurement, control, and communication with instrumentation systems employing sensors and actuators is the backbone of modern manufacturing plants. Communication employing 4-mA-to-20-mA analog signals has long been in widespread use, but instrumentation has matured from those purely analog systems to today's *smart* systems that use the HART protocol to enable two-way digital data. Page 21.

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PRODUCT INTRODUCTIONS: VOLUME 46, NUMBER 4

Data sheets for all ADI products can be found by entering the part number in the search box at www.analog.com.

October

Controller, dc-to-dc, step-down, synchronous **ADP1851**
Front-end, analog, single-lead heart-rate monitor..... **AD8232**
Supervisor, microprocessor, quad, low-voltage..... **ADM8710**
Transceiver, dual, RS-422, ±15-kV ESD protection **ADM4168E**

November

Accelerometer, MEMS, 3-axis, ±200-*g*, low-power **ADXL377**
Accelerometer, MEMS, digital, 3-axis, ±1-*g*/±2-*g*/±4-*g*/±8-*g* ... **ADXL350**
ADC, pipelined, dual, 14-bit, 170-MSPS/250-MSPS, JESD204B.... **AD9250**
Amplifier, audio, mono, 2.9-W, Class-D, digital output..... **SSM4321**
Amplifier, operational, dual, high-precision **ADA4077-2**
Amplifier, operational, dual, low-power, low-noise..... **ADA4895-2**
Front-end, analog, radar receive path, LNA/PGA/AAF/ADC..... **AD8284**
Generator, clock, eight low-jitter LVPECL outputs **AD9525**
Isolators, digital, 6-channel, 1-kV rms isolation..... **ADuM764x**
Microcontrollers, precision analog, Σ-Δ ADCs, ARM Cortex-M3 ..... **ADuCM360/ADuCM361**
Receiver, IF, dual..... **AD6673**
Regulator, dc-to-dc, step-down, 20-V, 4-A synchronous **ADP2384**
System, monitor and control, 10-bit **AD7292**

December

Accelerometer, MEMS, digital, 3-axis, ±2-*g*/±4-*g*/±8-*g*/±16-*g*..... **ADXL344**
ADC, Σ-Δ, 24-bit, 250-kSPS, 20-µs settling time **AD7176-2**
ADC, successive-approximation, 12-bit, 1-MSPS, low-power **AD7091**
Amplifier, audio, mono, 2.7-W, Class-D, PDM input..... **SSM2537**
Amplifier, operational, dual, 10-MHz, zero x'over distortion.... **ADA4500-2**
Charger, battery, power path, USB compatible..... **ADP5062**
Converter, dc-to-dc, step-up, 2 MHz..... **ADP1607**
Converters, dc-to-dc, integrated..... **ADuM5010/ADuM6010**
DAC, TxDAC+, dual, 16-bit, 1600-MSPS **AD9142**
Driver, differential line, wideband, 225-mA **ADA4312-1**
Driver, flash LED, two 750-mA outputs..... **ADP1660**
Front-end, analog, 3-electrode ECG systems, low-power **ADAS1000-3/ADAS1000-4**
Front-end, analog, 5-electrode ECG systems, low-power **ADAS1000-2**
Isolators, digital, 2-channel, 5-kV rms isolation **ADuM228x**
Potentiometers, digital, single/dual/quad, 128-/256-position..... **AD512x/AD514x**
Regulator, switching, isolated..... **ADuM4070**
Sensor, angular rate, ±14,000°/s dynamic range **ADIS16266**
Sensor, angular rate, high-performance, digital-output.... **ADXRS810**
Sensor, inertial, precision, six degrees of freedom **ADIS16445**
Splitter, HDMI, 4-input, 2-output, 2.25-GHz, XpressView..... **ADV7630**
Synthesizer, frequency, fractional-N..... **ADF4153A**
Synthesizer, PLL, 18-GHz, microwave **ADF41020**
System, data-acquisition, 8-channel, 16-bit, 1-MSPS..... **ADAS3022**

Analog Dialogue

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Compensating Amplifiers That Are Stable at Gain ≥ 10 to Operate at Lower Gains

By Charly El-Khoury

This article shows how compensating an amplifier—such as the ADA4895-2, which is normally stable for a gain higher than +9—to operate with a gain as low as +2 provides higher slew rate and faster settling time than an equivalent internally compensated amplifier. Two methods will be presented, and advantages and disadvantages of each circuit will be highlighted.

The ADA4895-2, a device in the same family as the ADA4896-2, ADA4897-1, and ADA4897-2, is a dual low-noise, high-speed, voltage-feedback amplifier with rail-to-rail outputs. Stable with a minimum gain of 10, it features 1.5-GHz gain-bandwidth product, 940-V/µs slew rate, 26-ns settling time to 0.1%, 2-nV/$\sqrt{\text{Hz}}$ 1/f noise at 10 Hz, 1-nV/$\sqrt{\text{Hz}}$ wide band noise, and −72-dBc spurious-free dynamic range at 2 MHz. Operating with a 3-V to 10-V supply, it draws a quiescent current of 3 mA per amplifier.

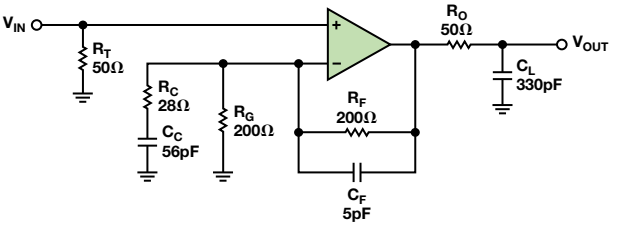

Figure 1. Method 1: Compensating the ADA4895-2 for a stable gain of +2.

Method 1, shown in Figure 1, adds a simple RC circuit (R_C = 28 Ω and C_C = 56 pF) to the inverting input and a feedback capacitor (C_F = 5 pF) in parallel with the feedback resistor. The circuit has a noise gain of +9 at high frequencies and a gain of +2 at frequencies below the resonance frequency, $1/2\pi R_C C_C$ = 100 MHz. Even though the noise gain at higher frequencies is approximately +9, the total output noise can be kept low as long as the low-pass filter, formed with R_O and C_L, blocks the high-frequency content. This allows the amplifier to operate at a gain of +2 while keeping the total output noise very low (3.9 nV/$\sqrt{\text{Hz}}$).

This configuration is scalable to accommodate any gain between +2 and +9. Table 1 shows the component values and total wideband output noise for each gain setting.

Table 1. Component Values Used for Gain < +10. R_T = R_O = 49.9 Ω.

Gain	R_C (Ω)	C_C (pF)	R_G (Ω)	R_F (Ω)	C_L (pF)	Total Output Noise[1] (nV/$\sqrt{\text{Hz}}$)
+2	28.6	56	200	200	330	3.88
+3	33.3	56	100	200	270	5.24
+4	40	56	66.7	200	200	6.60
+5	50	56	50	200	150	7.96
+6	66.7	40	40	200	150	9.32
+7	113	30	37.5	226	120	10.82
+8	225	20	32.1	226	120	12.18
+9	N/A	N/A	31.1	249	100	13.67

[1]See the complete total noise equation below.

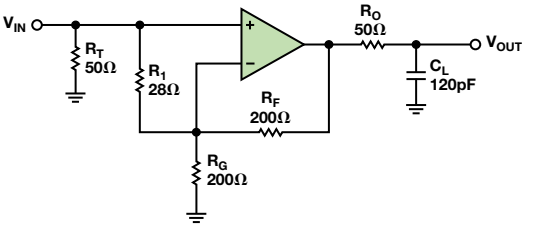

Figure 2. Method 2: Compensating the ADA4895-2 for a stable gain of +2.

Method 2, shown in Figure 2, adds a resistor (R_1 = 28 Ω) between the inverting and noninverting inputs to increase the amplifier's noise gain to +9. No voltage appears across R_1, so no current flows through it. Thus, the input impedance looking into R_1 in parallel with the noninverting input will remain high. The input-to-output signal gain is equal to 1 + R_F/R_G, or +2 in this case. No capacitor is used in the compensation circuit, so there is no frequency dependency. This means that the wideband output noise is always higher at lower frequencies as compared to the first method.

This configuration is also scalable to accommodate any gain between +2 and +9. Table 2 shows the component values and total wideband output noise for each gain setting.

Table 2. Component Values Used for Gain < +10. R_T = R_O = 49.9 Ω, C_L = 120 pF.

Gain	R_1 (Ω)	R_G (Ω)	R_F (Ω)	Total Output Noise[1] (nV/$\sqrt{\text{Hz}}$)
+2	28.6	200	200	13.39
+3	33.3	100	200	13.39
+4	40	66.5	200	13.39
+5	49.9	49.9	200	13.39
+6	66.5	40	200	13.39
+7	113	37.4	226	13.53
+8	225	32.4	226	13.53
+9	N/A	30.9	249	13.67

[1]See the complete total noise equation below.

Figure 3 shows the small signal and large signal frequency responses of the circuits shown in Figure 1 and Figure 2 into a 50-Ω analyzer, with G = +5 V/V or 14 dB. As shown, both circuits are very stable, and the peaking is a little over 1 dB. This stability will apply throughout the range of gains between +2 and +9 as long as the values in Table 1 and Table 2 are used.

For better total output noise, the low-pass RC filter at the output can be adjusted to cut the bandwidth of this circuit at 50 MHz or below, depending on the application.

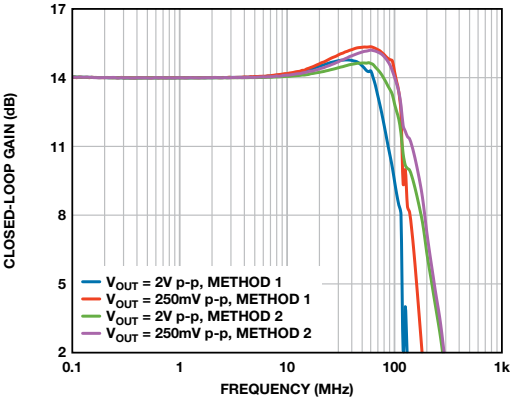

Figure 3. Frequency response for G = +5.

Equation for Method 1: total output noise =

$$\sqrt{\left(\sqrt{4KTR_T}\times\left(1+\frac{R_F}{R_G}\right)\right)^2+\left(e_n\times\left(1+\frac{R_F}{R_G}\right)\right)^2+\left(i_n\times10^{-3}\times R_T\times\left(1+\frac{R_F}{R_G}\right)\right)^2+\left(\sqrt{4KTR_G}\times\left(\frac{R_F}{R_G}\right)\right)^2+\left(i_n\times10^{-3}\times R_F\right)^2+\left(\sqrt{4KTR_F}\right)^2+\left(\sqrt{4KTR_O}\right)^2}$$

Equation for Method 2: total output noise =

$$\sqrt{\left(\sqrt{4KTR_T}\times\left(1+\frac{R_F}{R_E}\right)\right)^2+\left(e_n\times\left(1+\frac{R_F}{R_E}\right)\right)^2+\left(i_n\times10^{-3}\times R_T\times\left(1+\frac{R_F}{R_E}\right)\right)^2+\left(\sqrt{4KTR_E}\times\left(\frac{R_F}{R_E}\right)\right)^2+\left(i_n\times10^{-3}\times R_F\right)^2+\left(\sqrt{4KTR_F}\right)^2+\left(\sqrt{4KTR_O}\right)^2}$$

Why the Output Noise Is Better in Method 1 as Compared to Method 2

The output noise of Method 1 is much lower than that of Method 2, especially at gains below +7, because the noise gain of Method 1 is only high at high frequencies. At this point, a low-pass filter can be used to eliminate the high-frequency noise content. In Method 2, on the other hand, the amplifier is always operating at a noise gain of +9, even at low frequencies. Thus, the total output noise does not vary with the gain, as shown in Table 2. The equations above correspond to the two methods (note: $R_E = R_G//R_1$).

Advantages and Disadvantages of Each Method

We have shown two different methods, using a few external components, to make an amplifier that is designed for stability at higher gains operate stably at lower gain. Method 1 uses more passive components, which can increase board space and add cost as compared to Method 2. In return, the total output noise of the first circuit is lower than that of the second circuit. Therefore, the circuit choice will be determined by the application and its required specifications.

As shown in Figure 4, the decompensated ADA4895-2 provides a higher slew rate (300 V/μs vs. 100 V/μs) and faster settling time as compared to the internally compensated ADA4897-2, which is stable for gains ≥ +1. These advantages increase as the circuit gain increases.

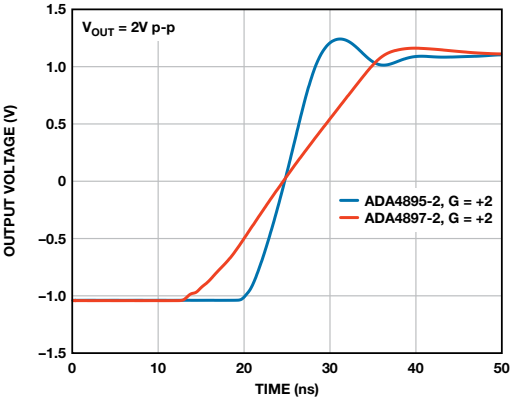

Figure 4. Comparing the compensated and decompensated amplifiers at G = +2.

Conclusion

A decompensated amplifier, such as the ADA4895-2, which is stable for G ≥ +10, can be compensated to allow operation at lower gains. The two methods presented here trade complexity for total wideband noise. Both provide higher slew rate and faster settling time than the equivalent internally compensated ADA4897-2, which is stable for G ≥ +1.

Author

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Front-End Amplifier and RC Filter Design for a Precision SAR Analog-to-Digital Converter

By Alan Walsh

Successive-approximation (SAR) ADCs offer high resolution, excellent accuracy, and low power consumption. Once a particular precision SAR ADC has been chosen, system designers must determine the support circuitry needed to obtain the best results. The three principal areas to consider are the *front end*, which interfaces the analog input signal to the ADC, the *voltage reference*, and the *digital* interface. This article focuses on the circuit requirements and trade-offs in designing the front end. Useful information on the other areas, which are device- and system-specific, can be found in data sheets—and in this article's references.

The front end consists of two parts: the driving amplifier and the RC filter. The amplifier conditions the input signal—as well as acting as a low-impedance buffer between the signal source and the ADC input. The RC filter limits the amount of out-of-band noise arriving at the ADC input and helps to attenuate the kick from the switched capacitors in the ADC's input.

Choosing the right amplifier and RC filter for a SAR ADC can be a challenge, especially when the application needs to differ from the routine data sheet usage of the ADC. Looking at the various application factors that influence amplifier and RC choice, we provide design guidelines that lead to the best solution. Major considerations include *input frequency*, *throughput*, and *input multiplexing*.

Selecting a Suitable RC Filter

To select a suitable RC filter, we must calculate the RC bandwidth for single-channel or multiplexed applications, then select values for R and C.

Figure 1 shows a typical amplifier, single-pole RC filter, and ADC. The ADC input presents a switched-cap load to the driving circuitry. Its 10-MHz input bandwidth means that low-noise is needed over a wide bandwidth to get a good signal-to-noise ratio (SNR). The RC network limits the bandwidth of the input signal and reduces the amount of noise fed to the ADC by the amplifier and upstream circuitry. Too much band limiting will increase the settling time and distort the input signal, however.

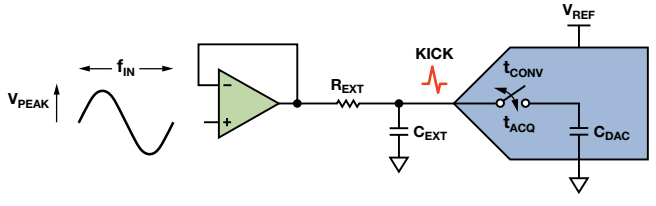

Figure 1. Typical amplifier, RC filter, and ADC.

The minimum RC value needed to settle the ADC input while also optimally band limiting the noise can be calculated assuming exponential settling of a step input. To calculate the size of the step, we need to know the input signal frequency, amplitude, and ADC conversion time. The *conversion time*, t_{CONV} (Figure 2), is when the capacitive DAC is disconnected from the input and is performing bit trials to generate the digital code. At the end of the conversion time, the capacitive DAC, which holds the previous sample charge, is switched back to the input. This step change represents how much the input signal has changed in that time. The time taken to settle this step is known as the *reverse settling time*.

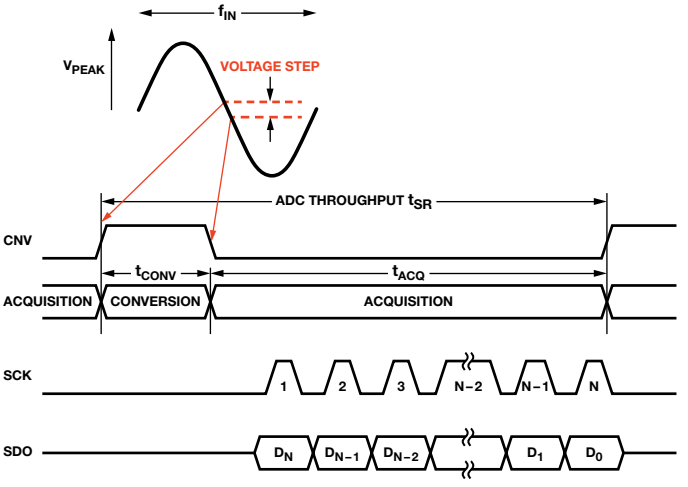

Figure 2. Typical timing diagram for N-bit ADC.

The maximum undistorted rate of change of a sine wave signal with a given input frequency can be calculated as

$$2\pi f_{IN} V_{PEAK}$$

If the conversion rate of the ADC is considerably higher than the maximum input frequency, the maximum amount the input voltage has changed during the conversion time is given by

$$2\pi f_{IN} V_{PEAK} t_{CONV}$$

This is the maximum voltage step that is seen by the capacitive DAC when it is switched back to acquire mode. This step is then attenuated by the parallel combination of the DAC's capacitance and that of the external capacitor. For this reason, it is important that the external capacitor be relatively large—a few nanofarads. This analysis will assume that the on resistance of the input switch has a negligible effect. The step size that now needs to be settled is given by

$$V_{STEP} = \frac{2\pi f_{IN} V_{PEAK} t_{CONV} C_{DAC}}{C_{EXT} + C_{DAC}}$$

Next, calculate the time constant to settle the ADC input to ½ LSB during the acquisition time of the ADC. Assuming exponential settling of the step input, the required RC time constant, τ, is

$$\tau = \frac{t_{ACQ}}{N_{TC}}$$

where t_{ACQ} is the acquisition time and N_{TC} is the number of time constants required to settle. The number of time constants required can be calculated from the natural logarithm of the ratio of the step size, V_{STEP}, to the settling error—which in this case is ½ LSB,

$$V_{half\_lsb} = \frac{V_{REF}}{2^{N+1}}$$

giving

$$N_{TC} = \ln\left(\frac{V_{STEP}}{V_{half\_lsb}}\right)$$

Substituting this in the previous equation gives

$$\tau = \frac{t_{ACQ}}{\ln\left(\frac{V_{STEP}}{V_{half\_lsb}}\right)}$$

And the equivalent RC bandwidth is $\frac{1}{2 \times \pi \times \tau}$

Example: Armed with an equation for calculating the RC bandwidth, choose the AD7980 16-bit ADC—shown in Figure 3—with its 710-ns conversion time, 1-MSPS throughput, and 5-V reference. The maximum input frequency of interest is 100 kHz. Calculating the maximum step size at this frequency gives

$$2\pi(100\text{ kHz})\left(\frac{5\text{ V}}{2}\right)(710\text{ ns}) = 1.115\text{ V}$$

This step is then attenuated by the charge from the external capacitor. Using a DAC capacitance of 27 pF and assuming a 2.7-nF external capacitance, the attenuation factor will be about 101. Plugging these numbers into the equation for V_{STEP} gives

$$V_{STEP} = \frac{1.115\text{ V} \times 27\text{ pF}}{2.7\text{ nF} + 27\text{ pF}} = 11.042\text{ mV}$$

Next, calculate the number of time constants to settle to ½ LSB at 16 bits; with a 5-V reference

$$N_{TC} = \ln\left(\frac{11.042\text{ mV}}{\frac{5\text{ V}}{2^{16+1}}}\right) = 5.668$$

The acquisition time is

$$t_{ACQ} = t_{SR} - t_{CONV} = \frac{1}{1\text{ MSPS}} - 710\text{ ns} = 290\text{ ns}$$

Calculating for τ,

$$\tau = \frac{290\text{ ns}}{5.668} = 51.16\text{ ns}$$

So, bandwidth = 3.11 MHz and R_{EXT} = 18.9 Ω.

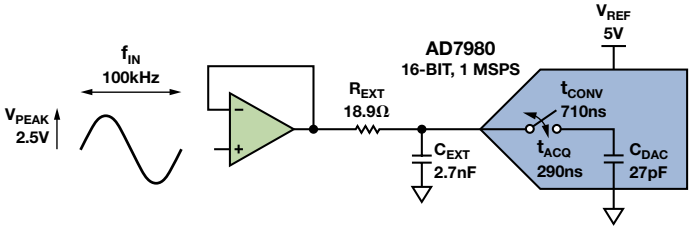

Figure 3. RC filter using AD7980 16-bit, 1-MSPS ADC.

This relationship between the minimum bandwidth, throughput, and input frequency shows that higher input frequencies require a higher RC bandwidth. Similarly, higher throughput, which results in lower acquisition time, increases the RC bandwidth. The acquisition time has the largest influence on the bandwidth needed; if it were doubled (reducing throughput), the bandwidth required would be halved. This simplified analysis does not include second-order charge kickback effects that become dominant at lower frequencies. In the case of very low input frequencies (<10 kHz), including dc, there will always be ~100 mV of voltage step to settle on the cap DAC. This number should be used as the minimum possible voltage step in the analysis above.

A *multiplexed* input signal is rarely continuous, typically consisting of large steps when switching between channels. In the worst case, one channel is at negative full scale, while the next channel is at positive full scale (see Figure 4). In this case, the step size will be the full range of the ADC, or 5 V in the above example, when the mux switches channels.

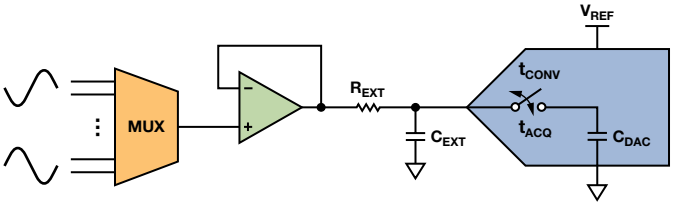

Figure 4. Multiplexed setup.

When using a multiplexed input in the above example, the required filter bandwidth for linear response would increase to 3.93 MHz (step size = 5 V vs. 1.115 V with a single channel). This assumes the mux switches shortly after conversion begins (Figure 5) and that the amplifier and RC forward settling time is sufficient to settle the input capacitor before acquisition begins.

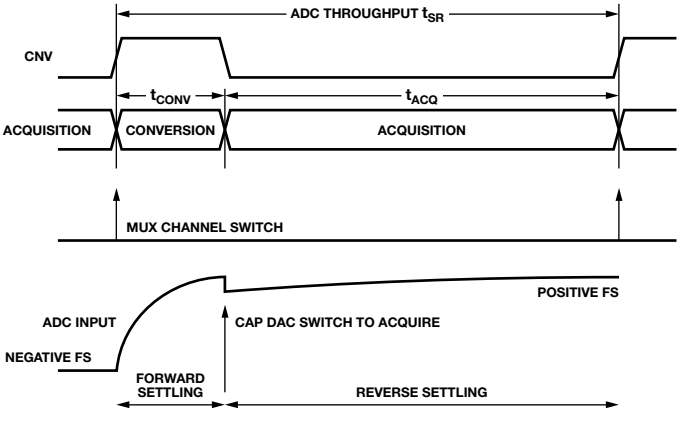

Figure 5. Multiplexed timing.

This can be checked for the calculated RC bandwidth by using Table 1. From the table, 11 time constants are needed to settle a full-scale step to 16 bits (Table 1). For the calculated RC, the forward settling time of the filter is 11 × 40.49 ns = 445 ns, which is much less than the conversion time of 710 ns. The forward settling does not necessarily have to occur completely during the conversion time (before the cap DAC gets switched to the input), but the combined forward and reverse settling time should not exceed the required throughput rate. Forward settling is less important for low-frequency inputs, as the rate of change of the signal is much lower.

Table 1. Number of Time Constants to Settle to N-Bit Resolution

Resolution (Bits)	LSB (%FS)	No. of Time Constants to 1- LSB Error
6	1.563	4.16
8	0.391	5.55
10	0.0977	6.93
12	0.0244	8.32
14	0.0061	9.70
16	0.0015	11.09
18	0.00038	12.48
20	0.000095	13.86
22	0.000024	15.25

With an approximate filter bandwidth calculated, the individual values of R_{EXT} and C_{EXT} can be chosen. The calculations above assume that C_{EXT} = 2.7 nF. This is a typical value in application circuits shown on data sheets. If a larger capacitor were chosen, there would be greater attenuation of the kick when the cap DAC is switched in. However, the larger the capacitance, the greater the chance the driving amplifier will become unstable, especially as the value of R_{EXT} gets smaller for a given bandwidth. If the value of R_{EXT} is too small, the amplifier phase margin will be degraded, potentially causing the amplifier output to ring or become unstable. Amplifiers with low output impedance should be used to drive loads with smaller series R_{EXT}. A stability analysis can be performed using Bode plots for the RC combination and amplifier to verify sufficient phase margin. It is best to choose a capacitance value of 1 nF to 3 nF and a reasonable resistance value that will keep the driving amplifier stable. It is also important to use capacitors with a low voltage coefficient, such as NP0 types, to keep distortion low.

It is important that the value of R_{EXT} keeps the level of distortion within requirements. Figure 6 shows the effect of the resistance of the driving circuit on distortion as a function of frequency for the AD7690. Distortion increases with both input frequency and source resistance. The cause of this distortion is mainly the nonlinear nature of the impedance presented by the cap DAC.

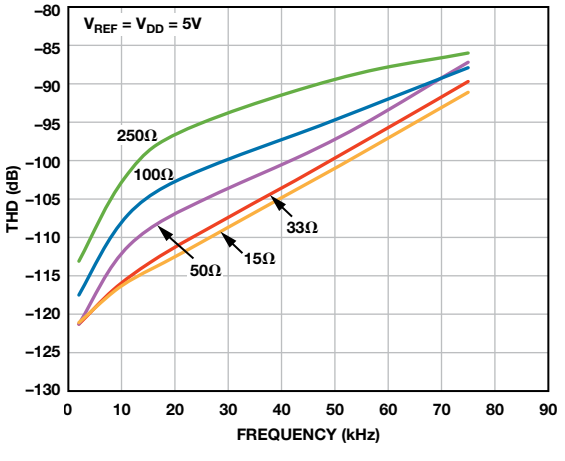

Figure 6. Effect of source resistance on THD vs. input frequency.

Larger series resistance values can be tolerated for low input frequencies (<10 kHz). The distortion is also a function of the input signal amplitude; a lower amplitude will allow a higher value of resistance for the same distortion level. Calculating for R_{EXT} in the example above, where τ = 51.16 ns and C_{EXT} is assumed to be 2.7 nF, yields a resistor value of 18.9 Ω. These are close to common values seen in application sections of Analog Devices data sheets.

The nominal RC values calculated here are useful guidelines, not a final solution. Choosing the right balance between the R_{EXT} and C_{EXT} requires knowledge of the input frequency range, how much capacitance the amplifier can drive, and the acceptable level of distortion. In order to optimize the RC value, it is important to experiment with actual hardware to arrive at the best performance.

Selecting a Suitable Amplifier

In the previous section, we calculated the RC bandwidth suitable for the ADC input, based on input signal and ADC throughput. Next, this information must be used to select a suitable amplifier to drive the ADC. The following aspects will be considered:

- Amplifier large and small signal bandwidth
- Settling time
- Amplifier noise specification and effect on system noise
- Distortion
- Headroom requirements for distortion and resulting supply rails

An amplifier's *small-signal bandwidth* is typically specified on its data sheet. Depending on the type of input signal, however, the *large-signal bandwidth* may be more important. This is especially the case for high input frequencies (>100 kHz) or multiplexed applications—due to the large voltage swings—and forward settling of the input signal is more critical. For example, the ADA4841-1 has an 80-MHz small-signal bandwidth (20 mV p-p signal), but its large-signal bandwidth is 3 MHz (2 V p-p signal). In the above example, using the AD7980, the calculated RC bandwidth was 3.11 MHz. The ADA4841-1 is a good choice for lower input frequencies, as its 80-MHz small-signal bandwidth is more than sufficient for reverse settling, but it would struggle in a multiplexed application—where the RC bandwidth requirement increases to 3.93 MHz for a large signal swing. A more suitable amplifier in this case would be the ADA4897-1, which has a 30 MHz large-signal bandwidth. In general, the small/large signal bandwidth of the amplifier should be at least two to three times greater than the RC bandwidth, depending on whether the reverse or forward settling is dominant. This is especially applicable if the amplifier stage is required to provide voltage gain, which will reduce the available bandwidth; an amplifier with even wider bandwidth may be required.

Another way of looking at the forward settling requirement is to look at the amplifier's settling-time specification, usually the time required to settle to a percentage of the specified step size. For 16- to 18-bit performances, settling to 0.001% is typically required—but most amplifiers are specified for 0.1% or 0.01%, with varying step sizes; hence, some compromises with the numbers are needed in order to get a good idea whether the settling behavior could be acceptable for the ADC throughput. The ADA4841-1 specified settling time to 0.01% is 1 μs for an 8-V step. In a muxed application driving the AD7980 at 1 MSPS (1-μs period), it will not be able to settle the input in time for a full-scale step, but a lower throughput of, say, 500 kSPS may be possible.

The RC bandwidth is important in determining the maximum amount of noise allowed in the amplifier. Amplifier noise is generally specified by low-frequency 1/f noise (0.1 Hz to 10 Hz) and wideband noise spectral density at a higher frequency on the flat part of the noise curve (Figure 7).

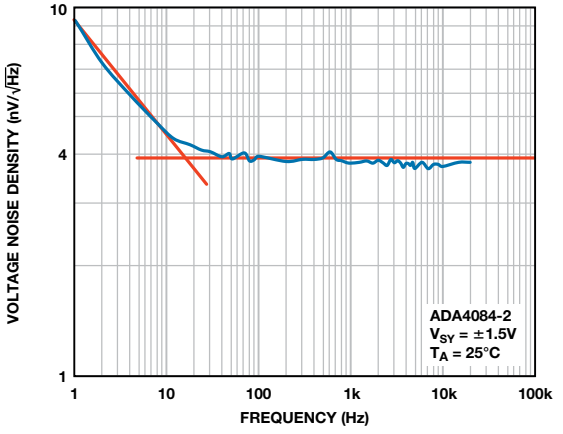

Figure 7. Voltage noise vs. frequency for the ADA4084-2.

The total noise referred to the input of the ADC can be calculated as follows. First, calculate the noise due to the wideband spectral density of the amplifier over the RC bandwidth

$$v_{n,\,rms} = Ne_{n,\,rms}\sqrt{\frac{\pi}{2}BW_{RC}}$$

where e_n = noise spectral density in nV/√Hz, N = amplifier circuit noise gain, and BW_{RC} = RC bandwidth in Hz.

Next, add in the low-frequency 1/f noise, which is usually specified peak-to-peak and needs to be converted to rms, typically using this equation

$$v_{n,1/f,\,rms} = N\frac{v_{n,1/f,\,pk-pk}}{6.6}$$

where $v_{n,1/f,\,pk-pk}$ = 1/f peak-to-peak noise voltage and N = amplifier circuit noise gain.

Total noise is then given by the root-sum-square:

$$v_{n,\,total} = \sqrt{v_{n,\,rms}^2 + v_{n,1/f,\,rms}^2}$$

This total noise should be ~1/10 of the noise of the ADC in order to have a minimal effect on the overall SNR. Higher noise may be allowable, depending on the target system's SNR. For example, if the ADC's SNR = 91 dB, with V_{REF} = 5 V, then the total noise should be less than or equal to

$$\frac{5\text{ V}}{2\sqrt{2}}10^{\left(-\frac{91\text{ dB}}{20}-1\right)} = 5\ \mu\text{V rms}$$

From this number, it is easy to work out maximum allowable specifications for 1/f noise and wideband noise spectral density. Assuming that the amplifier under consideration has negligible 1/f noise, operates at unity gain, and uses a filter with the RC bandwidth calculated previously, 3.11 MHz, then

$$v_{n,\,rms} = 5\ \mu\text{V} \Rightarrow e_{n,\,rms} = \frac{5\ \mu\text{V}}{(1)\sqrt{\frac{\pi}{2}(3.11\text{ MHz})}} = 2.26\text{ nV}/\sqrt{\text{Hz}}$$

Thus, the amplifier must have a wideband noise spectral density ≤ 2.26 nV/√Hz. The ADA4841-1 meets this criterion with a specification of 2.1 nV/√Hz.

Another important specification to consider for the amplifier is the distortion at a particular input frequency. Typically, for best performance, total harmonic distortion (THD) of ~100 dB is required at 16 bits and ~110 dB for 18-bit ADCs at the input frequency of interest. Figure 8 shows a typical distortion vs. frequency plot for the ADA4841-1 for a 2-V p-p input signal.

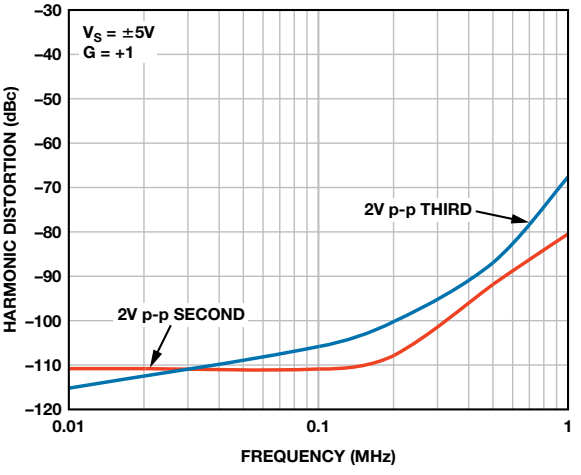

Figure 8. Distortion vs. frequency for the ADA4841-1.

Instead of showing total harmonic distortion, the plot is broken out into the generally most dominant second and third harmonic components. The ADA4841-1 is sufficiently clean to drive an 18-bit ADC up to ~30 kHz with excellent distortion characteristics. As the input frequency approaches 100 kHz and beyond, the distortion performance begins to degrade. For lower distortion at higher frequencies, a higher-power, wider-bandwidth amplifier will be required. Larger signals will also reduce performance. For an ADC input of 0 V to 5 V, the distortion performance signal range increases to 5-V p-p. This will produce differing performance from the distortion plot shown in Figure 8, so the amplifier potentially requires testing to make sure it still meets requirements. Figure 9 compares distortion performance at several output voltage levels.

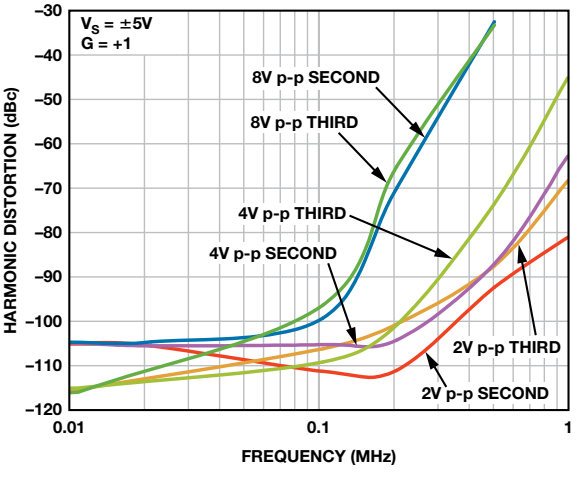

Figure 9. Distortion vs. frequency for various output voltage levels.

The THD can also be affected by the headroom—the difference between the amplifier's maximum practical input/output swing and the positive and negative supply rails. Amplifiers can have rail-to-rail inputs and/or outputs, or require up to 1 V or more headroom. Even with rail-to-rail inputs/outputs, it is difficult to get good distortion if running at a signal level that is close to the rails of the amplifier. For this reason, it is a good idea to choose supply levels that keep the maximum input/output signal away from the rails. Consider, for example, an ADC with a 0 V-to-5-V input range driven by an ADA4841-1 amplifier and a need to maximize the range of the ADC. The amplifier has a rail-to-rail output and a 1-V headroom requirement on the input. If used as a unity gain buffer, at least 1-V input headroom is needed, so the positive supply must be at least 6 V. The output is rail to rail but still can only drive to within ~25 mV of ground or the positive rail, so a negative rail is needed in order to drive all the way to ground. The negative rail could be –1 V, for example, in order to leave a margin for distortion performance.

The negative supply could be eliminated if it were feasible to lose some SNR by accepting a reduction in the ADC input range. For example, if the ADC's input range were to be reduced to 0.5 V to 5 V, this 10% loss of the ADC range would result in a ~1-dB reduction in SNR. However, this would allow the negative rail to be connected to ground, thus eliminating the circuitry necessary to generate the negative supply, reducing power consumption and cost.

Thus, when selecting the amplifier, it is important to consider the input and output signal range requirements, as this will determine the supply voltage needed. In this example, an amplifier rated for 5-V operation would not suffice; the ADA4841-1 is specified up to 12 V, however, so using a higher supply voltage will allow it to work well—with adequate supply margins.

Additional Information About the Featured Devices

Low-Power, Low-Noise, Low-Distortion Operational Amplifier Has Rail-to-Rail Output

The ADA4841-1 low-power op amp's 2-nV/$\sqrt{\text{Hz}}$ wideband noise and –110-dBc spurious-free dynamic range (SFDR) make it ideal for driving 16- and 18-bit PulSAR® ADCs—and for use in portable instrumentation, industrial process control, and medical equipment. Unity-gain stable, its specifications include 60-μV input offset voltage, 114-dB open-loop gain, 114-dB common-mode rejection, 80 MHz bandwidth (–3 dB), 12-V/μs slew rate, and 175-ns settling time to 0.1%. The input signal can extend 100 mV below the negative rail, and the output can swing to within 100 mV of either rail, providing true single-supply capability. Operating on a single 2.7-V to 12 V supply or ±1.5-V to ±6-V dual supplies, the ADA4841-1 consumes 1.1 mA in *normal* mode and 40 μA in *power-down* mode. Available in an 8-lead SOIC package, it is specified from –40°C to +125°C and priced at $1.59 in 1000s.

Low-Noise, Low-Power Op Amps Feature Rail-to-Rail Outputs

The ADA4897-1 low-noise, high-speed operational amplifier features rail-to-rail outputs, 1 nV/$\sqrt{\text{Hz}}$ voltage noise, 2.8-pA/$\sqrt{\text{Hz}}$ current noise, 230-MHz bandwidth, 120-V/μs slew rate, 45-ns settling time, and unity-gain stability, making it ideal for a variety of applications, including ultrasound, low-noise preamplifiers, driving high-performance ADCs, and buffering high-performance DACs. Operating on a single 3-V to 10-V supply, the AD4897-1 draws 3 mA. Available in 8-lead MSOP, LFCSP, and SOIC packages, it is specified from −40°C to +125°C and priced from $1.89 in 1000s.

16-Bit, 1-MSPS Successive-Approximation ADC Operates on 7 mW

The AD7980 low-power successive-approximation ADC achieves 16-bit resolution with no missing codes at a 1-MSPS sampling rate. Accepting pseudo-differential inputs with a 0-to-V_{REF} range, it specifies 91.5-dB signal-to-noise-and-distortion (SINAD), –110-dB total harmonic distortion (THD), and ±1.25-LSB maximum integral nonlinearity. Its successive-approximation architecture ensures that there will be no pipeline delays; and daisy-chaining allows several ADCs to share a single bus. Automatically powering down between conversions, its power consumption scales with throughput rate. Operating on a single 2.5-V supply, the AD7980 consumes 7 mW at 1 MSPS, 70 μW at 10 kSPS, and 350 pA in *standby* mode. Available in a 10-lead MSOP package, it is specified from –40°C to +85°C and priced from $11.95 in 1000s.

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Implementing an Isolated Half-Bridge Gate Driver

By Brian Kennedy

Many applications, ranging from isolated dc-to-dc power supply modules that call for high power density and efficiency, to solar inverters, where high isolation voltage and long-term reliability are critical, use isolated half-bridge gate drivers to control large amounts of power. This article will discuss details of these design concepts to illustrate the ability of isolated half-bridge gate driver ICs to provide high performance in a small package.

A basic half-bridge driver with optocoupler isolation, shown in Figure 1, controls output power by driving the gates of high- and low-side N-channel MOSFETs (or IGBTs) with signals of opposite polarity. The drivers must have low output impedance, to reduce conduction losses, and fast switching—to reduce switching losses. For accuracy and efficiency, the high- and low-side drivers need very closely matched timing characteristics in order to reduce the dead time when one switch of the half bridge turns off before the second switch turns on.

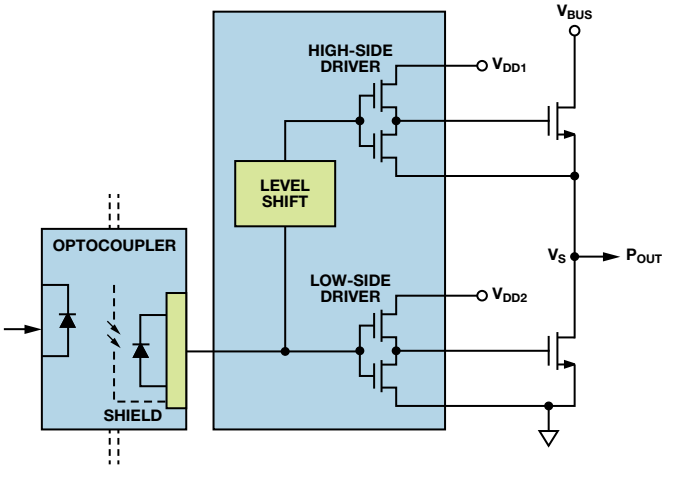

Figure 1. High-voltage half-bridge gate driver.

As shown, a conventional approach to implementing this function uses an optocoupler for isolation, followed by a high-voltage gate-driver IC. A potential drawback of this circuit is that the single isolated input channel relies on the high-voltage driver circuit for the needed channel-to-channel timing match, as well as the required dead time. Another concern is that high-voltage gate drivers do not have galvanic isolation; instead, they rely on the IC's junction isolation to separate the high-side drive voltage from the low-side drive voltage. Parasitic inductance in the circuit can cause the output voltage, V_S, to go below ground during a low-side switching event. When this happens, the high-side driver can latch up and become permanently damaged.

Optocoupler Gate Driver

Another approach, shown in Figure 2, avoids the problems of high-side to low-side interactions by using two optocouplers and two gate drivers to establish galvanic isolation between the outputs. The gate-driver circuit is often included in the same package as the optocoupler, so two separate optocoupler-gate-driver ICs are commonly required to complete the isolated half bridge—increasing the physical solution size. Note also that the optocouplers are manufactured separately, even if two are packaged together, limiting the ability to match the two channels. Allowing for this mismatch will increase the required dead time between switching one channel off and turning the other channel on, reducing efficiency.

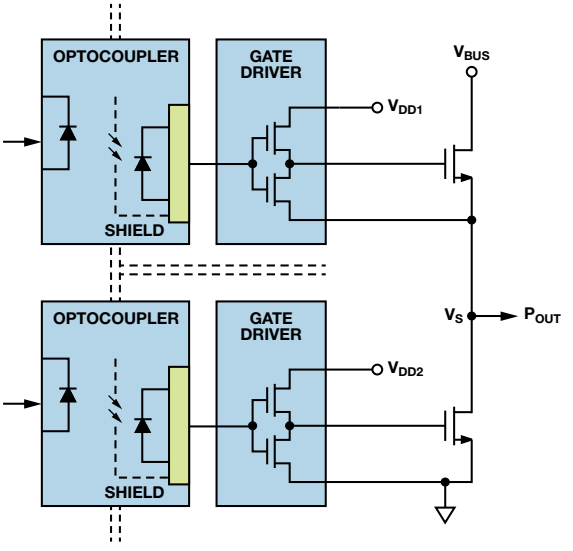

Figure 2. Dual optocoupler half-bridge gate driver.

The optocoupler's response speed is limited by the capacitance of the primary side light-emitting diode (LED); while driving the output to speeds up to 1 MHz, it will also be limited by its propagation delay (500 ns max) and slow rise and fall times (100 ns max). To run an optocoupler near its maximum speed, the LED current must be increased to more than 10 mA, consuming more power and reducing the optocoupler's lifetime and reliability—especially in the high-temperature environments common in solar inverter and power supply applications.

Pulse Transformer Gate Driver

Next, consider circuits where the galvanic isolation is provided by transformer coupling. Their lower propagation delays and more accurate timing can provide a speed advantage over optocouplers. In Figure 3, a pulse transformer is used; it can operate at the speeds often needed for half-bridge gate-driver applications (up to 1 MHz). A gate-driver IC can be used to deliver the high currents needed for charging the capacitive MOSFET gates. Here, the gate driver differentially drives the primary of the pulse transformer; the two secondary windings drive each gate of a half bridge. In this application, pulse transformers have the advantage of not requiring isolated power supplies to drive the secondary side MOSFETs.

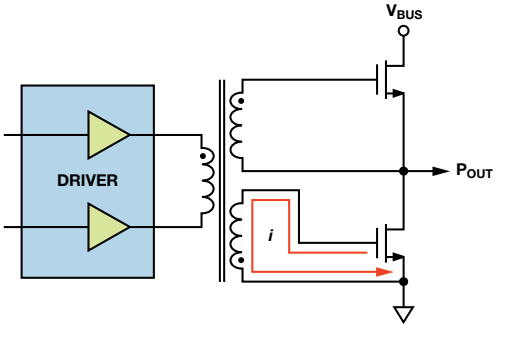

Figure 3. Pulse transformer half-bridge gate driver.

However, a problem can occur when large transient gate-drive currents flowing in the inductive coils cause ringing. This can switch the gate on and off when not intended, damaging the MOSFETs. Another limitation of pulse transformers is that they may not work well in applications that require signals with more than 50% duty cycle, as they can deliver only ac signals, and the core flux must be reset each half cycle to maintain a volt-second balance. A final difficulty: the magnetic core and isolated windings of the pulse transformer require a relatively large package which, combined with the driver IC and other discrete components, creates a solution that may be too large for many high-density applications.

Digital Isolator Gate Driver

Consider now applying a digital isolator in an isolated half-bridge gate driver. The digital isolator in Figure 4 uses a standard CMOS integrated-circuit process with metal layers to form transformer coils separated by polyimide insulation. This combination achieves more than 5 kV rms (1-minute rating) isolation, which can be used in robust isolated power supply and inverter applications.

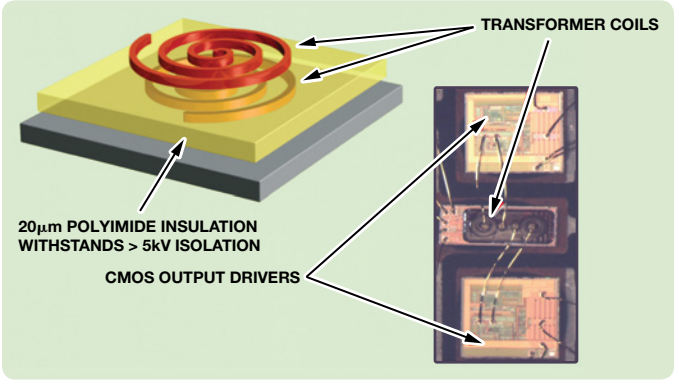

Figure 4. Digital isolator with transformer isolation.

As shown in Figure 5, the digital isolator eliminates the LED used in an optocoupler—and its associated aging problems—consumes far less power, and is more reliable. Galvanic isolation (dashed lines) is provided between input and output, and between the two outputs, eliminating high-side to low-side interactions. The output drivers feature a low output impedance to reduce the conduction losses—and a fast switching time to reduce the switching losses.

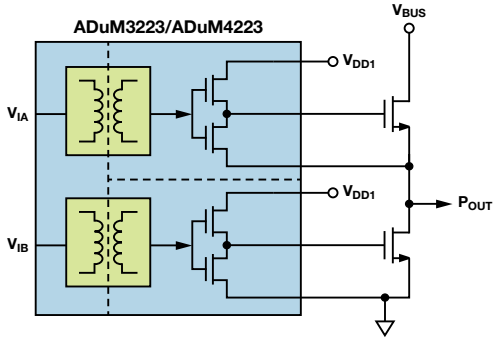

Figure 5. Digitally isolated 4-A gate driver.

Unlike an optocoupler design, the high- and low-side digital isolators are manufactured on a single integrated circuit, with inherently matched outputs for better efficiency. Note that the high-voltage gate driver integrated circuit shown in Figure 1 has additional propagation delay in the level-shifting circuit, so it cannot match channel-to-channel timing characteristics as well as the digital isolator. Furthermore, integration of the gate drivers with isolation in a single IC package reduces the footprint of the solution to a minimum.

Common-Mode Transient Immunity

In many half-bridge gate-driver applications for high-voltage power supplies, very fast transients can occur across the switching elements. In these applications, a rapidly changing voltage transient (high dV/dt) that capacitively couples across an isolation barrier can cause logic transition errors across the barrier. In an isolated half-bridge driver application, this could turn on both switches in a cross-conduction episode that could destroy the switches. Any parasitic capacitance across the isolation barrier tends to be a coupling path for common-mode transients.

Optocouplers need to have very sensitive receivers to detect the small amount of light transmitted across their isolation barrier, and their outputs can be upset by large common-mode transients. The optocoupler sensitivity to common-mode transient voltages can be reduced by the addition of a shield between the LED and the receiver; a technique used in most optocoupler gate drivers. The shield can improve the *common-mode transient immunity* (CMTI) from a standard optocoupler rating of less than 10 kV/μs to as much as 25 kV/μs for an optocoupler gate driver. This rating may be suitable for many gate-driver applications, but CMTI of 50 kV/μs or more may be needed for power supplies with large transient voltages, and for solar inverter applications.

Digital isolators can deliver higher signal levels to their receivers and withstand very high levels of common-mode transients without data errors. Transformer-based isolators, as four-terminal differential devices, can provide low differential impedance to the signal and high common-mode impedance to the noise—which can result in excellent CMTI. On the other hand, digital isolators that use capacitive coupling to create a changing electric field and transmit data across the isolation barrier are two-terminal devices, so the noise and the signal share the same transmission path. With a two-terminal device, the signal frequencies need to be well above the expected frequency of the noise so that the barrier capacitance presents low impedance to the signal and high impedance to the noise. When the common-mode noise level becomes large enough to overwhelm the signal, it can upset the data at the isolator output. An example of a capacitor-based isolator data upset is shown in Figure 6, where the output (Channel 4, green line) has glitched low for 6 ns during a common-mode transient of only 10 kV/μs.

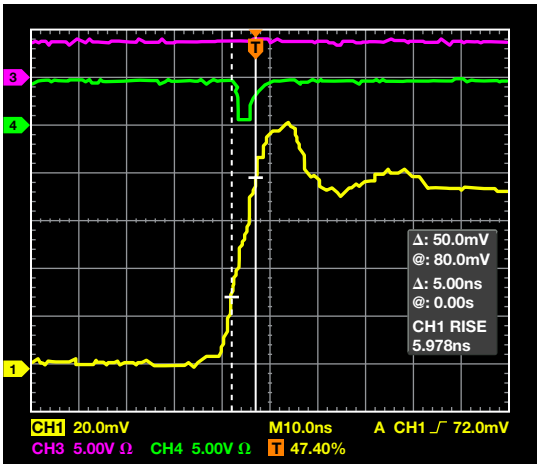

Figure 6. Capacitor-based digital isolator with CMTI of <10 kV/μs.

This data was taken merely at the *threshold* level of upsetting the capacitor-based isolator transient; a much larger transient could cause the upset to last for a much longer time, which could make the switching of the MOSFETs unstable. In contrast, transformer-based digital isolators have been shown to withstand common-mode transients in excess of 100 kV/μs without a data upset at the output (Figure 7).

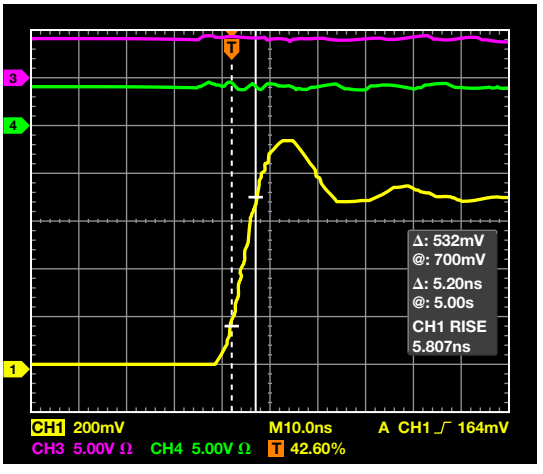

Figure 7. Transformer-based digital isolator with CMTI of 100 kV/μs (ADuM140x).

Isolated Half-Bridge Drivers Provide 4-A Peak Output Currents

The ADuM3223/ADuM4223 isolated half-bridge gate drivers, shown in Figure 8, use *i*Coupler® technology to provide independent, isolated outputs for driving the gates of the high-side and low-side IGBT and MOSFET devices used in motor control, switching power supplies, and industrial inverters. Combining high-speed CMOS with monolithic transformer technology, these isolation components provide precise timing, high reliability, and better overall performance than optocouplers or pulse transformers. Each output may be continuously operated up to 565 V_{PEAK} relative to the input, thereby supporting low-side switching to negative voltages. The differential voltage between the high side and low side may be as high as 700 V_{PEAK}. Switching at up to 1 MHz, the outputs can provide 4-A peak currents. The CMOS-compatible inputs provide 50-kV/μs common-mode transient immunity. The drivers operate with a 3.0-V to 5.5-V input supply, providing compatibility with lower voltage systems. Specified from –40°C to +125°C, they are available in 16-lead SOIC packages. Priced at $1.70 in 1000s, the ADuM3223 provides 3-kV rms isolation in a narrow body. Priced at $2.03 in 1000s, the ADuM4223 provides 5-kV rms isolation in a wide body.

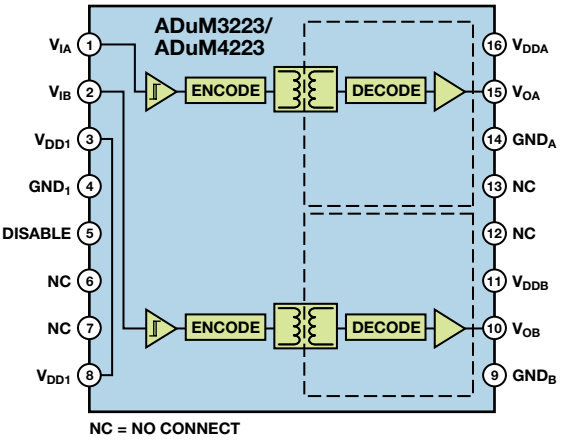

Figure 8. ADuM3223/ADuM4223 block diagram.

Summary

For isolated half-bridge gate-driver applications, the integrated transformer-based digital isolator has been shown to offer numerous advantages over optocoupler- and pulse-transformer-based designs. Size and design complexity are dramatically reduced through integration, greatly improving timing. Robustness is improved through galvanic isolation of the output drivers, and transformer coupling results in higher CMTI.

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Detecting and Distinguishing Cardiac Pacing Artifacts

John Kruse and Catherine Redmond

When heart patients with implanted pacemakers undergo electrocardiogram (ECG) testing, a cardiologist must be able to detect the presence and effects of the pacemaker. The electrical signature—or artifacts—of the pacing signal consists of small, narrow pulses. Buried in noise and larger cardiac signals, these artifacts can be difficult to detect. This article describes the nature of pacing artifacts and introduces a device and methodology to detect them.

The heart, a biochemical-electromechanical system, develops an electrical impulse that travels from the *sinoatrial* (SA) node in the upper right atrium to the *atrioventricular* (AV) node. The SA node acts as the pacemaker for the system (Figure 1).

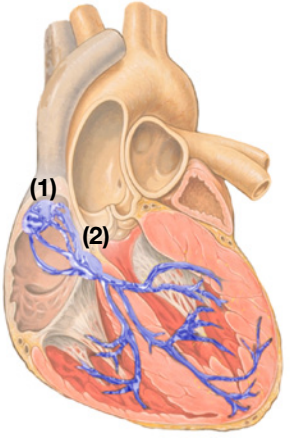

Figure 1. Heart muscle showing SA (1) and AV (2) nodes.[1]

This electrical impulse generates the P wave, which can be seen on the ECG capture in Figure 2. From the AV node, the electrical signal propagates, via the *His-Purkinje* system, to the ventricles, causing the ventricle muscles to contract. Their contraction (the *R* wave) moves oxygenated blood from the left ventricle into and through the body—and deoxygenated blood from the right ventricle to the lungs.

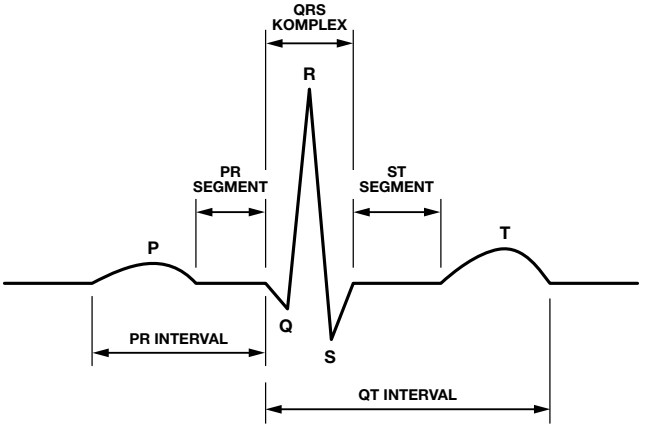

Figure 2. Graphical ECG representation of electrical action during heart muscle contractions.[2]

When the electrical system doesn't work perfectly, many different heart conditions can occur. For example, *bradycardia* occurs when the heart beats too slowly or misses beats. A typical surgical intervention for this condition would be to implant a *pacemaker* device (pulse generator) just under the skin of the patient's chest, with *endocardial* leads routed through the veins directly to the heart, as shown in Figure 3.

In another class of arrhythmias, called *tachycardia*, the heart beats too fast. This very serious condition is treated with *implantable cardiac defibrillators* (ICDs). Modern ICDs can also treat many bradycardia arrhythmias.

Heart failure can occur when the heart becomes enlarged, lengthening its conduction paths and upsetting the timing of the ventricular contractions. This forms a positive feedback system, further aggravating the heart. *Implantable cardiac resynchronization* (ICR) devices retime the ventricles by pacing both ventricles and usually one atrium. These devices actually improve cardiac output, allowing the heart to recover to a certain degree. *Cardiac resynchronization therapy* (CRT) devices include an ICD as part of the system.

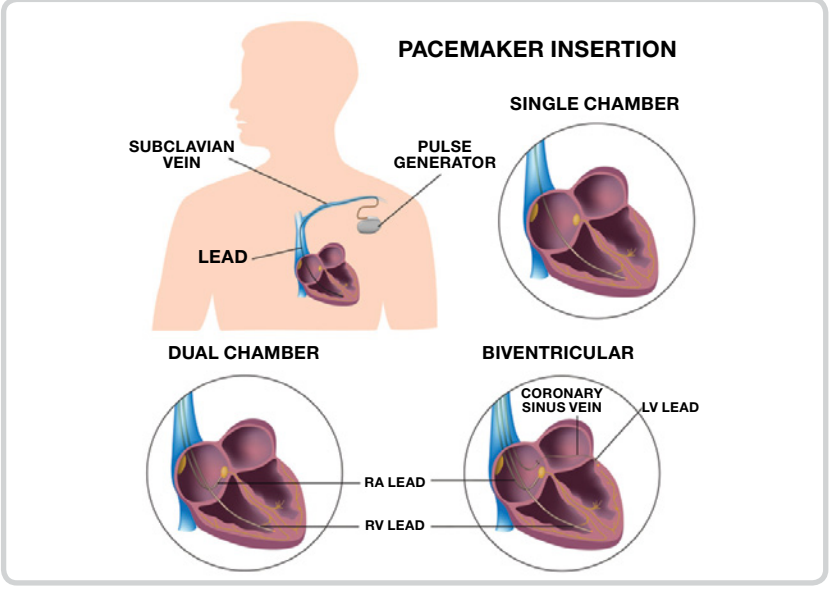

Figure 3. Positions of implanted pacemaker and leads for different types of pacemakers (RA—right atrium, RV—right ventricle, LV—left ventricle).

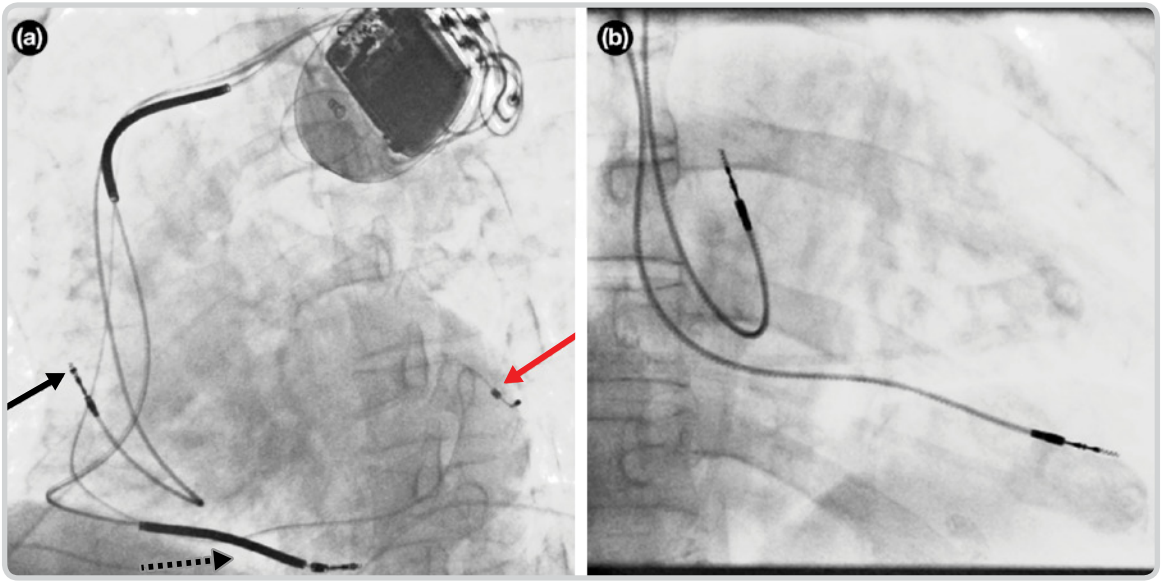

Figure 4. Fluoroscopy images showing pacemaker lead placement.[3]
(a). Single-chamber pacemaker. (b). Dual-chamber pacemaker.

A CRT device is seen in the fluoroscopic image of Figure 4(a). This is the image that physicians use to place the leads. Such images are difficult for lay persons to interpret. You can see a light outline of the heart—a static view of a beating heart. It is lying on the right atrium with the apex of the heart pointing to the right and downward. In this typical lead placement, the black arrow points to the right atrium lead. The dashed black arrow points to the right ventricle lead. The partially seen lead, indicated by the red arrow, is the left ventricle lead (the red arrow points to the tip of the electrode). Figure 4(b) shows a fluoroscopy image of typical lead placement for a dual-chamber pacemaker. The right atrium lead is pointing up and is placed in the right atrium. The right ventricle lead is positioned at the apex of the right ventricle.

Implantable pacemakers (Figure 5) are typically lightweight and compact. They contain the circuitry necessary to monitor the electrical activity of the heart through implanted leads and to stimulate the heart muscle when required to ensure a regular heartbeat. Pacemakers must be low-power devices, as they operate with a small battery that typically has a 10-year lifespan. As of 2010, the National Academy of Engineering states that over 400,000 pacemakers are implanted in patients every year.[4]

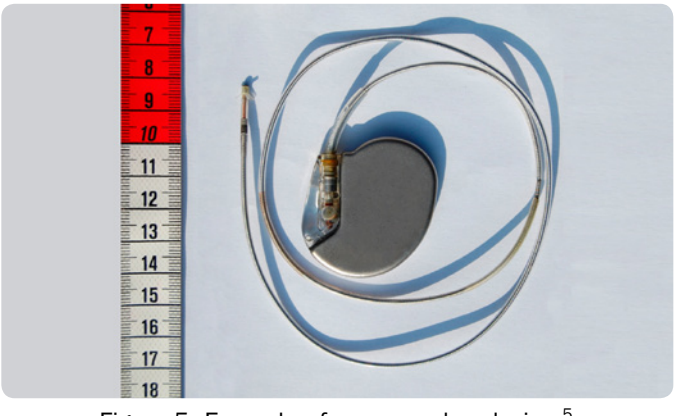

Figure 5. Example of a pacemaker device.[5]

Pacing Artifacts

A simple implanted pacer's activity is generally not perceptible on a normal ECG trace because the very fast pulses—with widths of microseconds—get filtered out, but in any case, they are too narrow to appear on a trace with resolution in the milliseconds. However, its signals can be inferred by pacing artifacts, voltage pulses that accompany the measurement of the heart's own electrical activity at the skin surface measured on ECG leads. It is important to be able to detect and identify pacing artifacts because they indicate the presence of the pacemaker—and help in evaluating its interaction with the heart.

Their small amplitude, narrow width, and varying wave shape make pacing artifacts very difficult to detect, especially in the presence of electrical noise that can be many times their amplitude. Furthermore, pacing therapy has become extremely advanced, with dozens of pacing modes available—from single-chamber pacing to three-chamber pacing. To further complicate the detection of pacing artifacts, pacemakers produce lead-integrity pulses, minute-ventilation (MV) pulses, telemetry signals, and other signals that can be incorrectly identified as pacing artifacts.

The use of real-time pacemaker telemetry has made the display of pacing artifacts on an ECG strip less important than it used to be, but an individual skilled in pacing therapies can look at the strip to infer the type of pacing therapy being administered to the patient and determine whether the pacemaker is working properly. In addition, all pertinent medical standards, including the following, require the display of pacing artifacts. They do vary somewhat in their specific requirements regarding the height and width of the pacer signal that needs to be captured.

- AAMI EC11:1991/(R)2001/(R)2007
- EC13:2002/(R)2007, IEC60601-1 ed. 3.0b, 2005
- IEC60601-2-25 ed. 1.0b
- IEC60601-2-27 ed. 2.0, 2005
- IEC60601-2-51 ed. 1.0, 2005

For example, IEC60601-2-27 states:

Equipment shall be capable of displaying the ECG signal in the presence of pacemaker pulses with amplitudes of ±2 mV to ±700 mV and durations of 0.5 ms to 2.0 ms. An indication of the pacemaker pulse shall be visible on the display with an amplitude of no less than 0.2 mV referred to input (RTI);

whereas, AAMI EC11 states:

The device shall have the capability of displaying the ECG signal in the presence of pacemaker pulses with amplitudes between 2 mV and 250 mV, durations between 0.1 ms and 2.0 ms, a rise time of less than 100 µs, and a frequency of 100 pulses/minute. For pacemaker pulses having durations between 0.5 ms and 2.0 ms (and amplitude, rise time, and frequency parameters as specified above), an indication of the pacemaker pulse shall be visible on the recording; this indication shall be visible on the display with an amplitude of at least 0.2 mV RTI.

These may be subtle differences, but they're differences nonetheless, in terms of the heights and widths to be captured.

How Pacemakers Pace

All pacing leads have two electrodes, with the location of the electrodes determining the *polarity* of the signal.

In *unipolar* pacing, the pacing leads consist of an electrode at the tip of a single pacing lead and the metal wall of the pacemaker housing (can) itself, so just one lead is inserted into the heart. The pacing artifacts caused by this mode of pacing can be several hundred millivolts at the skin surface with a width of a couple of milliseconds. Unipolar pacing is no longer commonly used.

In *bipolar* pacing, the heart is paced from the electrode at the tip of the pacing lead. The return electrode is a ring electrode located very close to the tip electrode. Most pacing artifacts are now created by bipolar pacing. The artifacts produced by this type of lead are much smaller than those produced by unipolar pacing; pulses on the skin surface can be as small as a few hundred microvolts high and 25 µs wide, with average artifacts 1 mV high and 500 µs wide. The amplitude of the artifact can be much smaller when the detection vector does not line up directly with the pacing lead vector.

Many pacemakers can be programmed for pulse widths as short as 25 µs, but these settings are typically used only in pacemaker threshold tests performed in an electrophysiology laboratory. Setting the lower limit to 100 µs eliminates the problem of falsely detecting *minute ventilation* (MV) and *lead integrity* (LV lead) pulses as valid pacing artifacts. These subthreshold pulses are usually programmed to be between 10 µs and 50 µs.

Various types of available pacemakers pace different chambers:

- *Single-chamber pacing* delivers pacing therapy to only one chamber of the heart; it can be either unipolar or bipolar. Single-chamber pacing is applied to the right atrium or the right ventricle.
- *Dual-chamber pacing* delivers pacing therapy to both the right atrium and the right ventricle.
- *Biventricular pacing* delivers pacing therapy to both the right ventricle and the left ventricle. In addition, the heart is usually paced in the right atrium. This mode of pacing can be very difficult to display properly for two main reasons: first, the two ventricle paces may occur at the same time, appearing as a single pulse at the skin surface. Second, the left ventricle lead placement is generally not on the same vector as the right ventricle lead and may actually be orthogonal to it. Usually, the right atrium is best displayed in Lead aVF, while the right ventricle is best displayed in Lead II. Most ECG systems do not employ three simultaneous lead-detection circuits or algorithms, making the left ventricle the toughest lead to pick up. Thus, it is sometimes best detected in one of the V leads.

Pacing Artifact Waveforms

Most pacing pulses have very fast rising edges. The rise time measured at the pacemaker output is generally about 100 ns. When measured at the skin surface, the rise time will be slightly slower because of the inductance and capacitance of the pacing lead. Most pacing artifacts at the skin surface are of the order of 10 µs or less. Complex devices with built-in protection, pacemakers can produce high-speed glitches that do not affect the heart but do affect pacemaker detection circuits.

Figure 6 shows an example of an ideal pacing artifact. The positive pulse has a fast rising edge. After the pulse reaches its maximum amplitude, a capacitive droop follows, and then the trailing edge occurs. The artifact then changes polarity for the recharge portion of the pacing pulse. This recharge pulse is required so that the heart tissue is left with a net-zero charge. With a monophasic pulse, ions would build up around the electrodes, creating a dc charge that could lead to necropsy of the heart tissue.

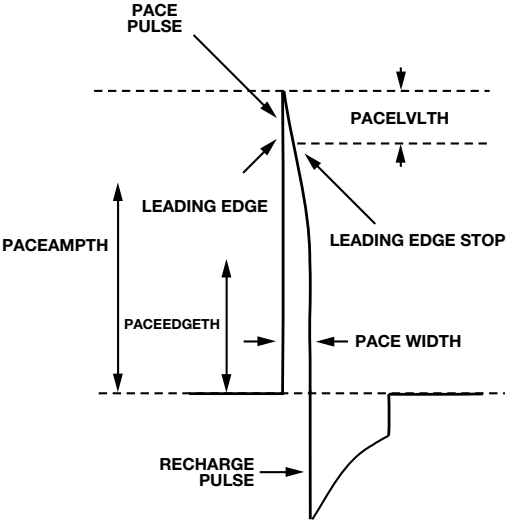

Figure 6. Ideal pacing artifact.

Introducing cardiac resynchronization devices adds another degree of complication in detecting and displaying pacing artifacts. These devices pace the patient in the right atrium and both ventricles. The pulses in the two ventricles can fall close together, overlap, or occur at exactly the same time; and the left ventricle can even be paced before the right ventricle. Currently, most devices pace both ventricles at the same time, but studies have shown that adjusting the timing will benefit most patients by yielding a higher cardiac output. Detecting and displaying both pulses separately is not always possible, and many times they will appear as a single pulse on the ECG electrodes. If both pulses occur at the same time, with the leads oriented in opposite directions, the pulses could actually cancel each other out on the skin surface. The probability of this occurring is very remote, but one can envision the appearance of two ventricle pacing artifacts on the skin surface with opposite polarities. If the two pulses were offset by a small time interval, the resulting pulse shape could be very complex.

Figure 7 shows scope traces of a cardiac resynchronization device pacing in a saline tank. This is a standard test environment for pacemaker validation; it is believed to be similar to the conductivity of the human body. The close proximity of the scope probes to the pacing leads causes the amplitudes to be much larger than what would be expected on the skin surface. In addition, the low impedance presented by the saline solution to the ECG electrodes results in much less noise than would normally be seen in a skin surface measurement.

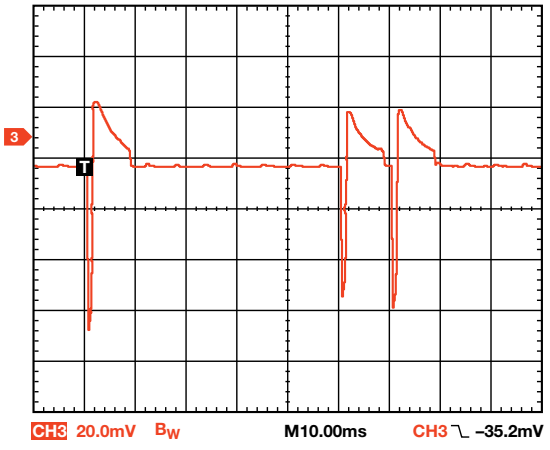

Figure 7. Pace signal capture from resynchronization device in saline tank.

The first pulse is the atrial, the second pulse is the right ventricle, and the third pulse is the left ventricle. The leads were placed in the saline tank with vectors optimized to see the pulses clearly. The negative-going pulse is the pace and the positive-going pulse is the recharge. The amplitude of the atrial pulse is slightly larger than the other two pulse amplitudes because the lead was in a slightly better vector than the ventricle leads, but in actuality, all three pacing outputs in the resynchronization device were programmed to have the same amplitude and width. With real patients, the amplitudes and widths are often different for each pacemaker lead.

Detecting Pacing Artifacts

With this understanding of the morphology and origin of the signals of interest, we can focus on the subject of detecting a pacing artifact. By their nature, it is impossible to detect all pacing artifacts and reject all possible noise sources in a cost-effective manner. Among the challenges are the number of chambers that pace detection must monitor, the interference signals encountered, and the variety of pacemakers from differing manufacturers. Solutions for detecting artifacts may range from hardware solutions to digital algorithms. These will all be discussed in more detail now.

The pacing leads for cardiac resynchronization devices will not all have the same vector. The right atrium lead usually aligns with Lead II, but it can sometimes point straight out of the chest, so a Vx vector may be needed to see it. The right ventricle lead is usually placed at the apex of the right ventricle, so it usually aligns well with Lead II. The left ventricle pacing lead, threaded through the coronary sinus, is actually on the outside of the left ventricle. This lead usually aligns with Lead II but may have a V-axis orientation. The pacing leads of *implantable* defibrillators and resynchronization devices are sometimes placed in areas of the heart that have not had an infarction. Placing them around infarcts is the main reason that this system uses three vectors and requires a high-performance pacing-artifact detection function.

One of the major noise sources is the H-field telemetry scheme used by most implantable heart devices. Other sources of noise include transthoracic impedance measurements for respiration, electric cautery, and conducted noises from other medical devices connected to the patient.

To further complicate the problem of acquiring pacing artifacts, each pacemaker manufacturer uses a different telemetry scheme. In some cases, a single manufacturer may use many different telemetry systems for different implantable device models. Many implantable devices can actually communicate using both H-field telemetry and either MICS- or ISM-band telemetry. The variability of H-field telemetry from one model to the next makes filter design very difficult. ECG devices have to be Class CF, but other medical devices may be Class B or BF, and their higher leakage currents may interfere with the performance of ECG acquisition devices.

ADAS1000 ECG Analog Front End Includes Pacing Artifact Detection Algorithm

The ADAS1000 (Figure 8) is a 5-channel electrocardiography (ECG) analog front end (AFE) designed to help address some of the challenges facing designers of next-generation low-power, low-noise, high-performance, tethered- and portable ECG systems. The ADAS1000, designed for both monitor- and diagnostic-quality ECG measurements, comprises five electrode inputs and a dedicated right-leg-drive (RLD) output reference electrode.

In addition to supporting the essential ECG signal-monitoring elements, the ADAS1000 is equipped with functions such as respiration measurement (thoracic impedance measurement), lead/electrode connection status, internal calibration, and capabilities for pace artifact detection—as discussed above.

One ADAS1000 supports five electrode inputs, facilitating a traditional 6-lead ECG measurement. By cascading a second ADAS1000-2 (companion) device, the system can be scaled up to a true 12-lead measurement; and by cascading multiple devices (three and above), the system can be scaled to measurements with 15 leads and beyond. See Table 1 for details on the different variants of the ADAS1000.

The respiration feature of the ADAS1000 provides the ability to measure thoracic impedance variations of the patient, indicating the extent, or absence, of breathing. At the heart of the respiration function is an integrated DAC (digital-to-analog converter) respiration drive at a programmable frequency (46 kHz to 64 kHz), and a dedicated analog-to-digital measuring circuit that simplifies this difficult measurement. The signal is demodulated and provided as magnitude and phase information, from which the corresponding respiration can be determined, given the specific cable parameters. The circuit is capable of detecting resolutions as small as 200 mΩ, using the internal capacitor—with even more-precise resolution, using an external capacitor—and has a flexible switching scheme, allowing measurement on one of three leads (I, II, III).

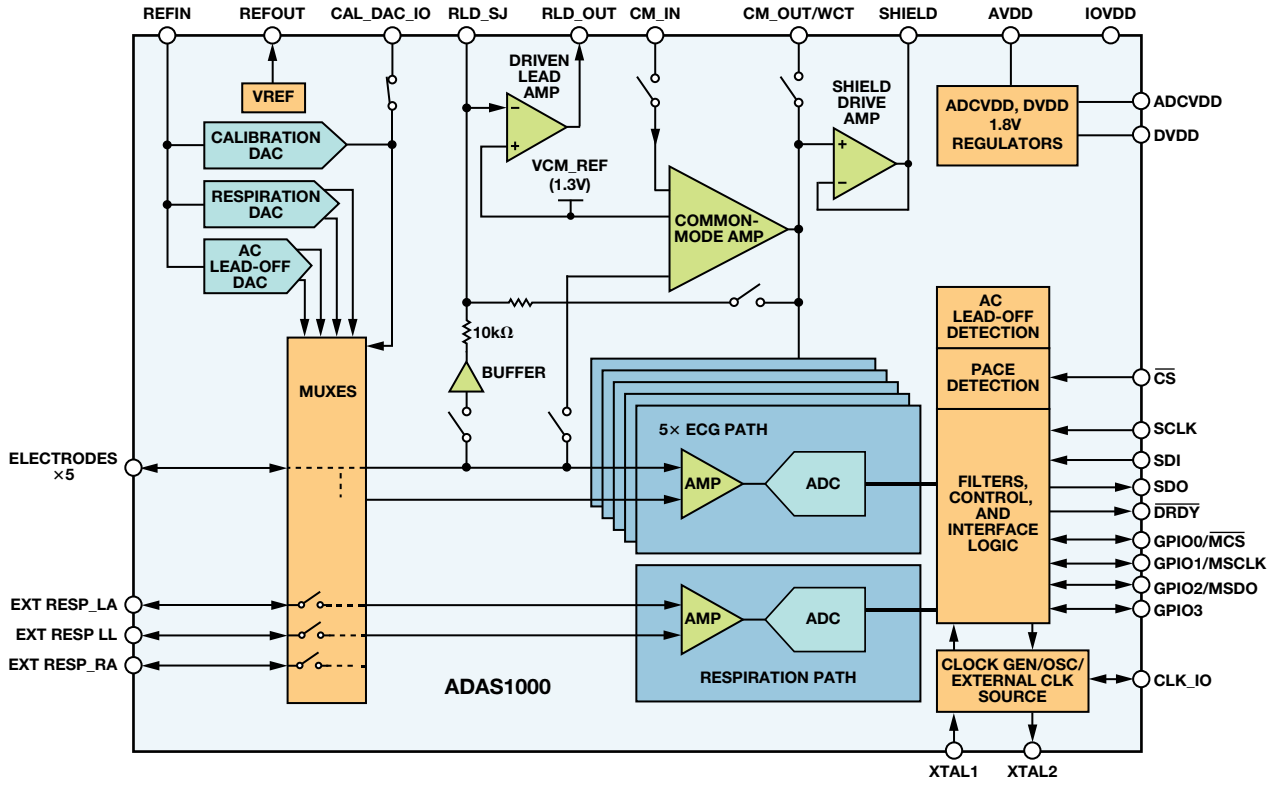

Figure 8. ADAS1000 block diagram.

Table 1. Overview of Available Models of the ADAS1000

Part Number	Number of Electrodes	Extra Features	Input Noise, 0.05 Hz to 150 Hz (μV p-p)	CM I/P Range (V)	Supply Voltage	Package Option
ADAS1000	5 ECG electrodes + RLD	Respiration, pace, and pace I/F	10	±1	3.3 to 5.5	56-lead LFCSP 64-lead LQFP
ADAS1000-1	5 ECG electrodes + RLD		10	±1	3.3 to 5.5	56-lead LFCSP
ADAS1000-2	5 ECG electrodes (companion for gang mode)		10	±1	3.3 to 5.5	56-lead LFCSP 64-lead LQFP
ADAS1000-3	3 ECG electrodes + RLD		10	±1	3.3 to 5.5	56-lead LFCSP 64-lead LQFP
ADAS1000-4	3 ECG electrodes + RLD	Respiration, pace, and pace I/F	10	±1	3.3 to 5.5	56-lead LFCSP 64-lead LQFP

Pace Detection Algorithm

The device's front end includes a digital pacemaker artifact-detection algorithm that detects pacing artifacts with widths that range from 100 μs to 2 ms, and amplitudes that range from 400 μV to 1000 mV—to align with the AAMI and IEC standards listed above. Based on testing and physician input, these limits are much more generous than the medical standards call for.

The pace-detection algorithm runs three instances of a digital algorithm on three of four possible leads (I, II, III, or aVF). It runs on the high-frequency ECG data, in parallel with the internal decimation and filtering. Designed to detect and measure pacing artifacts with widths ranging from 100 μs to 2 ms, and amplitudes of 400 μV to 1000 mV, it returns a flag that indicates pace was detected on one or more of the leads, and also the measured height and width of the detected signal. For users who wish to run their own digital pace algorithm, the ADAS1000 provides a high-speed pace interface that provides the ECG data at a fast data rate (128 kHz), while the filtered and decimated ECG data remains unchanged on the standard interface.

The ADAS1000 ECG IC has a minute-ventilation filter built into its algorithm. Minute-ventilation pulses, which are conducted from the ring of a bipolar lead to the can of the pacemaker, detect respiration rates to control the pacing rate. They're always less than 100 μs wide, varying from about 15 μs to 100 μs.

Many implantable devices are capable of being programmed for pacing pulses as narrow as 25 µs, but physicians almost never program implantable devices with pulses that narrow because there would not be enough of a safety margin of energy above the pacing threshold.

This pacing artifact system was developed by a team of engineers and pacing experts who worked in conjunction with the pacing industry. The result of this collaboration is a simultaneous three-vector pacing-artifact system that can detect pacing artifacts despite electrical noise that is significantly larger that the artifacts. Each of the three instances of the pace algorithm can be programmed to detect pace signals on different leads (I, II, II, or aVF). Programmable threshold levels allow it to be tailored to detect the range of pulse widths and heights presented, with internal digital filters designed to reject heartbeat, noise, and minute-ventilation pulses. When a pace has been validated in an individual instance of the pace signal, the device outputs a flag so that the user can mark or identify the pace signal in the ECG capture strip.

A simplified flowchart of the pacemaker algorithm is shown in Figure 9.

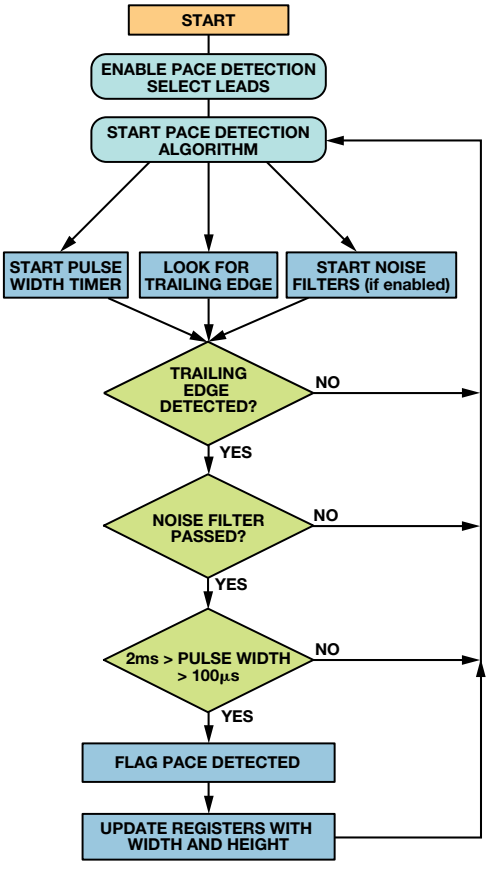

Figure 9. Flowchart of the pace algorithm.

The choice of sample rate for the pacing artifact algorithm is significant because it cannot be exactly the same frequency as those used by Medtronic, St. Jude, and Boston Scientific for the H-field telemetry carrier. All three corporations use different frequencies, and each has many different telemetry systems. Analog Devices believes that the sampling frequency employed by the ADAS1000 does not line up with any of the major telemetry systems of these three pacing companies.

As mentioned above, the ADAS1000 also includes respiration measurement and ac leads off. These features both inject ac signals at different frequencies onto the patient electrodes, but they don't interfere with the acquisition of pacing artifacts. Electric cautery signals can be filtered ahead of the ADAS1000 inputs for ECG, but performance of the pacing artifact detection algorithm may be degraded by the filtering, so care must be taken with its design.

Conclusion

Artifacts from implanted pacemakers can vary from 2 mV to 700 mV—with durations between 0.1 ms and 2 ms and rise times between 15 µs and 100 µs. Often swamped by telemetry noise or cardiac signals, they can be difficult to detect. The ADAS1000 analog front end for ECG systems includes all of the circuitry required to detect the electrical signals produced by a heart and its associated pacemaker—and an embedded algorithm that can help distinguish pacing artifacts and display them on the ECG strip chart.

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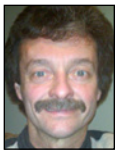
[3](a) http://en.wikipedia.org/wiki/File:Cardiac_resynchronisation_therapy.png.

(b) http://en.wikipedia.org/wiki/File:Fluoroscopy_pacemaker_leads_right_atrium_ventricle.png.

[4]http://www.nae.edu/page20019090/WhatisaPacemaker.aspx.

[5]http://en.wikipedia.org/wiki/File:St_Jude_Medical_pacemaker_with_ruler.jpg.

Authors



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Catherine Redmond [catherine.redmond@analog.com] is an applications engineer at Analog Devices in Limerick, Ireland. Since joining ADI in 2005, she has accumulated a wealth of experience in the industrial market arena through time spent supporting precision DACs as applied in automatic test equipment, and she now has a focus on precision ADC products, including applications responsibility for the ADAS1000 ECG front end. She graduated from Cork Institute of Technology with a bachelor's degree in electronic engineering and has since worked in an applications role within Analog Devices.

Versatile, Low-Power, Precision Single-Ended-to-Differential Converter

By Sandro Herrera and Moshe Gerstenhaber

Many applications, including driving modern analog-to-digital converters (ADCs), transmitting signals over twisted-pair cables, and conditioning high-fidelity audio signals, require differential signaling, which achieves higher signal-to-noise ratios due to the use of larger signals for a given set of power supply voltages, increased common-mode noise immunity, and lower second-harmonic distortion. This requirement presents a need for a circuit block that can convert single-ended signals, found in most signal chains, to differential signals.

Figure 1 shows a simple single-ended-to-differential converter using an AD8476 precision, low power, fully differential amplifier (diff-amp) with integrated precision resistors. The diff-amp is internally configured for a differential gain of one, so the circuit's transfer function is

$$V_{OUT,\,DIFF} = V_{OP} - V_{ON} = V_{IN}.$$

The output common-mode voltage, $(V_{OP} + V_{ON})/2$, is set by the voltage on the V_{OCM} pin. If the V_{OCM} pin is allowed to float, the output common-mode voltage will float to midsupply due to internal 1-MΩ resistors that form a resistance divider with the power supplies. Capacitor C1 filters the noise of the 1-MΩ resistors to lower the output common-mode noise. The circuit's gain error is only 0.04% maximum due to the AD8476's internal laser-trimmed gain-setting resistors.

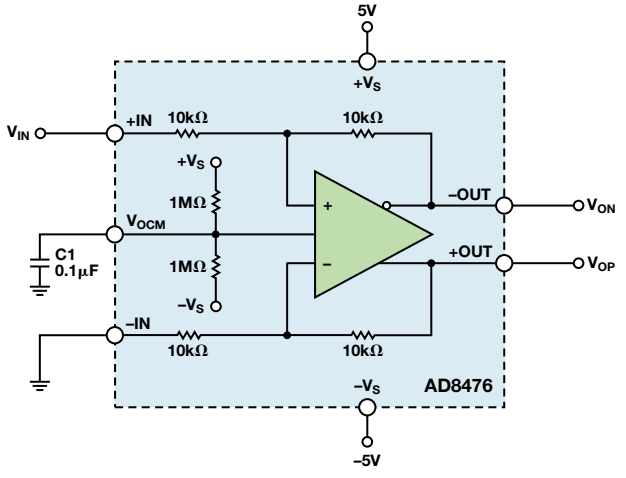

Figure 1. Simple single-ended-to-differential converter.

For many applications, the circuit in Figure 1 is more than adequate to perform the single-ended-to-differential conversion. For applications that require improved performance, Figure 2 shows a single-ended-to-differential converter that has very high input impedance, 2-nA maximum input bias current, 60-µV maximum offset (RTI), and 0.7-µV/°C maximum offset drift. The circuit achieves this level of performance by cascading an OP1177 precision operational amplifier (op amp) with the AD8476 and feeding back the positive output voltage of the AD8476 to the inverting input of the op amp. This feedback arrangement allows the op amp to determine the precision and noise performance of the configuration since it connects the diff-amp inside a feedback loop with an op amp's large open-loop gain preceding it. As a result, the errors of the AD8476—including noise, distortion, offset, and offset drift—are reduced by this large gain when referred to the input.

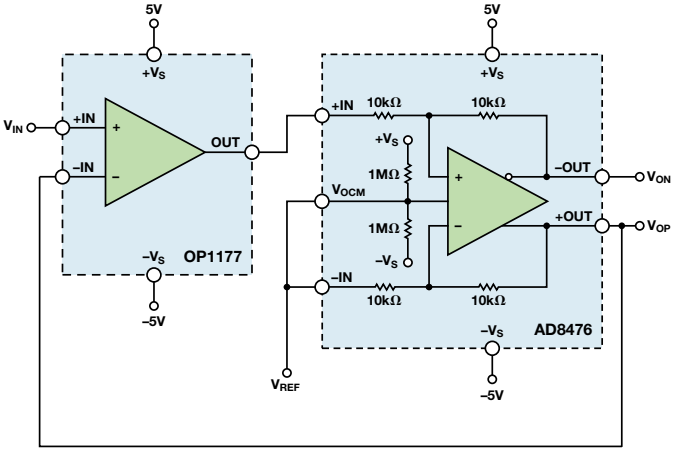

Figure 2. Improved single-ended-to-differential converter.

The circuit in Figure 2 is described by the following equations:

$$V_{OP} \approx V_{IN} \tag{1}$$

$$(V_{OP} + V_{ON}) = 2\,V_{OCM} = 2\,V_{REF} \tag{2}$$

$$V_{ON} = 2\,V_{REF} - V_{IN} \tag{3}$$

Combining (1) and (3),

$$V_{OUT,\,DIFF} = V_{OP} - V_{ON} = 2(V_{IN} - V_{REF}) \tag{4}$$

Equation 3 demonstrates two important properties about the circuit: first, the circuit's single-ended-to-differential gain is two. Second, the V_{REF} node serves as the reference for the input signal, so it can be used to null out an offset in the input signal. For example, if the input signal has a 1-V offset, applying 1-V to the V_{REF} node nulls it out.

If the intended application requires a gain greater than two, the circuit in Figure 2 can be modified, as shown in Figure 3. In this case, the single-ended-to-differential gain of the circuit is dictated by external resistors, R_F and R_G, such that:

$$Gain = \frac{V_{OUT,\,DIFF}}{V_{IN}} = 2\left(1 + \frac{R_F}{R_G}\right) \tag{5}$$

and

$$V_{OUT,\,DIFF} = V_{OP} - V_{ON} = 2\left(\left(1 + \frac{R_F}{R_G}\right)V_{IN} - V_{REF}\right) \tag{6}$$

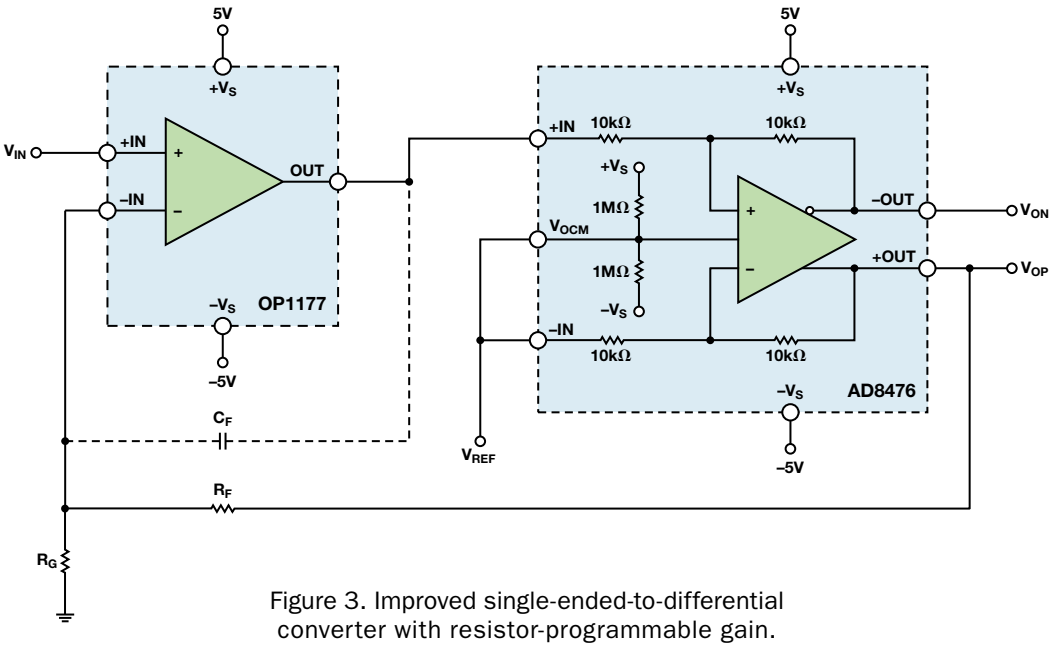

Figure 3. Improved single-ended-to-differential converter with resistor-programmable gain.

Like the circuit in Figure 2, this improved single-ended-to-differential converter rejects the errors of the diff-amp by placing it inside the op amp's feedback loop. As with any feedback connection, care must be taken to make sure the system is stable. Referring to Figure 2, the cascade of the OP1177 and the AD8476 form a composite differential-out op amp where the open-loop gain over frequency is the product of the op amp's open-loop gain and the diff-amp's closed-loop gain. Therefore, the closed-loop bandwidth of the AD8476 adds a pole to the open-loop gain of the OP1177. To ensure stability, the bandwidth of the diff-amp should be higher than the unity-gain frequency of the op amp. This requirement is relaxed in the circuit of Figure 3, as the resistive feedback network effectively reduces the unity-gain frequency of the OP1177 by a factor of $R_G/(R_G + R_F)$. Since the AD8476 has a bandwidth of 5 MHz and the OP1177 has a unity-gain frequency of 1 MHz, the circuits shown do not exhibit stability issues. Figure 4 shows an oscilloscope photo of the input and output signals of the circuit in Figure 2 when driven with a ground-referenced 10-Hz, 1-V p-p sinusoid. For simplicity, the V_{REF} node was tied to ground.

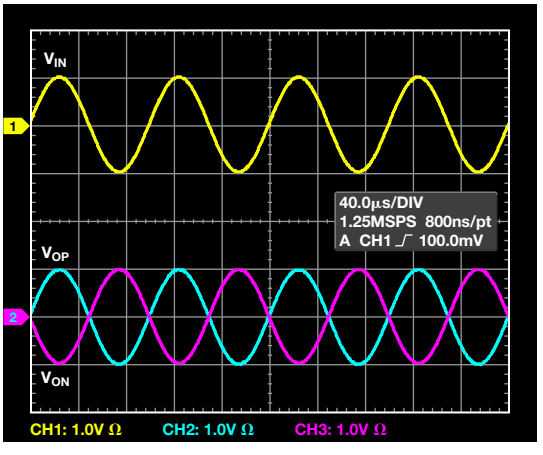

Figure 4. Input and output signals of the circuit in Figure 2 when driven with a ground-referenced 10-kHz, 1-V p-p sinusoid.

When using an op amp where the unity gain frequency is much larger than the diff-amp's bandwidth, a bandwidth-limiting capacitor, C_F, can be inserted, as shown in Figure 3. Capacitor C_F forms an integrator with the feedback resistor, R_F, such that the bandwidth of the overall circuit is given by

$$BW = \frac{1}{2}\,\frac{1}{2\pi R_F C_F} \qquad (7)$$

The ½ in the bandwidth equation is due to the feedback being single-ended rather than differential, which reduces the feedback and bandwidth by a factor of 2. If this reduced bandwidth is lower than the closed-loop bandwidth of the diff-amp, the circuit will be stable. This bandwidth-limiting technique can also be employed with a gain of two by making R_G an open circuit.

Authors

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HART Communication Networks Are Improved by Small, Flexible, Low-Power Modem ICs

By Tracey Johnson

The need to measure, control, and communicate with machinery and equipment has existed since the earliest days of the Industrial Revolution, with instrumentation systems employing sensors and actuators becoming the backbone of the modern manufacturing plant. Communication employing 4-mA-to-20-mA analog current signals to carry data and settings over wires has long been in widespread use. But instrumentation has matured from those purely analog systems to the "smart" systems used today, augmenting communications capability by the likes of the HART® *(highway addressable remote transducer)* protocol. Simply put, dc and low-frequency current signals are modulated by independent, higher-frequency signals that switch between a pair of frequencies (Figure 1)—a technique known as frequency-shift keying (FSK).

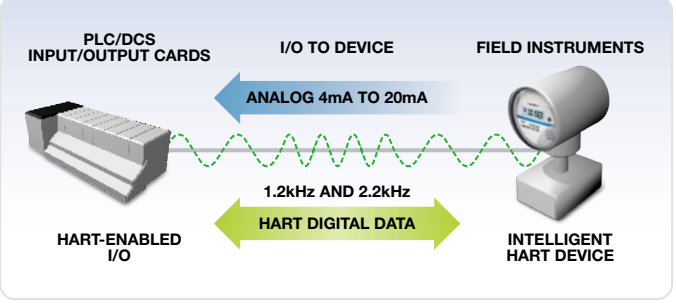


Figure 1. HART communication.

This article describes the technology's implementation, provides some application examples, discusses some of the devices employed by modern silicon integrated-circuit technology to aid the system designer, and—to illustrate the technology—introduces today's most compact, lowest power, and widest supply-voltage, fully compliant HART *modem* (modulate-demodulate) IC—the Analog Devices AD5700.

What Is HART Communication?

The primary form of communication used in analog transmitters is a current loop with a normal range of 4 mA to 20 mA, employing a transmitter, a receiver, and a power supply. It enables features such as remote calibration, fault interrogation, and transmission of process variable data. Low-power transmitters and receivers must operate on the minimum current, 4 mA or less, depending upon the "headroom" required for error indication. These current loops are reliable, robust, and highly immune to environmental interference over long communication distances. A significant disadvantage, however, is that a single loop allows only one-way communication *from* a sensor, or *to* an actuator, and can only transmit one process variable.

The introduction of the HART standard provided a means to create "smart" transmitters, by adding digital communication capability, sharing the same twisted-pair line used for traditional 4-mA-to-20-mA instrumentation. A 4-mA-to-20-mA analog current is modulated by a 1-mA peak-to-peak FSK signal—without interrupting the original primary variable transmission—while still leaving headroom for operating the loop. The HART protocol has become the global standard for sending and receiving digital information over analog wires between smart devices and a control or monitoring system.

Inside a HART Modem IC

The AD5700-1 complete HART modem IC (Figure 2) integrates all the necessary filtering, signal detection, modulation, demodulation, and signal generation needed—substantially reducing the number of external components required. Housed in a small 4-mm × 4-mm, 24-lead LFCSP package, it requires only a single 2-V to 5.5-V supply and operates over the –40°C to +125°C extended temperature range.

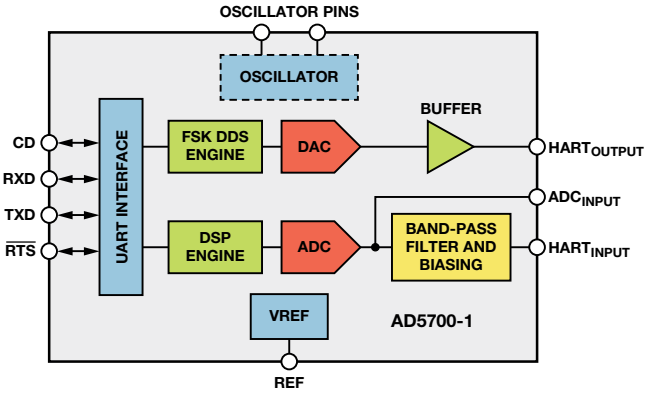


Figure 2. Block diagram of the AD5700-1; the -1 option includes an internal 0.5% precision RC oscillator.

Transmit Path

Figure 2 shows the main blocks involved in the modulation: the FSK *direct digital synthesis* (DDS) engine, the DAC (switched resistor string type), and the buffer. The digital data to be transmitted arrives via the UART. The modulator is enabled by bringing the $\overline{\text{RTS}}$ *(request to send)* signal low. The modulator converts a bit stream of UART-encoded HART data at the TXD input, to a binary sequence of 1200 Hz ("1") and 2200 Hz ("0") tones (Figure 3). The DDS produces a stream of sinusoidal digital words at either frequency, and the DAC converts it to an approximately 493-mV p-p analog sine wave. This sinusoidal signal is internally buffered and appears at the HART_OUT pin. The DDS engine inherently generates *continuous phase signals*, thus avoiding any output discontinuity when switching between frequencies. A key benefit of the internal buffering on HART_OUT is the resulting high drive capability, eliminating the need for external analog buffers and the issues they imply. The HART_OUT pin, dc biased to 0.75 V, should be capacitively coupled to the load. See the AD5700/AD5700-1 data sheet for more detailed information.

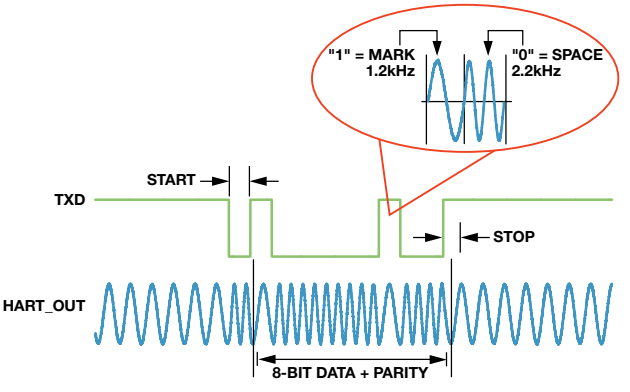


Figure 3. AD5700/AD5700-1 modulator waveform.

Receive Path

When $\overline{RTS}$ is logic high, the modulator is disabled and the demodulator is enabled, that is, the modem is in receive mode. The receiver demodulates the FSK modulated signal on the HART_IN pin. In this mode, the relevant blocks are the internal band-pass filter, the ADC, and the DSP engine. A high on CD (carrier detect) indicates that a valid carrier is detected. The demodulated data is sent to the host processor via the RXD pin on the UART interface.

The receive architecture was chosen to make the AD5700 robust against noise and interferers in harsh industrial environments. A combination of analog and digital filtering results in excellent sensitivity and a highly accurate output on the RXD pin. The HART bit stream follows a standard UART frame with a start bit, 8-bit data, one parity bit, and a stop bit. In demodulation mode, the modem has two filter configuration options: an internal filter (HART signal is applied to HART_IN) and an external filter (filtered HART signal is applied directly to ADC_IP). The external filter mode supports the use of the AD5700 in explosion-proof and intrinsically safe environments. Included is a 150-kΩ resistor, which limits current to a sufficiently low level to comply with intrinsic safety requirements. This option is recommended for operation in safety-critical applications, where the modem must be isolated from the high voltage of the loop supply. In this case, the input has higher transient voltage protection and should, therefore, not require additional protection circuitry, even in the most demanding of industrial environments.

Additional Blocks

The three remaining blocks shown in Figure 2 are the previously mentioned UART interface, the internal reference, and the oscillator. $\overline{RTS}$ and TXD are the important signals for modulation, while CD and RXD are important for demodulation. The AD5700 can accept an external 2.5-V reference, which can only be used if the AVDD supply is greater than 2.7 V. The use of the internal or external reference option is controlled by the polarity of the REF_SEL pin. For clocking, the device supports numerous schemes to allow a simple low-cost configurable solution. The AD5700 can use an external crystal, ceramic resonator, or CMOS input. The AD5700-1 is the first HART modem IC to incorporate an internal, low-power, 0.5% accurate oscillator, reducing the required external circuitry as well as overall cost. The many functions integrated on-chip greatly simplify the design of HART-compatible systems, resulting in more reliable, cost-effective, and robust networked solutions.

Low-Power Application Example

Low power is important because all circuitry powered by the loop must consume less than 3.5 mA. An example of the application of HART communication within a loop is shown in Figure 4. An AD5700 HART modem is interfaced with an AD5421 16-bit, serial-input, loop-powered, 4-mA-to-20-mA DAC and the ADuCM360 microcontroller, on an AD5700 evaluation board, to demonstrate a loop-powered transmitter circuit for two shared data channels measuring pressure (“0”) and temperature (“1”).

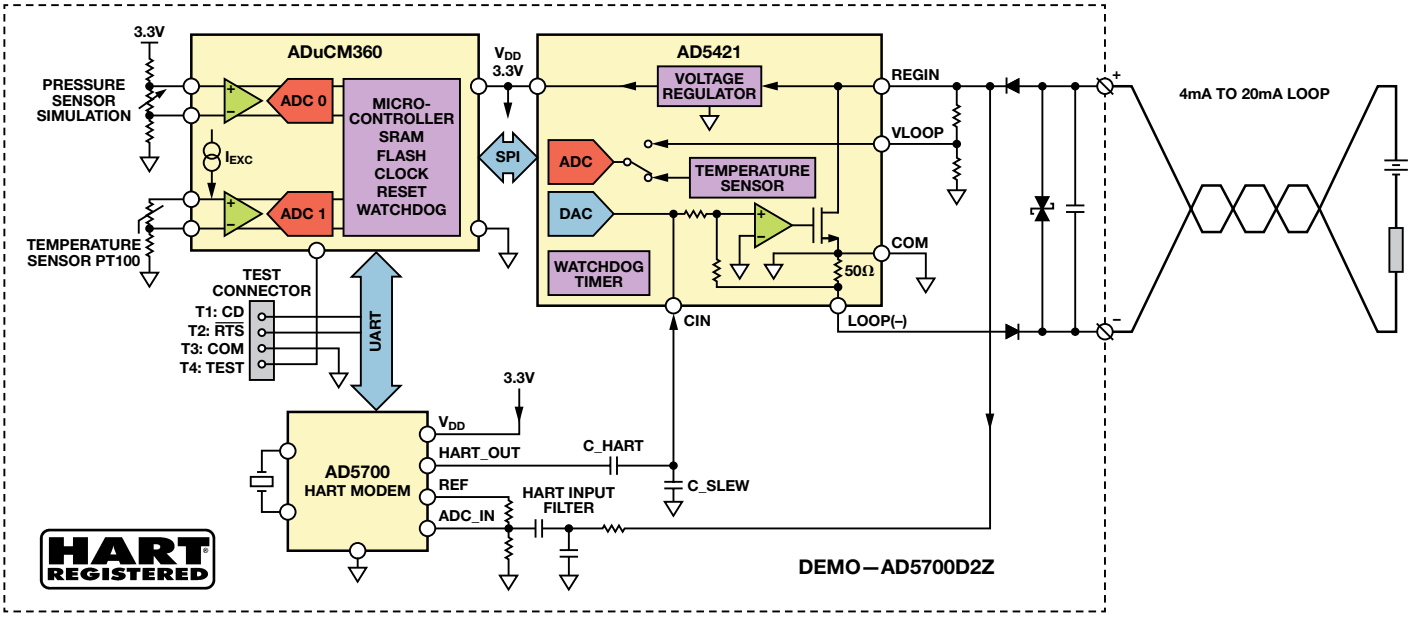


Figure 4. AD5421 loop DAC and AD5700 HART modem as a loop-powered data transmitter with HART communication.

This circuit has been compliance tested, verified, and registered as an approved HART solution by the HART Communication Foundation. The details of the product registration are available on their website.

The most important constraint in such 4-mA-to-20-mA loop-powered applications is that the entire circuit must draw less than 3.5 mA (the "low alarm" setting, 0.5 mA below the 4-mA signal floor). This is where the low power specification of the AD5700 becomes most important. Here, every microamp counts, so if each IC in the design can individually draw a small enough current, the 3.5-mA budget will not be surpassed, and the application will function as required. With typical transmit and receive currents of 124 µA and 86 µA, respectively, and corresponding maximum specified current drain of 140 µA and 115 µA, respectively, the AD5700 will not contribute significantly to the overall current budget.

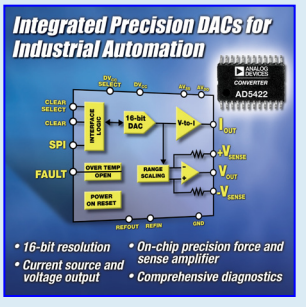
Conclusion

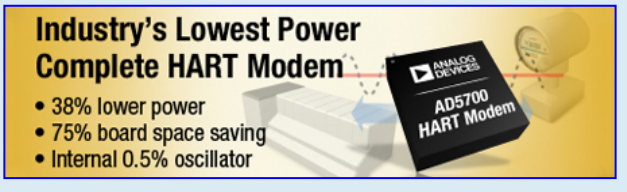
Besides the industry's lowest power HART modem IC, Analog Devices also offers complete HART solution capability, including microcontroller products, amplifiers, precision references, switches, ADCs, and current-output DACs. The AD5700 HART modem has been designed to interface easily with: the AD5421, which was used above in the loop-powered smart transmitter application example; the AD5422 16-bit voltage- and current-output DAC, useful for field instruments or analog I/O cards; and the AD5755-1 16-bit, quad DAC with innovative dynamic power control technology, for multichannel applications. In addition, components designed to mate easily together are available for the entire signal chain. When combined with the AD5700/AD5700-1, system design is simplified, reliability is enhanced, and quick, easy deployment of robust HART-compliant systems is enabled.

Author

Tracey Johnson [tracey.johnson@analog.com], an applications engineer in the Precision Digital-to-Analog Converter Group, is principally focused on industrial converters for process-control applications—including HART-enabled smart transmitters. In 2003, Tracey graduated from the University of Limerick, Ireland, with a bachelor's degree in electronic engineering. She joined Analog Devices as a design evaluation engineer in the DAC Group and has served in that role for seven years.

The AD5700 single-chip HART modem is registered with the HART Communication Foundation as part of a smart field instrument demo solution. It makes possible the industry's lowest power, complete HART modem that is fully compliant with the HART communication protocol, accurately encoding and decoding HART communication signals in noisy, harsh industrial environments and ensuring a reliable communication interface that is quick and easy to implement and register with the HART Communication Foundation. It requires 60% fewer external support components than alternative solutions and can provide greater than 75% saving in board area.





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