

Analog Dialogue

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IN THIS ISSUE

Robust Amplifiers Provide Integrated Overvoltage Protection

Faulty performance or damage can occur when an op amp's input voltage exceeds the specified input-voltage range. This article discusses some common causes and effects of *overvoltage conditions*, how cumbersome overvoltage protection can be added to an unprotected amplifier, and how the *integrated overvoltage protection* of newer amplifiers provides a compact, robust, cost-effective solution. Page 3.

Modern DACs and DAC Buffers Improve System Performance, Simplify Design

As the heart of many instrumentation and control systems, digital-to-analog converters (DACs) play a key role in determining system performance and accuracy. This article looks at a new precision, fast-settling, voltage-output 16-bit DAC and shows some ideas for buffering the outputs of high-speed complementary current-output DACs that can rival transformer performance. Page 7.

DDS Devices Generate High-Quality Waveforms Simply, Efficiently, and Flexibly

Direct digital synthesis (DDS) technology is used to generate and modify high-quality waveforms in a broad range of applications in such diverse fields as communications, defense, medicine, industry, and instrumentation. This article provides an overview of the technology, describes its strengths and limitations, looks at some application examples, and showcases some significant new products. Page 12.

Efficient FSK/PSK Modulator Uses Multichannel DDS to Switch at Zero Crossings

This article describes how two synchronized DDS channels can implement a zero-crossing FSK or PSK modulator. In phase-coherent radar systems, zero-crossing switching reduces the amount of postprocessing needed for target signature recognition; and zero-crossing switching reduces PSK spectral splatter. Here, the AD9958 two-channel complete DDS is used to switch at the zero crossing. Page 17.

Low-Noise, Gain-Selectable Amplifier

Traditional gain-selectable amplifiers use switches in the feedback loop to connect resistors to an amplifier, but the switch resistance degrades the noise performance of the amplifier, adds significant capacitance on the inverting input, and contributes to nonlinear gain error. This article presents a gain-selectable amp that uses an innovative switching technique that preserves the noise performance while reducing the nonlinear gain error. Page 20.

Designing a Low-Power Toxic Gas Detector

Safety first! Many industrial processes involve toxic compounds, including chlorine, phosphine, arsine, and hydrogen cyanide, so it is important to know when dangerous concentrations exist. This article describes a portable carbon monoxide detector using an electrochemical sensor. CO is relatively safe to handle, but it is still lethal, so use extreme care and appropriate ventilation when testing the circuit described here. Page 21.

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PRODUCT INTRODUCTIONS: VOLUME 46, NUMBER 1

Data sheets for all ADI products can be found by entering the part number in the search box at www.analog.com.

January

Amplifier, power, 2-W stereo, Class-D,
digital input SSM2518
DAC, 16-bit, ultra-stable, voltage-output AD5760
DAC, 18-bit, system-ready, voltage-output AD5780
DAC, 20-bit, system-ready, voltage-output AD5790
Transmitter, HDMI, 165-MHz,
high-performance ADV7513

February

Processor, video, 10-bit, multiformat,
SDTV/HDTV ADV7181D
Switch, analog crosspoint, 60-MHz,
16 × 16, G = 2 ADV3205
Transceivers, M-LVDS, 200-Mbps
half-/full-duplex ADN4696E/ADN4697E

March

ADCs, 16-bit, low-power, successive-
approximation AD7988-1/AD7988-5
Amplifier, difference, dual, short-to-battery
protection ADA4830-2
Amplifier, operational, dual, high-precision,
JFET-input ADA4610-2
Amplifier, operational, dual, low-noise,
JFET-input ADA4001-2
Comparator, fast, low-power, automotive AD8469
Controller, power supply, 3-channel, digital ADP1053
DAC, RF, 11-bit, 2.5-GSPS, current-output, AD9737A
Demodulator, quadrature, 50-MHz to 525-MHz,
PLL, VCO ADRF6806
Micro-PMU, 1.2-A buck, two
300-mA LDOs ADP5040
Micro-PMU, 1.2-A buck, two 300-mA
LDOs, watchdog ADP5041
Regulator, dc-to-dc, high-efficiency,
step-down, 4 A ADP2164
Sensor, temperature, 16-bit,
automotive, +175°C ADT7312

Analog Dialogue

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Robust Amplifiers Provide Integrated Overvoltage Protection

By Eric Modica and Michael Arkin

Faulty performance, or even damage, can occur when an op amp's input voltage exceeds the specified input-voltage range, or—in extreme cases—the amplifier's supply voltage. This article discusses some common causes and effects of *overvoltage conditions*, how cumbersome *overvoltage protection* can be added to an unprotected amplifier, and how the *integrated overvoltage protection* of newer amplifiers provides designers with a compact, robust, transparent, cost-effective solution.

All electronic components have upper limits to the applied voltages they can tolerate. When any of these upper limits are exceeded, the effects can range from momentary interruption of operation to system latch-up to permanent damage. The amount of overvoltage a given component can tolerate depends on several factors, including whether the part is installed or incidentally contacted, the amplitude and duration of the overvoltage event, and the robustness of the device.

Precision amplifiers, often the first component in sensor measurement signal chains, are the most exposed to overvoltage faults. When selecting a precision amplifier, system designers must be aware of the *common-mode input range* of the amplifier. On the data sheet, the common-mode input range may be specified by the *input voltage range* (IVR), or in the test conditions for the *common-mode rejection ratio* (CMRR), or both.

Real World Causes of Overvoltage Conditions

Amplifiers require: *overvoltage* protection to protect against faults caused by power-supply sequencing, sleep-mode switching, and voltage spikes; and *ESD* protection to protect against faults caused by *electrostatic discharge* (ESD), even during handling. When *installed*, the device can be subjected to system power sequence conditions, which cause repetitive overvoltage stress. System designers seek methods of routing the fault currents away from sensitive components, or limiting those fault currents enough to avoid damage.

In complex *distributed power architecture* (DPA) systems with multiple supply voltages, power-supply sequencing allows the supplies powering various portions of the system circuitry to turn on and off at different times. Improper sequencing can cause overvoltage and latch-up conditions to occur on any pin on any device.

With an increasing focus on energy efficiency, many systems implement complex *sleep* and *standby* modes. This means that some sections of a system may be powered down while others may remain powered and active. As with supply sequencing, these situations can cause unpredictable overvoltage events, but primarily on input pins.

Many types of sensors can generate unexpected output spikes that are unrelated to the physical phenomena they are meant to measure. This type of overvoltage condition generally affects only input pins.

Electrostatic discharge is a well-known overvoltage event that often occurs before the component is installed. The damage it can cause is so prevalent that industry-driven specifications, such as [JESD22-A114D](#), determine how to test and specify the

semiconductor's ability to withstand various types of ESD events. Almost all semiconductor products incorporate some form of integrated protection devices. The AN-397 Application Note, "[Electrically Induced Damage to Standard Linear Integrated Circuits: The Most Common Causes and the Associated Fixes to Prevent Recurrence](#)," is a good reference that covers this topic in detail. ESD cells are designed to go into a low-impedance state after a high-energy pulse. This does not limit the input current, but it does provide a low-impedance path to the supply rails.

A Simple Case Study: Power-Supply Sequencing

As mixed-signal circuits become ubiquitous, so too does the need for multiple supplies on a single PCB. See the AN-932 Application Note, "[Power Supply Sequencing](#)," for a look at some subtle issues to consider in new designs, especially when several unrelated power supplies are required.

Precision amplifiers can fall victim to this condition. Figure 1 shows an op amp configured as a differential amplifier. The amplifier senses the current through R_{SENSE} and provides an output proportional to the resultant voltage drop. Care must be taken that the divider formed by R_3 and R_4 biases the inputs somewhere within the specified IVR. If the amplifier's supply voltage is not derived from V_{SY} , and V_{CC} comes up after V_{SY} , the voltage at the inverting input of A1 will be:

$$V_- = V_{SY} - (I_- \times R_1) \quad (1)$$

where I_- depends on the input impedance of A1 with no supply. If the amplifier is not designed to handle overvoltage conditions, the most likely current path will be through an ESD diode, clamp diode, or parasitic diode to the power supply or ground. Damage can occur if this voltage falls outside of the IVR or if the current exceeds the data sheet maximum rating.

The ESD structures used on overvoltage-protected amplifiers, such as the [ADA4091](#) and [ADA4096](#), are not diodes, but **DIAC** (bidirectional "diode for alternating current") devices, making these amplifiers tolerant of overvoltage conditions, even without power.

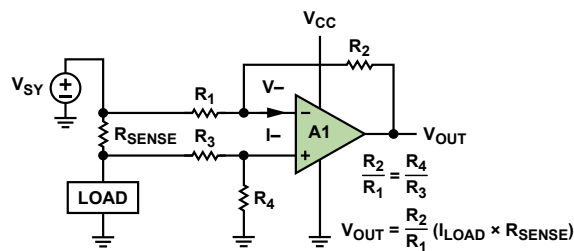


Figure 1. Differential amplifier high-side current sensor. If V_{SY} powers up before V_{CC} , the amplifier's input voltage or current can exceed the data sheet maximum.

Fault Conditions in Operational Amplifiers

Figure 2 shows an N-channel JFET input stage (J_1 , J_2 , R_1 , and R_2), followed by a secondary gain stage and output buffer (A1). When the open-loop amplifier is within its specified IVR, the differential input signal ($V_{IN+} - V_{IN-}$) is 180 degrees out of phase with V_{DIFF} . When connected as a unity-gain buffer, as shown, if the common-mode voltage at V_{IN+} exceeds the amplifier's IVR, J_1 's gate-drain will un-pinch and conduct the entire 200- μ A stage current. As long as J_1 's gate-drain voltage remains reverse-biased, a further increase at V_{IN+} causes no change in V_{DIFF} (V_{OUT} stays at the positive rail). Once J_1 's gate-drain becomes forward-biased, however, a further increase in V_{IN+} raises the voltage at A1's inverting input, causing an undesirable phase-reversal between the input signal and V_{DIFF} .

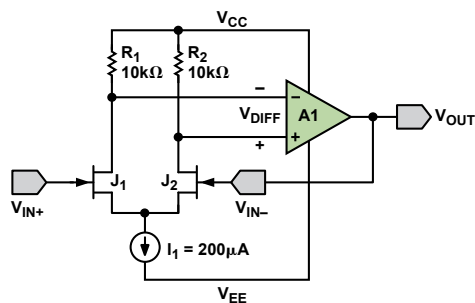


Figure 2. A conceptual N-channel, JFET-input op amp.

Figure 3 shows an example of phase reversal at the output of A1. Unlike bipolar input amplifiers, JFET amplifiers are prone to phase reversal because their inputs are not clamped. CMOS amplifiers are typically immune to phase reversal because the gates are electrically isolated from the drains. If phase inversion doesn't occur, op amp manufacturers will often state this on the data sheet. Phase inversion is possible if: the amplifier inputs are not CMOS, the maximum differential input is V_{SY} , and the data sheet does not claim immunity to phase inversion. Although phase inversion by itself is nondestructive, it can cause positive feedback, which leads to instability in servo loops.

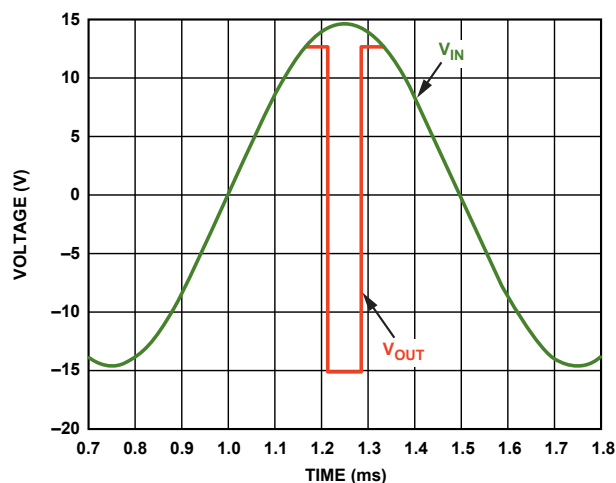


Figure 3. When V_{IN} exceeds the specified IVR, input phase inversion causes the output of the amplifier to become negative.

System designers also have to be concerned about what happens when the amplifier inputs are pulled outside the power supplies. Most often this fault condition occurs when power-supply sequencing causes a source signal to be active before the amplifier supplies turn on, or when a power supply spikes during turn-on, turn-off, or in operation. This condition is destructive for most amplifiers, especially if the overvoltage is greater than a diode drop.

Figure 4 shows a typical bipolar input stage with ESD protection diodes and clamp diodes. In a buffer configuration, when V_{IN+} exceeds either rail, ESD and clamp diodes will be forward biased. With very low source impedance, these diodes will conduct as much current as the source will allow. Precision amplifiers, such as the AD8622, provide a modicum of differential protection by including 500-Ω resistors in series with the inputs to limit the input current when a differential voltage is applied, but they protect only as long as the maximum input current specification isn't exceeded. If the maximum input current is 5 mA, then the maximum allowed differential voltage is 5 V. Note that these resistors are not in series with the ESD diodes, so they cannot limit current to the rails (for example, during an overvoltage condition).

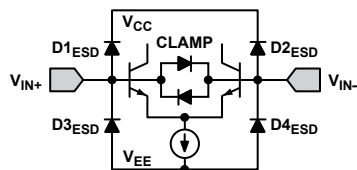
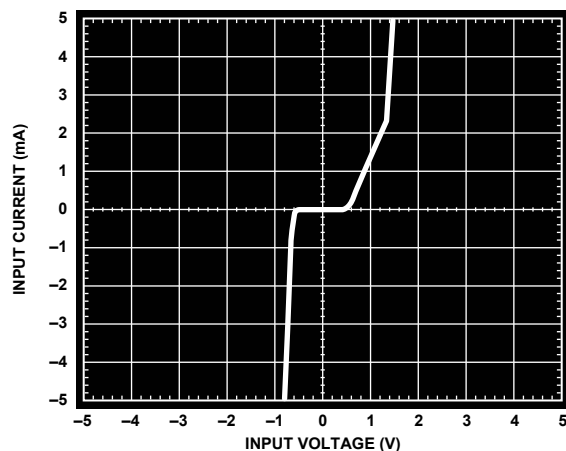


Figure 4. A bipolar input stage showing ESD, and differential protection diodes.

Figure 5 shows the input current-voltage relationship of an unprotected bipolar op amp with differential input and overvoltage applied simultaneously. Once the applied voltage exceeds a diode drop, the current can become destructive, degrading or even destroying the op amp.



OVERVOLTAGE CURVE TRACER TEST SETUP

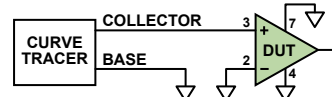


Figure 5. Op amp input current as the differential input voltage exceeds a diode drop.

External Input Overvoltage Protection

From the earliest days of semiconductor op amps, IC designers have had to deal with trade-offs between chip architecture and the external circuitry needed to deal with its weaknesses. Fault protection has been among the most difficult of problem areas (for examples, see MT-036, "Op Amp Output Phase-Reversal and Input Over-Voltage Protection" and MT-069, "In-Amp Input Overvoltage Protection").

Two properties system designers need precision op amps for are their low offset voltage (V_{OS}) and high common-mode rejection ratio (CMRR), both of which simplify calibration and minimize dynamic error. To maintain these specifications in the presence of electrical overstress (EOS), bipolar op amps often include internal clamp diodes and small limiting resistors in series with their inputs, but these cannot address fault conditions caused when the inputs exceed the rails. To add protection, the system designer can implement circuitry such as that shown in Figure 6.

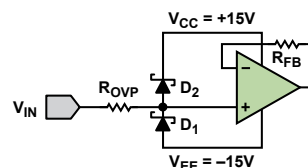


Figure 6. Precision op amp with external protection using a current-limiting resistor and two Schottky diodes. R_{FB} is set equal to R_{OVP} to balance offsets due to input bias currents.

R_{OVP} will limit the current into the op amp if the signal source at V_{IN} powers up first. Schottky diodes have a forward voltage 200 mV less than typical small-signal diodes, so all of the overvoltage current will be shunted through external diodes D_1 and D_2 . However, these diodes can degrade the op amp specifications. For example, the reverse leakage plots from the 1N5711 (see Figure 7) can be used to determine the CMRR penalty for a given OVP resistor. The reverse leakage of the 1N5711 is 0 nA at 0 V and 60 nA at 30 V. With a common mode of 0 V, the additional I_{OS} caused by D_1 and D_2 depends on how well their leakages match. When V_{IN} is taken to +15 V, D_1 will be reverse biased by 30 V, and D_2 will have 0 V bias. Thus, an additional 60 nA flows into R_{OVP} . When the input is taken to -15 V, D_1 and D_2 swap positions electrically, and 60 nA flows out of R_{OVP} . The additional I_{OS} caused by the protection diodes at any common mode is simply:

$$I_{OSaddr} = I_{D1} - I_{D2} \quad (2)$$

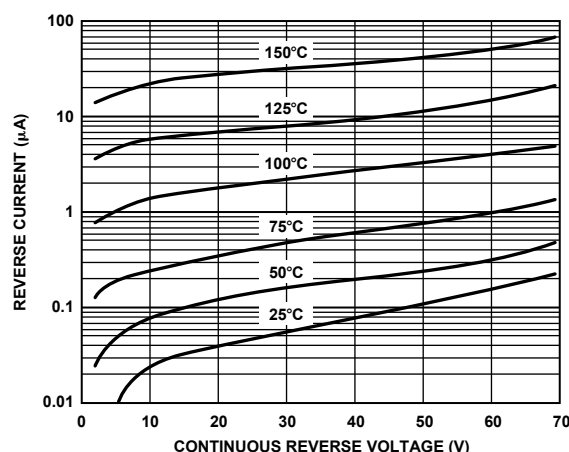


Figure 7. 1N5711 reverse current vs. continuous reverse voltage.

From Equation 2, the V_{OS} penalty can be derived at the extremes of the common-mode range as follows:

$$V_{OSpenalty} = I_{OSaddr} \times R_{OVP} \quad (3)$$

Using 60 nA as the leakage of the 1N5711 at 30 V, and a 5-k Ω protection resistor, V_{OS} at each extreme would be increased by 300 μ V, causing an additional 600 μ V ΔV_{OS} over the entire input-voltage range. In data sheet terms, an op amp with 110-dB CMRR would suffer a 17-dB reduction. Inserting a feedback resistor to equalize source impedance only helps when the common mode is 0 V, and does nothing to prevent additional I_{OS} over the full common-mode range. Table 1 shows the same calculation for diodes commonly used for protecting precision amplifiers. For CMRR penalty calculations, a 5-k Ω protection resistor is assumed. All costs are recent quotes (2011) in USD from www.mouser.com.

Another possible drawback to the method shown in Figure 6 is that the protection diodes shunt the overvoltage current into

the supplies. If, for example, the positive supply cannot sink a significant amount of current, the overvoltage current can force the positive supply voltage to increase.

One way to prevent this is to use back-to-back Zener diodes from the positive input to ground, as shown in Figure 8. When the Zener voltage of either D_1 or D_2 is exceeded, the diode shunts the overvoltage current to ground, protecting the power supplies. This configuration prevents charge pumping during overvoltage conditions, but Zener diodes have higher leakage current and capacitance than small-signal diodes. In addition, Zener diodes have a soft-knee characteristic in their leakage current profile. This, as described previously, adds an additional CMRR penalty over the amplifier's common-mode range. For example, the BZB84-C24 is a back-to-back Zener diode pair with a working voltage between 22.8 V and 25.6 V. The reverse current is specified as 50 nA max at 16.8 V, but the manufacturer doesn't specify what the leakage is closer to the Zener voltage. Also, to achieve a sharper breakdown characteristic, Zener diodes are generally made of more highly doped diffusions than their small-signal cousins. This causes a relative increase in parasitic capacitance, which translates to increased distortion (especially at higher amplitudes) and increased instability.

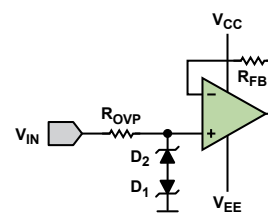


Figure 8. Precision op amp with external protection using a current-limiting resistor and two Zener diodes.

Early Integrated Overvoltage Protection

The previous section discussed drawbacks to some commonly used methods of external amplifier protection. Some of these drawbacks could be avoided if the amplifier itself is designed to tolerate a large input overvoltage. Figure 9 shows a common integrated protection scheme used on a differential input pair.

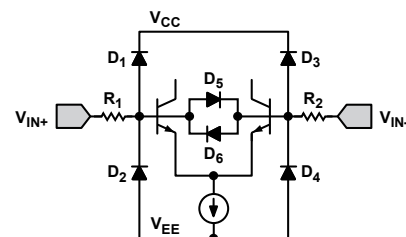


Figure 9. A differential input pair with resistive overvoltage protection (ESD protection not shown).

This circuit includes input protection resistors on both amplifier inputs. Although overvoltage protection is generally needed on only one input, equalizing the parasitic capacitance and leakage

Table 1. Commonly Used Protection Diodes and Their Impact on a 110-dB CMRR Precision Op Amp

	1N5711	BAV99	PAD5	BAS70-04	1N914	BZB84-C24
I_{OSaddr} (nA)	60	10	<<0.005	8	40	50
$V_{OSpenalty}$ (μ V)	600	100	0	80	400	500
CMRR Penalty (dB)	17	6	0	5	14	16
Cost @ 1k Quantities	\$0.07	\$0.015	\$3.52	\$0.095	\$0.01	\$0.034

at each input reduces distortion and offset current. Furthermore, the diodes do not have to handle ESD events, so they can be relatively small.

Adding resistance, either external or internal, adds to the amplifier's root-sum-square (RSS) thermal noise (Equation 4):

$$E_{n,total} = \sqrt{(e_{n,op\ amp})^2 + (e_{n,Rovp})^2 + (R_S \times i_{n,op\ amp})^2} \quad (4)$$

If a 1-k Ω resistor is used to protect an op amp with 4-nV/ $\sqrt{\text{Hz}}$ of noise, the total voltage noise will increase by $\sqrt{2}$. Integrating the protection resistors doesn't change the fact that overvoltage protection increases the input-referred voltage noise, but integrating R_1 and R_2 with the op amp ensures that the data sheet noise specification covers the protective circuitry.

To avoid the noise-overvoltage trade-off requires a protective circuit that presents a low resistance when the amplifier inputs are within the specified range and a very high resistance when the amplifier inputs exceed the rails. This characteristic would provide improved overvoltage protection on-demand, thus lowering the overall noise contribution under normal operating conditions. Figure 10 shows one circuit implementation that behaves in this way.

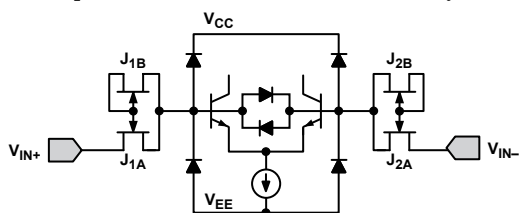


Figure 10. Input differential pair with active overvoltage protection.

J_{xy} are all P-channel JFETs; they are depletion mode devices, so the channel is the same polarity as the source and drain. When the amplifier input levels are between the rails, J_{1A} and J_{2A} act as simple resistors with resistance equal to $R_{DS(on)}$ because the input bias currents are small enough that any potential difference between the channel and gate won't pinch the channel closed. If V_{IN+} were to exceed the negative supply by a diode drop, current would begin to flow through J_{1A} , causing the drain to pinch closed. This transition is actually J_{1A} moving out of triode and into the linear region. If V_{IN+} were to exceed the positive supply voltage by a diode drop, J_{1A} would act as a lateral PNP. V_{IN+} to the gate would act as a forward-biased emitter-base junction, with the other junction acting as the base-collector, standing off overvoltage.

The current-voltage plot of Figure 11 shows the change in input impedance of a FET-protected op amp when subjected to an overvoltage sweep. The $R_{DS(on)}$ of the protection FET is 4.5 k Ω ; as the amplifier's positive input is pulled above the rail, the protection FET's resistance increases rapidly to 22 k Ω at 30 V, limiting the input current to 1.5 mA.

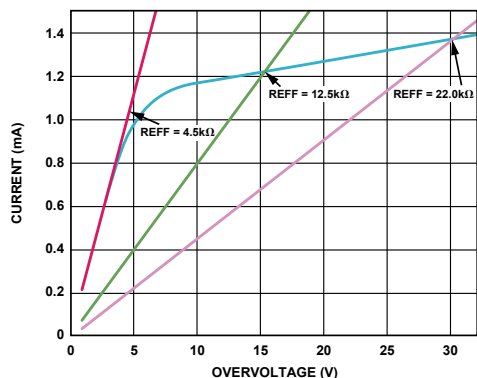


Figure 11. Effective input impedance of a FET protected op amp when subjected to a dc overvoltage sweep.

The Benefits of Integration

Amplifiers such as the ADA4091 and ADA4096 demonstrate that robust, overvoltage-tolerant op amp inputs can be achieved with a minimal impact on precision (as in Figure 10). The ADA4096 provides 32-V protection, regardless of supply levels—eliminating the need for external components that can either be inexpensive but vastly degrade the amplifier's precision, or precise but more costly than the amplifiers themselves.

Figure 12 shows the ADA4096-2 in a 2-mm $\times$ 2-mm LFCSP package next to a couple of discrete components often used for external input protection. The ADA4096-2's integrated protection provides a significantly reduced PCB footprint; its effects are included in the op amp's specifications; and it protects the amplifier even when power is not applied (see Figure 13). In addition, the ADA4091 and ADA4096 have rail-to-rail inputs and outputs (RRIO) and are free from phase-inversion over the entire overvoltage protection range (see Figure 14). These benefits allow system designers to worry a little less about power-supply sequencing and latch-up.

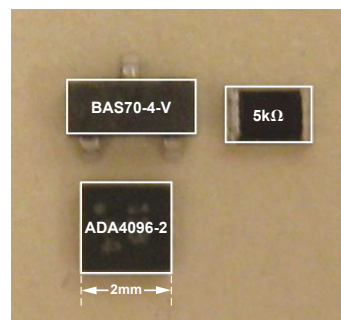


Figure 12. The ADA4096-2 in a 2-mm $\times$ 2-mm package occupies less space than two components commonly used for external voltage protection.

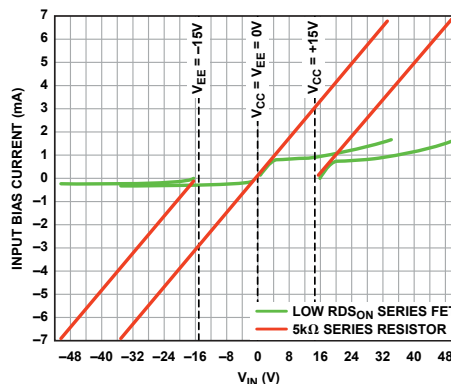


Figure 13. ADA4096-2 input OVP current limiting with and without power.

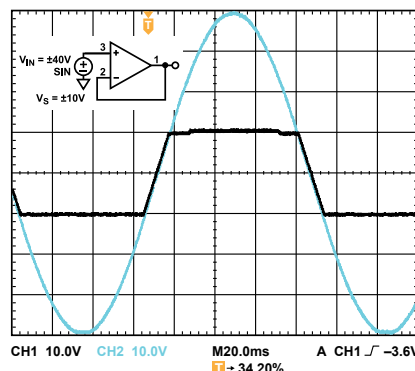


Figure 14. ADA4096-2 on ± 10 -V supplies with the inputs pulled 30 V above and below the rails.

(continued on Page 23)

Modern DACs and DAC Buffers Improve System Performance, Simplify Design

By Padraic O'Reilly and Charly El-Khoury

At the heart of many control systems, digital-to-analog converters (DACs) play a key role in determining system performance and accuracy. This article looks at a new precision 16-bit DAC and shows some ideas for buffering the outputs of high-speed complementary current-output DACs that can rival transformer performance.

Voltage-Switching, 16-Bit DACs Provide Low Noise, Fast Settling, Improved Linearity

By Padraic O'Reilly

Resistance-ladder multiplying DACs, based on the game-changing 10-bit CMOS [AD7520](#)—introduced nearly 40 years ago—were, at first, used with inverting op amps, with the amplifier's summing point (I_{OUTA}) providing a convenient virtual ground (Figure 1).

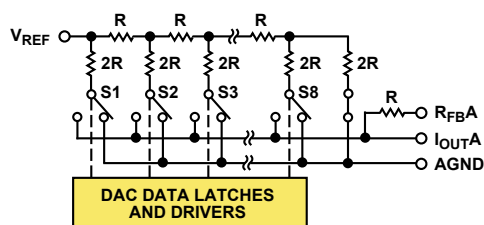


Figure 1. CMOS multiplying DAC architecture.

However, they can also be used, with some limitations, in a [voltage-switching configuration](#) that provides a noninverting voltage output, with the op amp used as a voltage buffer (Figure 2). Here the reference voltage, V_{IN} , is applied to I_{OUT} , and the output voltage, V_{OUT} , is available at V_{REF} . A [12-bit version](#), optimized for this purpose, soon became available.

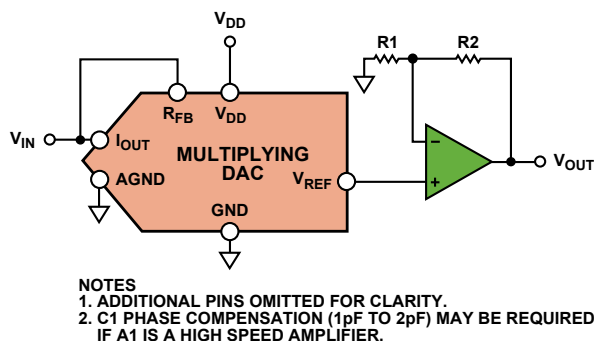


Figure 2. Multiplying DAC in voltage-switching mode.

Fast-forward to the present: As single-supply systems become increasingly common, designers are faced with the challenge of trying to maintain the level of performance achieved at higher voltages while keeping power consumption in check. The need has grown for devices with higher resolution (to 16 bits), capable of being used in this mode.

The obvious advantage of using multiplying DACs in voltage-switching mode is that no signal inversion occurs, so a positive reference voltage results in a positive output voltage. But the R-2R ladder architecture also has a weakness when used in this mode. The nonlinear resistance of the N-channel switches used in series with the R-2R ladder will degrade the integral linearity (INL), as compared to when the same DAC is used in current-steering mode.

Newer high-resolution DACs, such as the [AD5541A](#), shown in Figure 3, have been developed to overcome the limitations of multiplying DACs while maintaining the benefits of voltage switching. Using a partially segmented R-2R ladder network and complementary switches, the AD5541A achieves ± 1 -LSB accuracy at 16 bits without adjustment over the full specified temperature range of -40°C to $+125^{\circ}\text{C}$, 11.8-nV/ $\sqrt{\text{Hz}}$ noise, and 1- μs settling time.

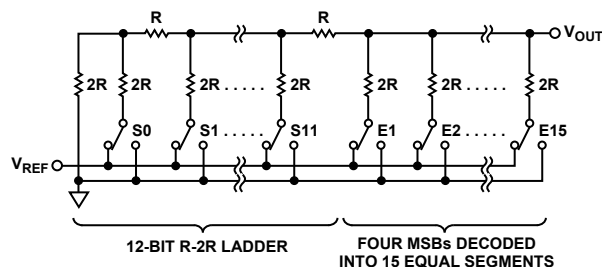


Figure 3. AD5541A architecture.

Performance Features

Settling Time: Figure 4 and Figure 5 compare the respective settling times of a multiplying DAC in voltage mode and the AD5541A. The AD5541A has a settling time of approximately 1 μs when capacitive loading on the output is minimized.

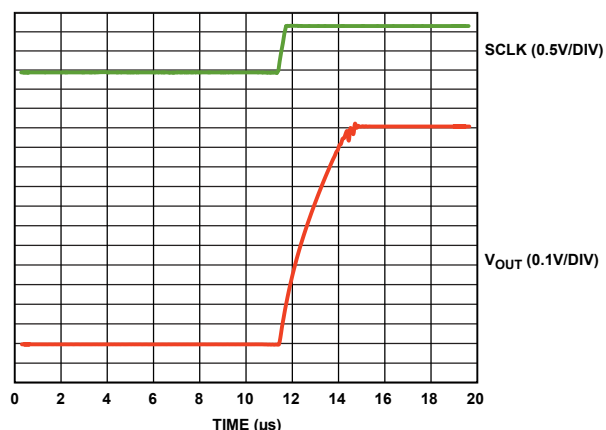


Figure 4. Multiplying DAC settling time.

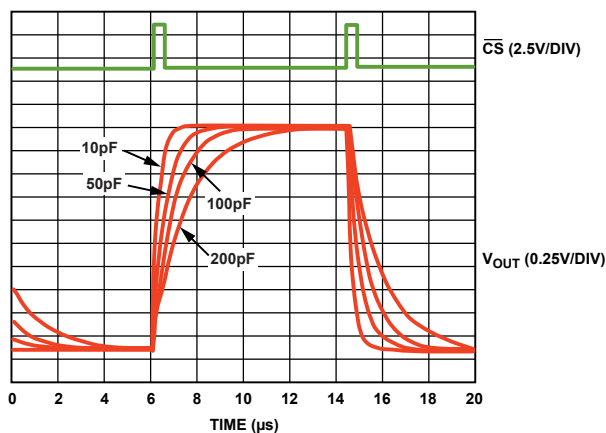


Figure 5. AD5541A settling time.

Noise Spectral Density: Table 1 compares noise spectral density of the AD5541A and the multiplying DAC. The AD5541A exhibits slightly better performance at 10 kHz and far better performance at 1 kHz.

Table 1. Noise Spectral Density of AD5541A vs. Multiplying DAC

DAC	NSD @ 10 kHz (nV/√Hz)	NSD @ 1 kHz (nV/√Hz)
AD5541A	12	12
MDAC	30	140

Integral Nonlinearity: Integral nonlinearity measures the maximum deviation between the ideal output of a DAC and the actual output after gain and offset errors have been removed. The switches used in series with the R-2R network can affect the INL. Multiplying DACs generally employ NMOS switches. When used in voltage-switching mode, the source of the NMOS switch is connected to the reference voltage, the drain is connected to the ladder, and the gate is driven by the internal logic (Figure 6).

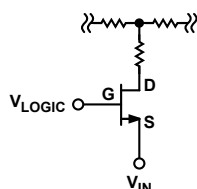


Figure 6. Multiplying DAC switch.

For current to flow in an NMOS device, V_{GS} must be greater than the threshold voltage, V_T . In voltage-switching mode, $V_{GS} = V_{LOGIC} - V_{IN}$ must be greater than $V_T = 0.7$ V.

The R-2R ladder of a multiplying DAC is designed to divide the current evenly through each of the legs. This requires the overall resistance to ground, seen from the top of each leg, to be exactly the same. This can be accomplished by scaling the switches, where the size of each switch is proportional to its *on* resistance. If the resistance in one leg changes, the current flowing through that leg will change, causing a linearity error. V_{IN} cannot be so large as to shut off the switch, but it must be large enough to keep the switch resistance low, as changes in V_{IN} affect V_{GS} and, therefore, cause a nonlinear change in on resistance as shown by:

$$R_{ON} = \frac{1}{\beta(V_{GS} - V_T)}$$

This change in on resistance will unbalance the currents and degrade the linearity. Thus, the supply voltage on the multiplying DAC cannot be reduced too much. Conversely, the reference voltage should be no more than 1 V above AGND to maintain linearity. With a 5-V supply, the linearity starts to degrade when moving from a 1.25-V reference to a 2.5-V reference, as shown in Figure 7 and Figure 8. The linearity falls apart altogether when the supply voltage is decreased to 3 V, as shown in Figure 9.

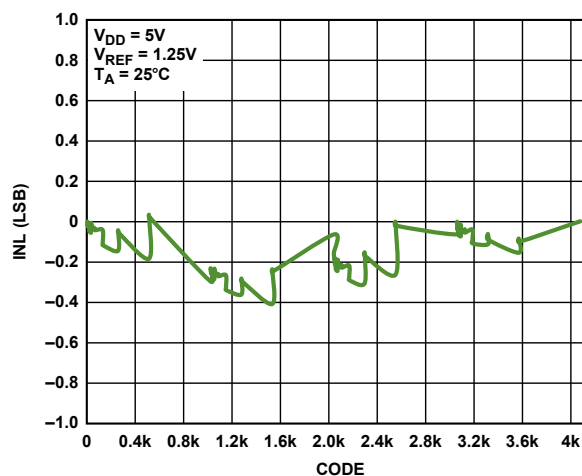


Figure 7. INL of I_{OUT} multiplying DAC in reverse mode, $V_{DD} = 5$ V, $V_{REF} = 1.25$ V.

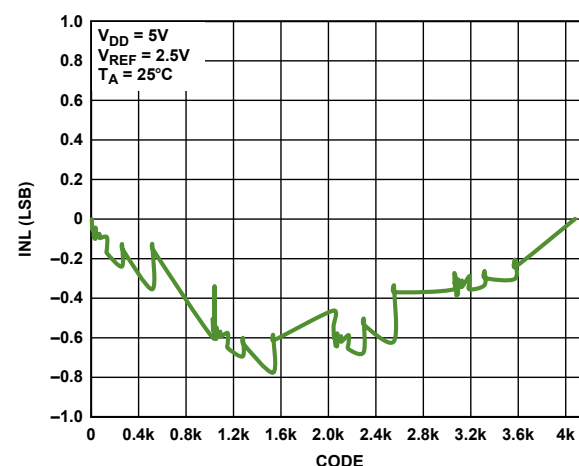


Figure 8. INL of I_{OUT} multiplying DAC in reverse mode, $V_{DD} = 5$ V, $V_{REF} = 2.5$ V.

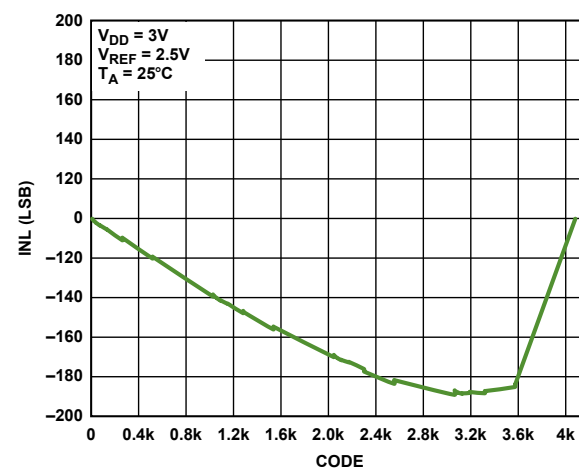


Figure 9. INL of multiplying DAC in reverse mode, $V_{DD} = 3$ V, $V_{REF} = 2.5$ V.

To minimize this effect, the AD5541A uses complementary NMOS/PMOS switches, as shown in Figure 10. Now, the total on resistance of the switch comes from the parallel contribution of the NMOS and PMOS switches. As previously shown, the gate voltage of the NMOS switch is controlled by internal logic. An internally generated voltage, V_{GN} , sets the ideal gate voltage to balance the on resistance of the NMOS with that of the PMOS. The switches are sized to scale with code so the on resistance will scale with code. Thus, the currents will scale, and accuracy will be maintained. As the reference input sees an impedance that varies with code, it should be driven from a low impedance source.

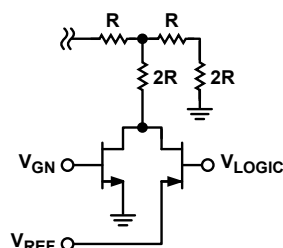


Figure 10. Complementary NMOS/PMOS switches.

Figure 11 and Figure 12 show the INL performance of the AD5541A with 5-V and 2.5-V references.

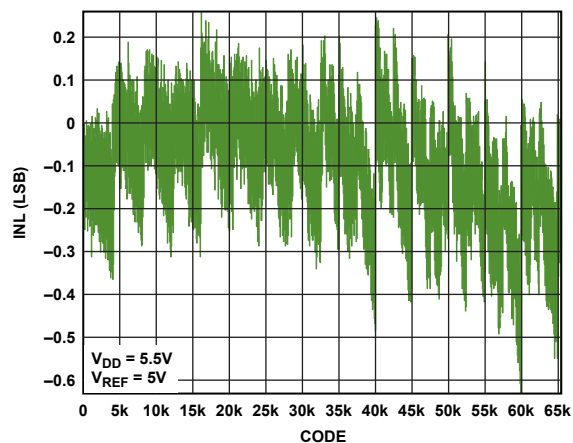


Figure 11. INL of AD5541A, $V_{DD} = 5.5\text{ V}$, $V_{REF} = 5\text{ V}$.

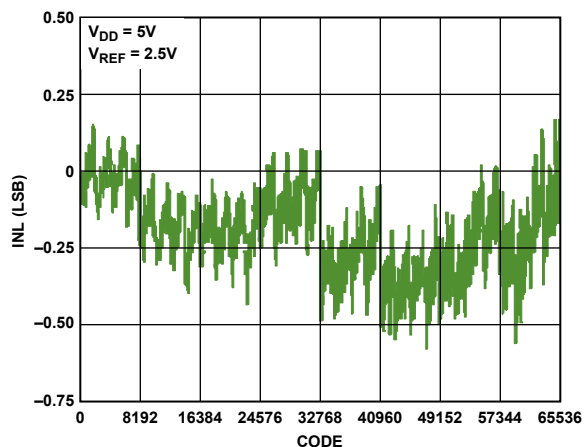


Figure 12. INL of AD5541A, $V_{DD} = 5\text{ V}$, $V_{REF} = 2.5\text{ V}$.

Figure 13 and Figure 14 show that the linearity changes very little over a wide range of reference and supply voltages. The DNL behavior is similar to that of the INL. The AD5541A linearity is specified over temperature and supply voltage; and the reference voltage can go from 2.5 V to the supply voltage.

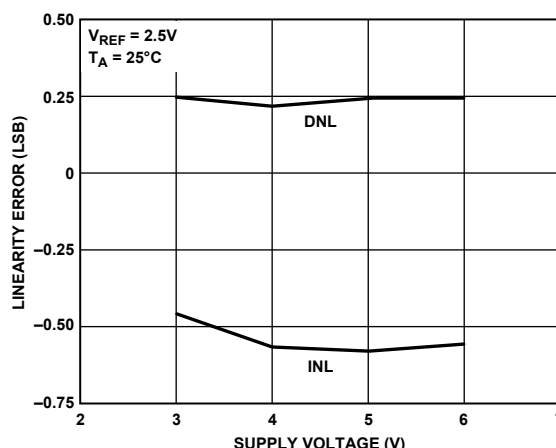


Figure 13. AD5541A INL vs. supply voltage.

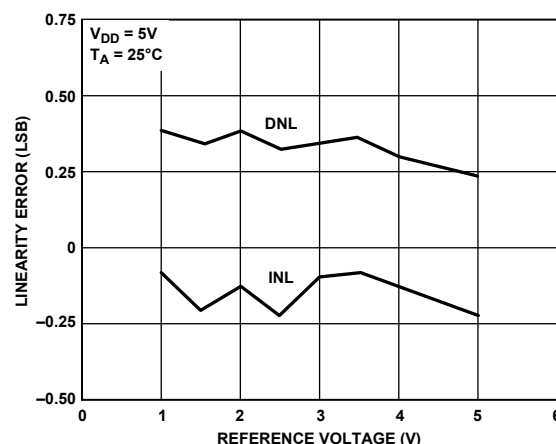


Figure 14. AD5541A INL vs. reference voltage.

More About the AD5541A

The [AD5541A](#) serial-input, single-supply, voltage-output *nanoDAC+* digital-to-analog converter provides 16-bit resolution with ± 0.5 -LSB typical integral- and differential nonlinearity. It is well suited to applications that use multiplying DACs in voltage-switching mode. It performs well over both temperature and supply voltage, achieves excellent linearity, and can be used in 3-V to 5-V systems where precision dc performance and quick settling are required. Using an external reference voltage that can range from 2 V to the supply voltage, the unbuffered voltage output can drive a 60-k Ω load from 0 V to V_{REF} . Featuring 1- μ s settling to $\frac{1}{2}$ LSB, 11.8-nV/ $\sqrt{\text{Hz}}$ noise, and low glitch, the device is well suited for deployment in a wide variety of medical, aerospace, communications, and industrial applications. Its 3-wire, low-power SPI-compatible serial interface can be clocked at up to 50 MHz. Operating on a single 2.7-V to 5.5-V supply, the AD5541A draws only 125 μ A. Available in 8-lead and 10-lead LFCSP and 10-lead MSOP packages, it is specified from -40°C to $+125^{\circ}\text{C}$ and priced from \$6.25 in 1000s.

High Speed Current Output DAC Buffers

By Charly El-Khoury

Transformers are often considered to be the best option for converting the complementary output of a high-speed current-output DAC to a single-ended voltage output, as transformers do not add noise or consume power. Although transformers operate well with high-frequency signals, they cannot handle the low-frequency signals required for many instrumentation and medical applications. These applications require a low-power, low-distortion, low-noise, high-speed amplifier to convert the complementary current to a single-ended voltage. The three circuits presented here accept the complementary output currents from the DAC and provide a single-ended output voltage. Distortion for the last two is compared with a transformer solution.

Difference Amplifier: The AD8129 and AD8130 differential-to-single-ended amplifiers (Figure 15) are used in the first circuit (Figure 16). They feature extremely high common-mode rejection at high frequency. The AD8129 is stable for gains of 10 or more, whereas the AD8130 is stable with unity gain. Their user-adjustable gain can be set by the ratio of two resistors, R_F and R_G . The AD8129 and AD8130 have very high input impedance on Pin 1 and Pin 8, regardless of the gain setting. A reference voltage (V_{REF} , Pin 4) can be used to set a bias voltage that is multiplied by the same gain as the differential input voltage.

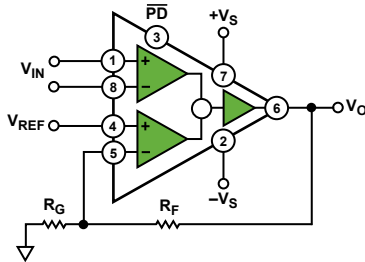


Figure 15. AD8129/AD8130 difference amplifiers.

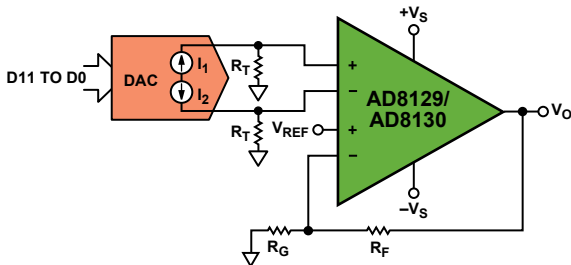


Figure 16. DAC buffer using AD8129/AD8130.

Equation 1 and Equation 2 show the relation between the output voltage of the amplifier and the complementary output current of the DAC. The termination resistors, R_T , perform a current-to-voltage conversion; the ratio of R_F and R_G determines the gain. V_{REF} is set to 0 in Equation 2.

$$V_{IN} = I_1 R_T - I_2 R_T = R_T (I_1 - I_2) \quad (1)$$

$$V_O = \left(1 + \frac{R_F}{R_G}\right) (V_{IN} + V_{REF}) \quad (2)$$

$$= \left(1 + \frac{R_F}{R_G}\right) R_T (I_1 - I_2)$$

In Figure 16, this circuit is applied with a quad high-speed, low-power, 14-bit DAC, where the complementary current-output stage increases the speed and reduces the distortion of low-power DACs.

Figure 17 shows the spurious-free dynamic range (SFDR) of the circuit, as a function of frequency, using the DAC and the AD8129, with $R_F = 2 \text{ k}\Omega$, $R_G = 221 \Omega$, $R_T = 100 \Omega$, and $V_O = 8 \text{ V p-p}$, at two values of the supply voltage. Here, the AD8129 was chosen because it provides a large output signal, is stable for $G = 10$, and has a high gain-bandwidth product compared to the AD8130. The SFDR is generally better than 55 dB for both cases, to beyond 10 MHz, with approximately >3-dB improvement at the lower supply voltage.

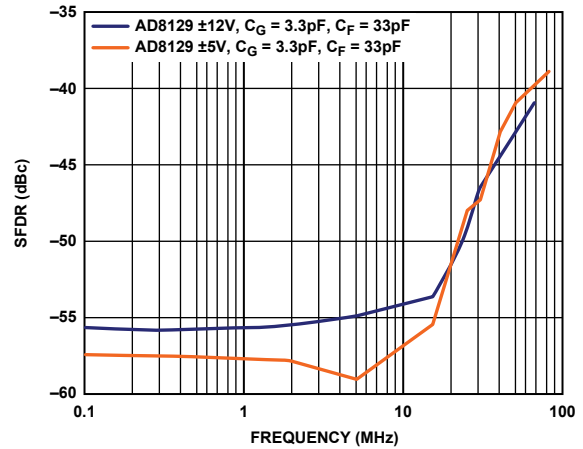


Figure 17. Distortion of the DAC and AD8129 with $V_O = 8 \text{ V p-p}$.

Op Amp at Unity Gain: The second circuit (Figure 18) uses a high-speed amplifier with two R_T resistors. The amplifier simply transforms the complementary currents, I_1 and I_2 , into a single-ended output voltage, V_O , through R_T . This simple circuit does not allow signal amplification using the amplifier as a gain block.

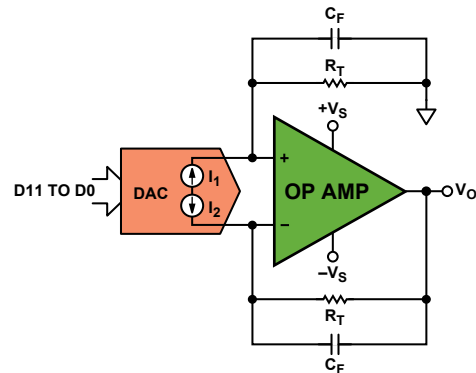


Figure 18. Simple differential-to-single-ended converter using an op amp.

Equation 3 shows the relationship between V_O and the DAC output current. Distortion data was measured with 5-pF capacitors in parallel with R_T .

$$V_O = (I_1 R_T - I_2 R_T) = R_T (I_1 - I_2) \quad (3)$$

To demonstrate the performance of this circuit, the DAC was paired with the ADA4857 and ADA4817 op amps, with $R_T = 125 \Omega$ (and $C_T = C_F = 5 \text{ pF}$ in parallel with R_T for stability and low-pass filtering). The single ADA4857-1 and dual ADA4857-2 are unity-gain stable, high-speed, voltage-feedback amplifiers with low distortion, low noise, and high slew rate. An ideal solution for a variety of applications, including ultrasound, ATE, active filters, and ADC drivers, it features 850-MHz

bandwidth, 2800-V/ μ s slew rate, and 10-ns settling time to 0.1%—all while operating on 5 mA of quiescent current. With a wide supply voltage range (5 V to 10 V), the ADA4857-1 and ADA4857-2 are ideal candidates for systems that require wide dynamic range, precision, high speed, and low power.

The single ADA4817-1 and dual ADA4817-2 *FastFET™* amplifiers are unity-gain stable, ultrahigh-speed, voltage-feedback op amps with FET inputs. Developed on ADI's proprietary *eXtra Fast Complementary Bipolar* (XFCB) process, they achieve ultralow noise (4 nV/ $\sqrt{\text{Hz}}$ and 2.5 fA/ $\sqrt{\text{Hz}}$) and very high input impedance. With 1.3-pF input capacitance, 2-mV maximum offset voltage, low power dissipation (19 mA), and wide -3-dB bandwidth (1050 MHz), they are ideal for data acquisition front ends, photodiode preamps, and other wideband transimpedance applications. With a 5-V to 10-V supply voltage range and the ability to operate on either single or dual supplies, they are designed to work in a variety of applications, including active filtering, ADC driving, and DAC buffering.

Figure 19 compares the distortion vs. frequency of this circuit at $V_O = 500$ mV p-p with a circuit using a transformer. The transformer has less distortion than the amplifier, which has decreasing gain, at high frequencies, but its distortion becomes increasingly worse at low frequencies. Here, SFDRs of nearly 90 dB are achievable over a limited range, with better than 70 dB to 10 MHz.

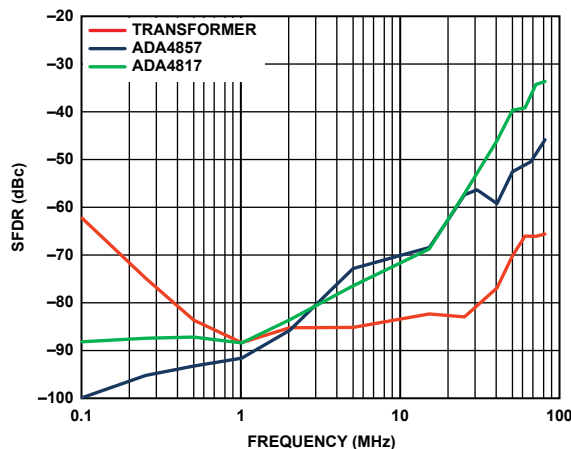


Figure 19. Distortion of the DAC, ADA4857, and ADA4817 with $V_O = 500$ mV p-p, $R_L = 1$ k Ω .

Op Amp with Gain: The third circuit (Figure 20) also uses the same high-speed op amps but includes a resistive network that distances the amplifier from the DAC, allows for gain setting, and has the flexibility to adjust the output bias voltage using either of the two reference voltages, V_{REF1} and V_{REF2} .

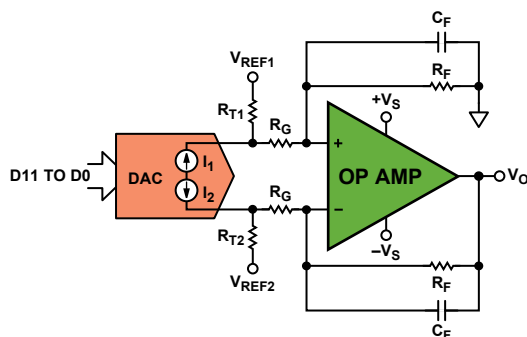


Figure 20. Differential-to-single-ended with gain and bias capability.

Equation 4 defines the relationship between the DAC output current and the amplifier output voltage for $V_{REF1} = V_{REF2} = 0$. To match the input impedance of the amplifier network looking out of the DAC, the two termination resistors, R_{T1} and R_{T2} , must be set individually, taking into consideration the characteristics of the amplifier.

$$V_O = I_1 \left(\frac{R_{T1} \times R_F}{R_{T1} + R_F + R_G} \right) \left(1 + \frac{R_F}{R_G + R_{T2}} \right) - I_2 \left(\frac{R_{T2} \times R_F}{R_G + R_{T2}} \right) \quad (4)$$

Figure 21 compares the distortion of the amplifiers in this configuration with that of the transformer circuit. $R_{T1} = 143 \Omega$, $R_{T2} = 200 \Omega$, $R_F = R_G = 499 \Omega$, $C_F = 5$ pF—for stability and high frequency filtering—and $R_L = 1$ k Ω . Here, the performance of the ADA4817 is comparable to that of the transformer at high frequency, maintaining better than -70 dBc SFDR up to 70 MHz. Both op amps maintain excellent low-frequency fidelity compared to the transformer.

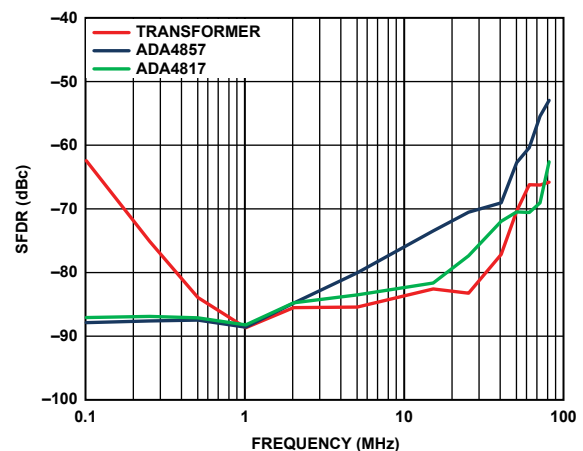


Figure 21. Distortion of the DAC, ADA4817, and ADA4857 with $V_O = 500$ mV p-p.

This article showed some of the advantages of using low-distortion, low-noise, high-speed amplifiers as DAC buffers comparing their performance with that of transformers. It also compares three types of application circuits using two different amplifier architectures, while giving examples of measured data with a DAC and the AD8129, ADA4857-1/ADA4857-2, and ADA4817-1/ADA4817-2 amplifiers. The data show that the amplifier outperforms the transformer at frequencies less than 1 MHz and can closely match its performance up to 80 MHz. Amplifier selection is important when considering trade-offs in terms of power dissipation and distortion.

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DDS Devices Generate High-Quality Waveforms Simply, Efficiently, and Flexibly

By Brendan Cronin

Abstract

Direct digital synthesis (DDS) technology is used to generate and modify high-quality waveforms in a broad range of applications in such diverse fields as medicine, industry, instrumentation, communications, and defense. This article provides an overview of the technology, describes its benefits and limitations, and takes a look at some application examples—and new products that make the technology more readily available.

Introduction

A key requirement across a multitude of industries is to accurately produce, easily manipulate, and quickly change waveforms of various frequencies and types. Whether a wideband transceiver requires an agile low-phase-noise frequency source with excellent spurious-free dynamic performance or an industrial measurement and control system needs a stable frequency stimulus, the ability to quickly, easily, and cost effectively generate an adjustable waveform while maintaining phase continuity is a critical design criterion that *direct digital frequency synthesis* can fulfill.

The Task of Frequency Synthesis

Increasing spectrum congestion, coupled with the insatiable need for lower power, higher quality measurement equipment, calls for the use of new frequency ranges and better exploitation of existing ones. As a result, better control of frequency generation is being sought—in most cases with the assistance of *frequency synthesizers*. These devices use a given frequency, f_C , to generate a waveform at a related desired frequency (and phase), f_{OUT} . The general relationship can be written simply as

$$f_{OUT} = \varepsilon_x \times f_C$$

where the scaling factor, ε_x , is sometimes called the *normalized frequency*.

The equation is always implemented using algorithms for step-by-step approximations of real numbers. When the scaling factor is a rational number, a ratio of two relatively prime integers, the output frequency and the reference frequency will be harmonically related. In most cases, however, ε_x can belong to a much broader set of real numbers, and the approximation process is truncated as soon as it falls within an acceptable limit.

Direct Digital Frequency Synthesis

One such practical realization of a frequency synthesizer is *direct digital frequency synthesis* (DDFS), often shortened to *direct digital synthesis* (DDS). The technique uses digital data processing to generate a frequency- and phase-tunable output related to a fixed frequency reference, or clock source, f_C . In a DDS architecture, the reference or system clock frequency is divided down by the scaling factor, set by a programmable binary tuning word.

Simply stated, a direct digital frequency synthesizer translates a train of clock pulses into an analog waveform, typically a sine, triangular, or square wave. As Figure 1 shows, its essential parts are: a *phase accumulator*, which produces a number corresponding to a phase angle of the output waveform, a *phase-to-digital converter*, which generates the instantaneous digital fraction of the output amplitude occurring at a particular phase angle, and a *digital-to-analog converter* (DAC), which converts that digital value to a sampled analog data point.

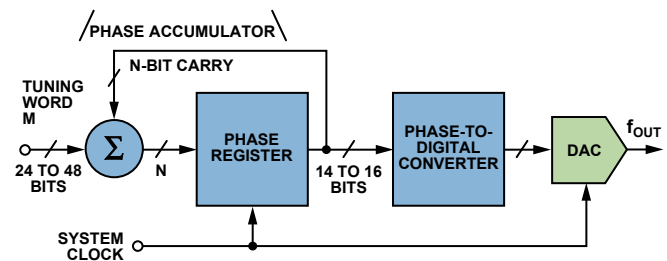


Figure 1. Functional block diagram of a DDS system.

For sine-wave outputs, the phase-to-digital converter is usually a sine lookup table (Figure 2). The phase accumulator counts by N , to generate a frequency related to f_C according to the equation,

$$f_{OUT} = \frac{N}{2^M} f_C$$

where:

M is the resolution of the tuning word (24 bits to 48 bits).

N is the number of pulses of f_C corresponding to the smallest incremental phase change of the phase accumulator's output word.

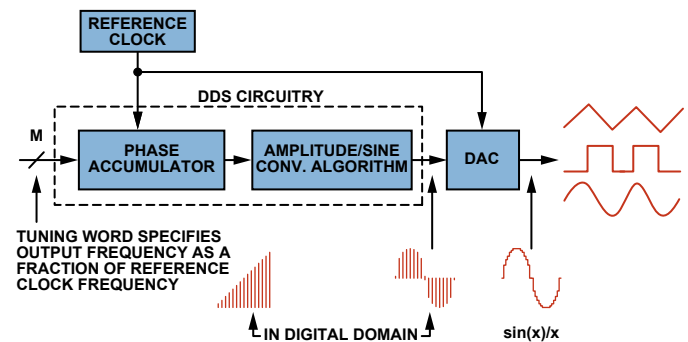


Figure 2. Typical DDS architecture and signal path with DAC.

Since changes to N result in immediate changes in the output phase and frequency, the system is inherently *phase-continuous*, a critical attribute in many applications. No loop settling time is required, in contrast to analog-type systems, such as *phase-locked loops* (PLLs).

The DAC is usually a high-performance circuit specifically designed to work with the DDS core (phase accumulator and phase-to-amplitude converter). In most cases, the resulting device, often a single chip, is commonly referred to as a complete DDS or C-DDS.

Practical DDS devices often integrate multiple registers to allow various frequency- and phase-modulation schemes to be realized. When included, the phase register's contents are added after the phase accumulator. This enables the output sine wave to be phase-delayed in correspondence with a phase tuning word. This is extremely useful for phase-modulation applications in communication systems. The resolution of the adder circuit determines the number of bits in the phase tuning word and, therefore, the resolution of the delay.

Integrating a DDS engine and a DAC in a single device has advantages and disadvantages, but whether integrated or not, a DAC is required to create a high quality analog signal of exceptional purity. The DAC converts the digital sine output into an analog sine wave and may be either single-ended or differential. A few of the key requirements are low phase noise, excellent wideband (WB-) and narrow-band (NB-) *spurious-free dynamic range* (SFDR), and low power consumption. If it is an external component, the DAC needs to be fast enough to process the signal—so devices with a parallel port are common.

DDS vs. Other Solutions

Other possibilities for frequency generation include analog *phase-locked loops* (PLLs), clock generators, and using an FPGA to dynamically program the output of a DAC. A simple comparison of the technologies can be made by examining spectral performance and power consumption, qualitatively demonstrated in Table 1.

Table 1. DDS vs. Competing Technologies—High Level Comparison

	Power Consumption	Spectral Purity	Comment
DDS	Low	Medium	Easy to tune
Discrete DAC + FPGA	Medium	Medium-high	Ability to tune
Analog PLL	Medium	High	Difficult to tune

A phase-locked loop is a feedback loop comprising: a *phase comparator*, a divider, and a *voltage-controlled oscillator* (VCO). The phase comparator compares a reference frequency with the output frequency (usually divided down by a factor, N). The error voltage generated by the phase comparator is applied to the VCO, which generates the output frequency. When the loop has settled, the output will bear an accurate relationship to the reference in frequency and/or phase. PLLs have long been recognized as superior devices for low phase noise and high *spurious-free dynamic range* (SFDR) applications requiring high fidelity and stable signals in a specific band of interest.

Their inability to accurately and quickly tune the frequency output and waveform and their slow response limits their suitability for applications such as agile frequency hopping and some frequency- and phase-shift keying applications.

Other approaches, including *field-programmable gate arrays* (FPGAs) with embedded DDS engines—in combination with off-the-shelf DACs to synthesize output sine waves—solve the frequency-hopping difficulties of PLLs, but have their own weaknesses. The main system disadvantages include higher operating and interface power requirements, higher cost, large size, and additional software-, hardware-, and memory overhead for the system developer. For example, up to 72 kB of memory are required to generate a 10-MHz output signal with 60-dB dynamic range using the DDS engine option on modern FPGAs. In addition, the designer needs to be comfortable and familiar with subtle trade-offs and the architecture of the DDS core.

As a practical matter (see Table 2), rapid advances in CMOS processing, together with modern digital design techniques and improved DAC topologies, have resulted in the DDS technology achieving power consumption, spectral performance, and cost levels that were previously unattainable for a wide range of applications. While complete DDS products will never match the highest performance and design flexibility achievable with custom combinations of high-end DAC technology and FPGAs, the size-, power- and cost benefits, coupled with the simplicity of DDS devices, may make them easily the first choice for many applications.

Also note that since a DDS device fundamentally embodies a digital method of generating an output waveform, it can simplify the architecture of some solutions or make it possible to digitally program the waveform. While a sine wave is normally used to explain the function and operation of a DDS, it is easily possible to generate triangular or square (clock) wave outputs from modern DDS ICs, avoiding the need for a lookup table in the former case, and for a DAC in the latter case, where the integration of a simple yet precise comparator will suffice.

DDS Performance and Limitations

Images and Envelopes: $\sin(x)/x$ Roll-Off

The actual output of the DAC is not a continuous sine wave but a train of pulses with a sinusoidal time envelope. The corresponding frequency spectrum is a set of images and aliases. The images lie along a $\sin(x)/x$ envelope (see $|\text{amplitude}|$ plot in Figure 3). Filtering is necessary to suppress frequencies outside the band of interest, but it cannot suppress higher-order aliases (due to DAC nonlinearities, for example) appearing within the pass band.

The *Nyquist Criterion* dictates that a minimum of two samples per cycle are required to reconstruct a desired output waveform. Image responses are created in the sampled output spectrum at $K f_{\text{CLOCK}} \pm f_{\text{OUT}}$. In this example, where $f_{\text{CLOCK}} = 25$ MHz and $f_{\text{OUT}} = 5$ MHz, the first and second images occur (see Figure 3) at $f_{\text{CLOCK}} \pm f_{\text{OUT}}$, or 20 MHz and 30 MHz. The third and fourth images appear at 45 MHz and 55 MHz. Note that the $\sin(x)/x$ nulls appear at multiples of the sampling frequency. In the case where f_{OUT} is greater than the *Nyquist bandwidth* ($1/2 f_{\text{CLOCK}}$), the first image response will appear within the Nyquist bandwidth as an *aliased* image (a 15-MHz signal will alias down to 10 MHz, for example). The aliased image cannot be filtered from the output with a traditional Nyquist *antialiasing* filter.

Table 2. Benchmark Analysis Summary—Frequency-Generation Technologies (<50 MHz)

	Phase-Locked Loops	DAC + FPGA	DDS
Spectral Performance	High	Medium-high	Medium
System Power Requirements	High	High	Low
Digital Frequency Tuning	No	Yes	Yes
Tuning Response Time	High	Low	Low
Solution Size/Footprint	Medium	High	Low
Waveform Flexibility	Low	Medium	High
Cost	Medium	High	Low
Design Reuse	Medium	Low	High
Implementation Complexity	Medium	High	Low

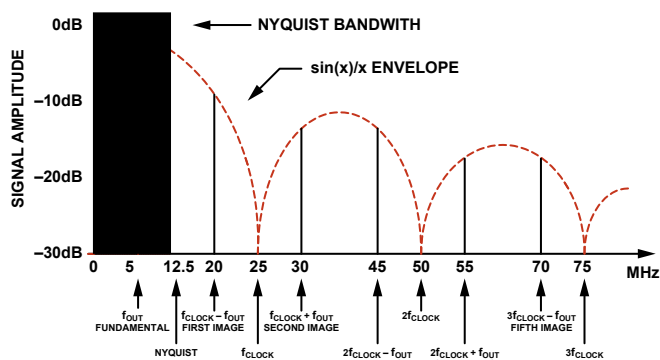


Figure 3. $\sin(x)/x$ roll-off in a DDS.

In typical DDS applications, a low-pass filter is utilized to suppress the effects of the image responses in the output spectrum. To keep the cutoff requirements of the low-pass filter reasonable and the filter design simple, an accepted guideline is to limit the f_{OUT} bandwidth to approximately 40% of the f_{CLOCK} frequency using an economical low-pass output filter.

The amplitude of any given image in response to the fundamental can be calculated using the $\sin(x)/x$ formula. Because the function rolls off with frequency, the amplitude of the fundamental output will decrease inversely with its tuned frequency; in a DDS system, the decrease will be -3.92 dB over the dc to Nyquist bandwidth.

The amplitude of the first image is substantial—within 3 dB of the fundamental. To simplify filtering requirements for DDS applications, it is important to generate a frequency plan and analyze the spectral considerations of the image and the $\sin(x)/x$ amplitude responses at the desired f_{OUT} and f_{CLOCK} frequencies. Online interactive [design tools](#) supporting the Analog Devices DDS product family allow for quick and easy simulation of where images lie and allow the user to choose frequencies where images are outside the band of interest. See the *Further Information and Useful Links* section for additional useful information.

Other anomalies in the output spectrum, such as integral and differential linearity errors of the DAC, glitch energy associated with the DAC, and clock feedthrough noise, will not follow the $\sin(x)/x$ roll-off response. These anomalies will appear as harmonics and spurious energy in many places in the output spectrum—but will generally be much lower in amplitude than the image responses. The general noise floor of a DDS device is determined by the cumulative combination of substrate noise, thermal noise effects, ground coupling, and other sources of signal coupling. The noise floor, performance spurs, and jitter of a DDS device are greatly influenced by circuit board layout, the quality of the power supplies, and—most importantly—the quality of the input reference clock.

Jitter

A perfect clock source would have edges occurring at precise intervals in time that would never vary. This, of course, is impossible; even the best oscillators are constructed from non-ideal components and have noise and other imperfections. A high-quality, low-phase-noise crystal oscillator will have jitter on the order of picoseconds, accumulated over many millions of clock edges. Jitter is caused by thermal noise, instabilities in the oscillator's electronic circuitry, and external interference through the power, ground, and output connections—all contributing to disturbances in the oscillator's timing. In addition, oscillators are influenced by external magnetic or electric fields, and RF interference from nearby transmitters. A simple amplifier, inverter, or buffer in the oscillator circuitry will also add jitter to a signal.

So choosing a stable reference clock oscillator with low jitter and sharp edges is critical. Higher frequency reference clocks allow greater oversampling, and jitter can be somewhat ameliorated by *frequency division*, since dividing the frequency of the signal yields the same amount of jitter across a longer period, and so reduces the percentage of jitter on the signal.

Noise—including Phase Noise

Noise in a sampled system depends on many factors, starting with reference clock jitter, which shows up as phase noise on the fundamental signal. In a DDS system, truncation of the phase register output may introduce code-dependent system errors. Binary-coded words don't cause truncation errors. For nonbinary coded words, however, the phase-noise truncation error produces spurs in the spectrum. The frequency/magnitude of the spurs is determined by the code word. The DAC's quantization and linearity errors will also add harmonic noise in the system. Time-domain errors, such as undershoot/overshoot and code glitches, all contribute distortion to the output signal.

Applications

DDS applications can be segmented into two primary categories:

- Communication and radar systems that require agile frequency sources for data encoding and modulation applications
- Measurement, industrial, and optical applications that require a generic frequency synthesis function with programmable tuning, sweeping, and excitation

In both cases, an increasing trend towards higher spectral purity (lower phase noise and higher spurious-free dynamic range) is coupled with low operating power and size requirements for remote or battery-operated equipment.

DDS in Modulation/Data Encoding and Synchronization

From its exclusive origins in radar and military applications, some of the advances in DDS product characteristics (performance improvements, cost, and size) have combined to make DDS technology very popular in modulation and data encoding applications. This section will discuss two data encoding schemes and their proposed implementation with a DDS system.

Binary frequency shift keying (BFSK, or simply FSK) is one of the simplest forms of data encoding. The data is transmitted by shifting the frequency of a continuous carrier between one (binary 1, or *mark*) and the other (binary 0, or *space*) of two discrete frequencies. Figure 4 shows the relationship between the data and the transmitted signal.

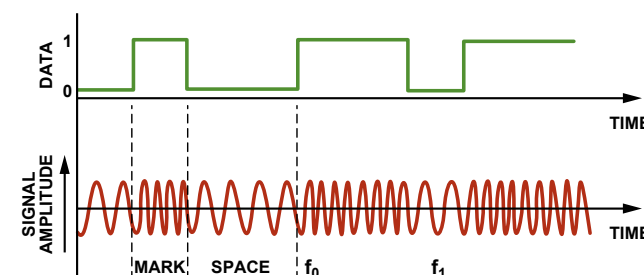


Figure 4. Binary FSK modulation.

Binary 1s and 0s are represented as two different frequencies, f_0 and f_1 , respectively. This encoding scheme is easily implemented with a DDS device. The DDS frequency tuning word representing the output frequencies is changed so that f_0 and f_1 are generated from 1s and 0s to be transmitted. In at least two members of Analog Devices complete DDS product families (the [AD9834](#) and the [AD9838](#)—see also the Appendix), the user can simply

program the two current FSK frequency tuning words into the IC's embedded frequency registers. To shift output frequency, a dedicated pin, FSELECT, selects the register containing the appropriate tuning word (see Figure 5).

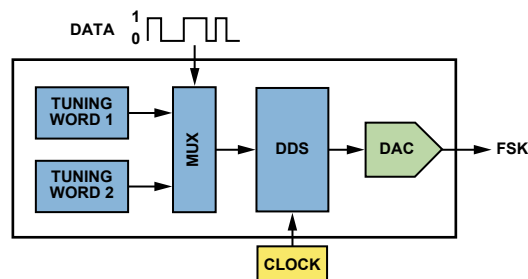


Figure 5. FSK encoding using the tuning-word selector of an AD9834 or AD9838 DDS.

Phase-shift keying (PSK) is another simple form of data encoding. In PSK, the frequency of the carrier remains constant, and the phase of the transmitted signal is varied to convey the information. Several schemes can be used to accomplish PSK. The simplest method, commonly known as binary PSK (or BPSK), uses only two signal phases: 0° (Logic 1) and 180° (Logic 0). The state of each bit is determined according to the state of the preceding bit. If the phase of the wave does not change, the signal state stays the same (low or high). If the phase of the wave changes by 180° , that is, if the phase reverses—the signal state changes (low to high, or high to low). PSK encoding is easily implemented with a DDS product as most of the devices have a separate input register (a *phase register*) that can be loaded with a phase value. This value is directly added to the phase of the carrier without changing its frequency. Changing the contents of this register modulates the phase of the carrier, generating a PSK output. For applications that require high-speed modulation, the AD9834 and AD9838, which have pairs of phase registers, allow signals on a PSELECT pin to alternate between the preloaded phase registers to modulate the carrier as required.

More complex forms of PSK employ four or eight wave phases. This allows binary data to be transmitted at a faster rate per phase change than is possible with BPSK modulation. In four-phase modulation (*quadrature PSK*), the possible phase angles are 0° , $+90^\circ$, -90° , and $+180^\circ$; each phase shift can represent two signal elements. The AD9830, AD9831, AD9832, and AD9835 provide four phase registers to allow complex phase modulation schemes to be implemented by continuously updating different phase offsets to the registers.

I/Q Capability Using Multiple DDS Components in Synchronous Mode

Many applications require the generation of two or more sinusoidal or square wave signals having a known phase relationship. A popular example is *in-phase and quadrature modulation (I/Q)*, a technique wherein signal information is derived from a carrier frequency at its 0° and 90° phase angles. Two single DDS components can be run from the same source clock to output signals whose phase relationship can be directly controlled and manipulated. In Figure 6, the AD9838 devices are programmed using one reference clock; the same RESET pin is used to update both devices. In this way, simple I/Q modulation can be achieved.

A reset must be initiated after power-up and before transferring any data to the DDS. This establishes the DDS output in a known phase, which becomes the common reference angle that allows synchronization of multiple DDS devices. When new data is sent simultaneously to multiple DDS devices, a coherent phase relationship can be maintained—or the relative phase offset

between multiple DDS devices can be predictably shifted by means of the phase offset register. The AD983x series of DDS products have 12 bits of phase resolution, providing an effective resolution of 0.1° .

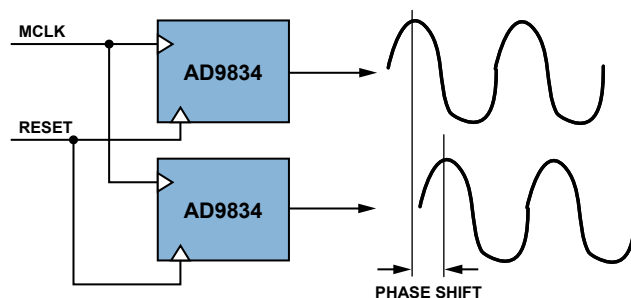


Figure 6. Synchronizing two DDS components.

For more information about synchronizing multiple DDS devices, see [AN-605](#) Application Note, *Synchronizing Multiple AD9852 DDS-Based Synthesizers*.

Network Analysis

Many applications in the electronic world involve the gathering and decoding of data from networks such as analog measurement and optical communications systems. Normally, the system analysis requirement is to stimulate a circuit or system with a frequency of known amplitude and phase, and analyze the signal characteristics of the response signal through the system.

The information gathered on the response signal is used to determine key system information. The range of networks being tested (see Figure 7) can be quite wide, including cable integrity testing, biomedical sensing, and flow-rate measurement systems. Wherever the basic requirement is to generate frequency-based signals and compare phase and amplitude of the response signal(s) to the original signal, or if a range of frequencies needs to be excited through the system, or if test signals with different phase relationships (as in systems with I/Q capability) are required, direct digital synthesis ICs can be highly useful for digitally controlling stimulus frequency and phase through software with simplicity and elegance.

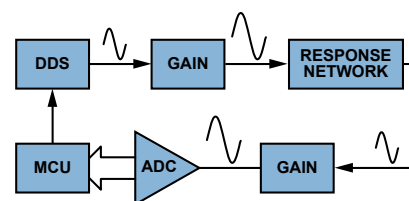


Figure 7. Typical network analysis architecture using frequency stimulus.

Cable Integrity/Loss Measurement

Cable integrity measurement is a noninvasive method of analyzing cables in applications such as airplane wiring, local area networks (LANs), and telephone lines. One way to determine performance is to see how much signal is lost through the cable. By injecting a signal of known frequency and amplitude, the user can calculate cable attenuation by measuring the amplitude and phase at remote portions of the cable. Parameters such as dc resistance and characteristic impedance will affect a particular cable's attenuation. The result is usually expressed in decibels below the signal source (0 dB) over the frequency range of the test. The frequencies of interest depend on the cable type. DDS devices, with their ability to generate a wide range of frequencies, can be used as a stimulus with the necessary frequency resolution.

Flow Meter

A related application area is in water, other liquids, and gas flow analysis in pipelines. An example is ultrasonic flow measurement, which operates on a phase-shift principle, as shown in Figure 8. Basically, a signal is transmitted from one side of the channel where the liquid is flowing and a transducer sensor is positioned on the opposite side to measure the phase response—which depends on the flow rate. There are many variations on this technique. Test frequencies depend on the substance being measured; in general, the output signal is often transmitted over a range of frequencies. DDS provides the flexibility to set and change the frequency seamlessly.

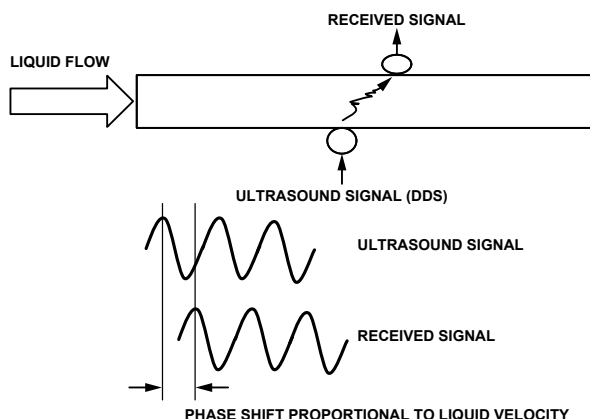


Figure 8. Ultrasonic flow meter.

Author

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FURTHER INFORMATION AND USEFUL LINKS

Interactive Design Tool

What is it? An online interactive design tool for DDS is an assistant for selecting tuning words, given a reference clock and desired output frequencies and/or phases. The tool shows the tuning word and other configuring bits encoded as a sequence of codes for use in programming the part via its serial interface. Idealized output harmonics can be shown for the selected reference clock and output frequency after an external reconstruction filter has been applied. Links to ADI's design tools can be found on the [Interactive Design Tools](#) home page. One example is the [AD9834 design tool](#).

Evaluation Kit

The AD983x series of products come with a fully functional [evaluation kit](#) with schematics and layout. The software provided in the evaluation kit allows the user to easily program, configure, and test the device (see Figure 9).

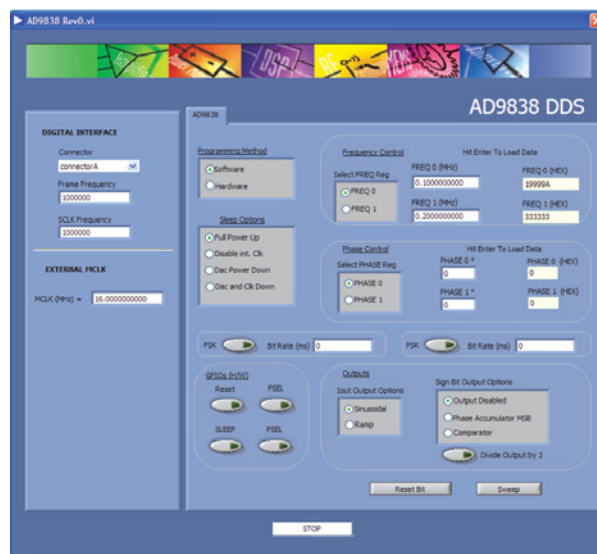


Figure 9. AD9838 evaluation software interface.

Other useful DDS information can be found on the [DDS website](#).

See also:

Murphy, Eva and Colm Slattery. "All About Direct Digital Synthesis." Ask The Applications Engineer—33. *Analog Dialogue*. Volume 38, No. 3, (2004): 8–12.

A Technical Tutorial on Digital Signal Synthesis. 1999. Analog Devices, Inc.

APPENDIX

The AD9838 in Brief: A block diagram of the AD9838 DDS appears in Figure 10. Built on a fine-line CMOS process, the device is an ultralow power (11-mW), complete DDS. The 28-bit frequency registers permit 0.06-Hz frequency resolution with a 16-MHz clock and 0.02-Hz frequency resolution with a 5-MHz clock. Phase- and frequency modulation are configured via on-chip registers using software or pin selection. The device features –68-dBc wideband and –97-dBc narrow-band SFDR and operates over the extended temperature range of –40°C to +125°C. The device is housed in a small 4-mm × 4-mm, 20-lead LFCSP (lead-frame chip-scale package).

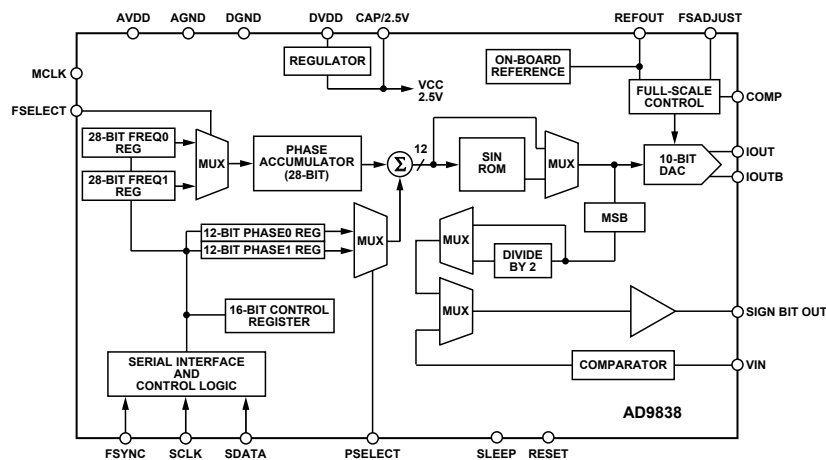


Figure 10. Block diagram of the AD9838 DDS.

Efficient FSK/PSK Modulator Uses Multichannel DDS to Switch at Zero Crossings

By David Brandon and Jeff Keip

Frequency-shift keying (FSK) and phase-shift keying (PSK) modulation schemes are used in digital communications, radar, RFID, and numerous other applications. The simplest form of FSK uses two discrete frequencies to transmit binary information, with Logic 1 representing the mark frequency and Logic 0 representing the space frequency. The simplest form of PSK is binary (BPSK), which uses two phases separated by 180° . Figure 1 illustrates the two types of modulation.

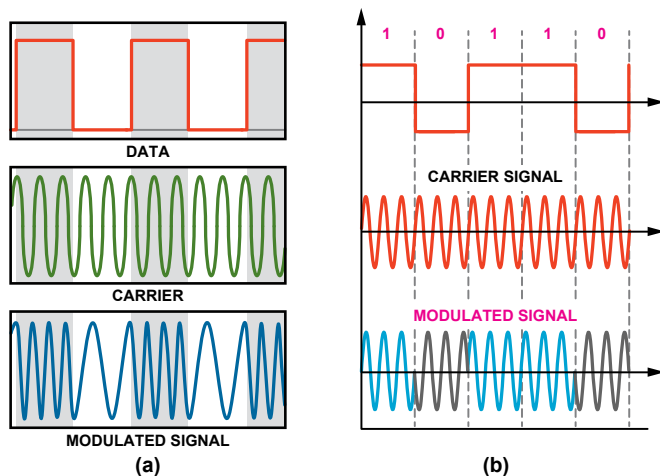


Figure 1. Binary FSK (a) and PSK (b) modulation.

The modulated output of a *direct digital synthesizer* (DDS) can switch frequency and/or phase in a *phase-continuous* or *phase-coherent* manner, as shown in Figure 1, and as described in “[Multichannel DDS Enables Phase-Coherent FSK Modulation](#),” making DDS technology well suited for both FSK and PSK modulation.

This article describes how two synchronized DDS channels can implement a *zero-crossing* FSK or PSK modulator. Here, the AD9958 two-channel, 500-MSPS, complete DDS (see Appendix) is used to switch frequencies or phases at the zero-crossing point, but any two-channel synchronized solution should be capable of accomplishing this function. In phase-coherent radar systems, zero-crossing switching reduces the amount of post processing needed for signature recognition of the target; and implementing PSK at the zero crossing reduces spectral splatter.

Although both of the AD9958 DDS-channel outputs are independent, they share an internal system clock and reside on a single piece of silicon, so they should provide more reliable channel-to-channel tracking over temperature and power-supply deviations than the outputs of multiple, single-channel devices synchronized together. The process variability that may exist between distinct devices is also larger than any process variability you might see between two channels fabricated in a single piece of silicon, making a multichannel DDS preferable for use as a zero-crossing FSK or PSK modulator.

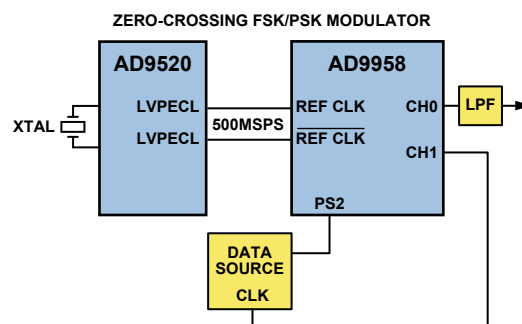


Figure 2. Setup for zero-crossing FSK or PSK modulator.

A critical element of any DDS is the phase accumulator, which, in this implementation, is 32 bits wide. When the accumulator overflows, it retains any excess value. When the accumulator overflows with no remainder (see Figure 3), the output is precisely at Phase 0, and the DDS engine starts over from where it was at Time 0. The rate at which the zero-overflow is experienced is referred to as the *grand-repetition rate* (GRR) of the DDS.

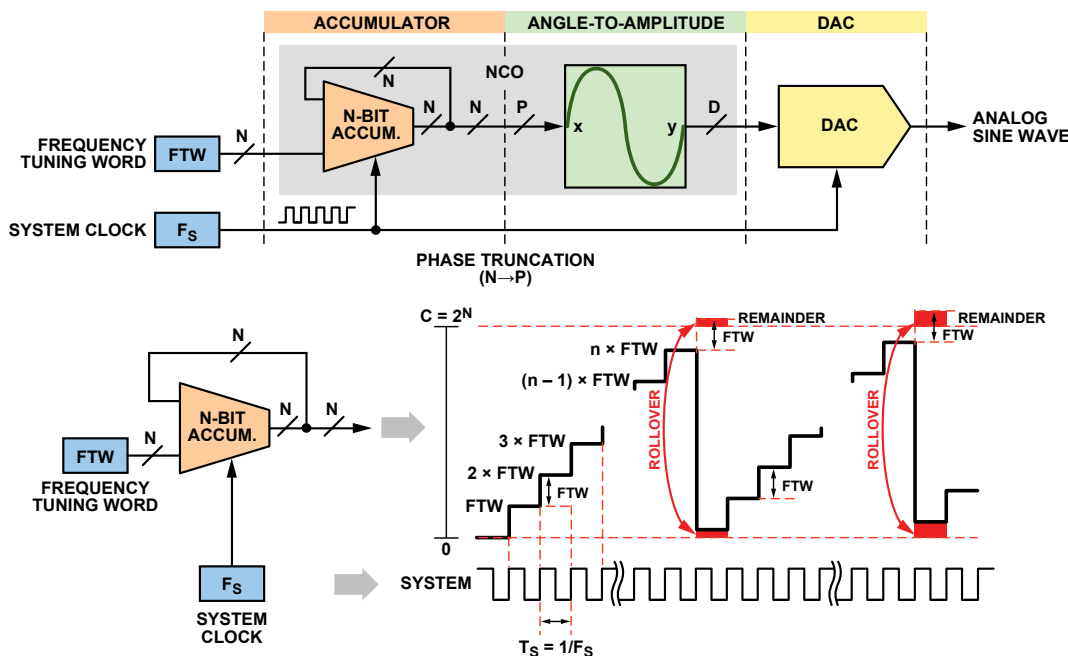


Figure 3. Basic DDS with overflowing accumulator.

The GRR is determined by the rightmost nonzero bit of the DDS *frequency tuning word* (FTW), as established by the following equation:

$$GRR = F_S/2^n$$

where:

F_S is the sampling frequency of the DDS.

n is the rightmost nonzero bit of the FTW.

For example, suppose a DDS with a 1-GHz sampling frequency employs 32-bit mark and space FTWs with the binary values shown. In this case, the rightmost nonzero bit of either FTW is the 19th bit, so $GRR = 1 \text{ GHz}/2^{19}$, or approximately 1907 Hz.

```
Mark (CH0) 00101010 00100110 10100000 00000000
Space (CH0) 00111010 11110011 11000000 00000000
GRR (CH1) 00000000 00000000 00100000 00000000
```

A DDS inherently switches frequency in a phase-continuous manner. This means that no instantaneous phase change occurs when the frequency tuning word changes. That is, the accumulator starts accumulating the new FTW from whatever phase position it was at when the new FTW was applied. Phase coherence, on the other hand, requires an instantaneous transition to the phase of the new frequency as if the new frequency had been present all along. Therefore, in order for a standard DDS to implement a phase-coherent FSK switch, the change from a mark frequency to a space frequency must occur when both frequencies have the same absolute phase. To implement a zero-crossing switch in a phase-coherent manner, the DDS must make the frequency transition at 0 degrees (that is, when the accumulator overflows with zero excess). Therefore, we must determine the instants at which phase coherent zero-crossings occur. If the GRR of the mark and space FTWs are known, the smaller of the two GRRs (if different) will indicate the desired phase coherent zero-crossing point.

Three criteria are necessary for implementing a phase-coherent zero-crossing switch:

1. The ability to determine the smaller GRR of the mark and space FTWs associated with CH0 of Figure 2.
2. A second DDS channel (CH1 of Figure 2) synchronized to CH0 of Figure 2 and programmed with an FTW having all zeros except for the one bit corresponding to the smaller GRR.
3. The capability to use the rollover of the second channel to trigger a frequency change on CH0 of Figure 2.

Unfortunately, the latency between when a DDS accumulator hits zero and when that zero phase is represented at the output further complicates the solution. Fortunately, this latency is constant. The ideal solution necessitates that the auxiliary channel be phase adjusted to compensate for this latency. Both channels on the AD9958 have a *phase-offset* word that can be used to fix this problem.

The AD9958 two-channel DDS produced the results shown in Figure 4, Figure 5, and Figure 6. Figure 4 and Figure 5 exhibit phase-continuous FSK switching vs. zero-crossing FSK switching. Figure 5 shows both phase continuous switching and phase coherent switching. Figure 6 shows the results from a pseudorandom sequence (PRS) data stream that toggles between multiple frequencies.

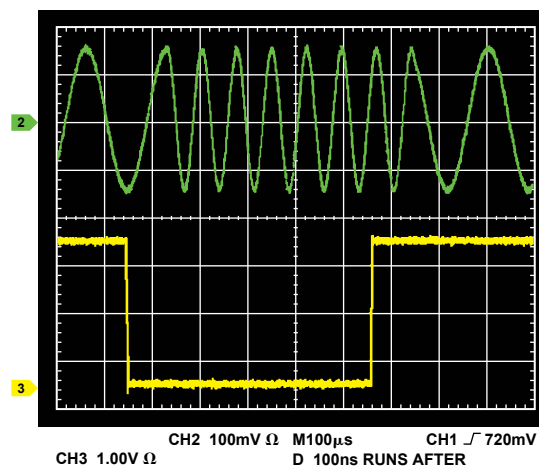


Figure 4. Phase-continuous FSK transition.

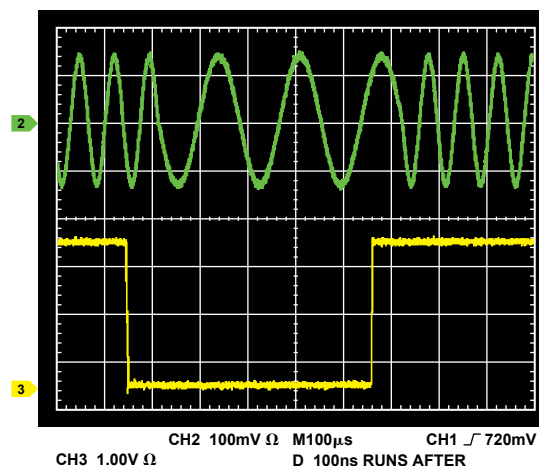


Figure 5. Zero-crossing FSK transition.

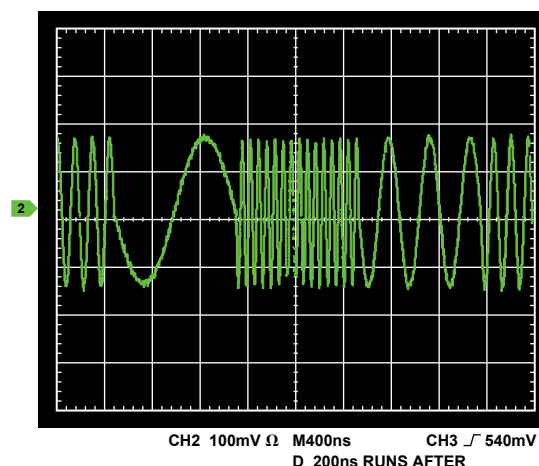


Figure 6. Zero-crossing with multi-FSK transitions.

The AD9958 two-channel DDS produced the results shown in Figure 7 and Figure 8. These figures exhibit phase-continuous BPSK switching vs. zero-crossing BPSK switching.

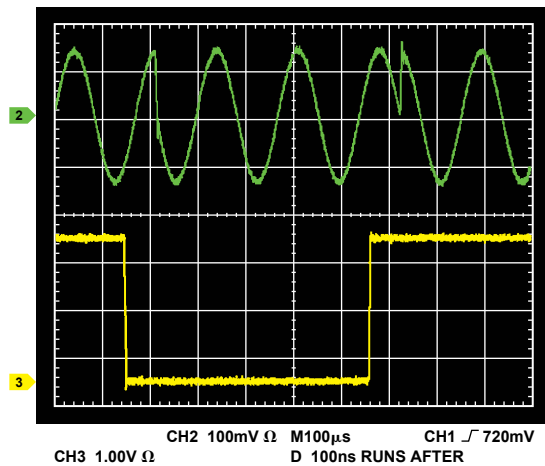


Figure 7. Phase-continuous BPSK transition.

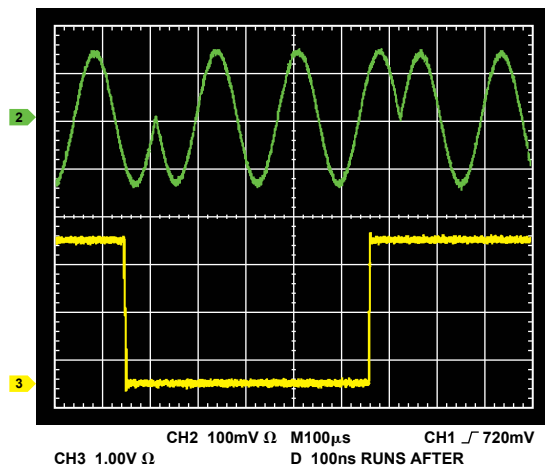


Figure 8. Zero-crossing BPSK transition.

Authors

David Brandon [david.brandon@analog.com] has supported DDS products since the first DDS released back in 1995. His career spans 28 years at ADI, with the last 11 years as an applications engineer in the Clock and Signal Synthesis Group. He has authored a number of application notes and a couple of magazine articles.



Jeff Keip [jeff.keip@analog.com] has nearly 20 years of experience in the semiconductor industry; over 15 of those have been spent working on and with frequency synthesis products. For the past nine years, Jeff has had primary responsibility for the high-speed DDS product portfolio at ADI.



APPENDIX

Two-Channel, 10-Bit, 500-MSPS Direct Digital Synthesizer

The **AD9958** two-channel direct digital synthesizer (DDS) comes complete with two 10-bit, 500-MSPS current-output DACs, as shown in Figure 9. Both channels share a common system clock, providing inherent synchronization; additional packages can be used if more than two channels are required. The frequency, phase, and amplitude of each channel can be independently controlled, allowing them to provide correction for system-related mismatches. These parameters can be swept linearly; or 16 levels can be chosen for FSK, PSK, or ASK modulation. Output sine waves can be tuned with 32-bit frequency resolution, 14-bit phase resolution, and 10-bit amplitude resolution. Operating with a 1.8-V core supply, plus a 3.3-V I/O supply for logic compatibility, the AD9958 consumes 315 mW with all channels *on*, and 13 mW in *power-down* mode. Specified from -40°C to $+85^{\circ}\text{C}$, it is available in a 56-lead LFCSP package and priced at \$20.24 in 1000s.

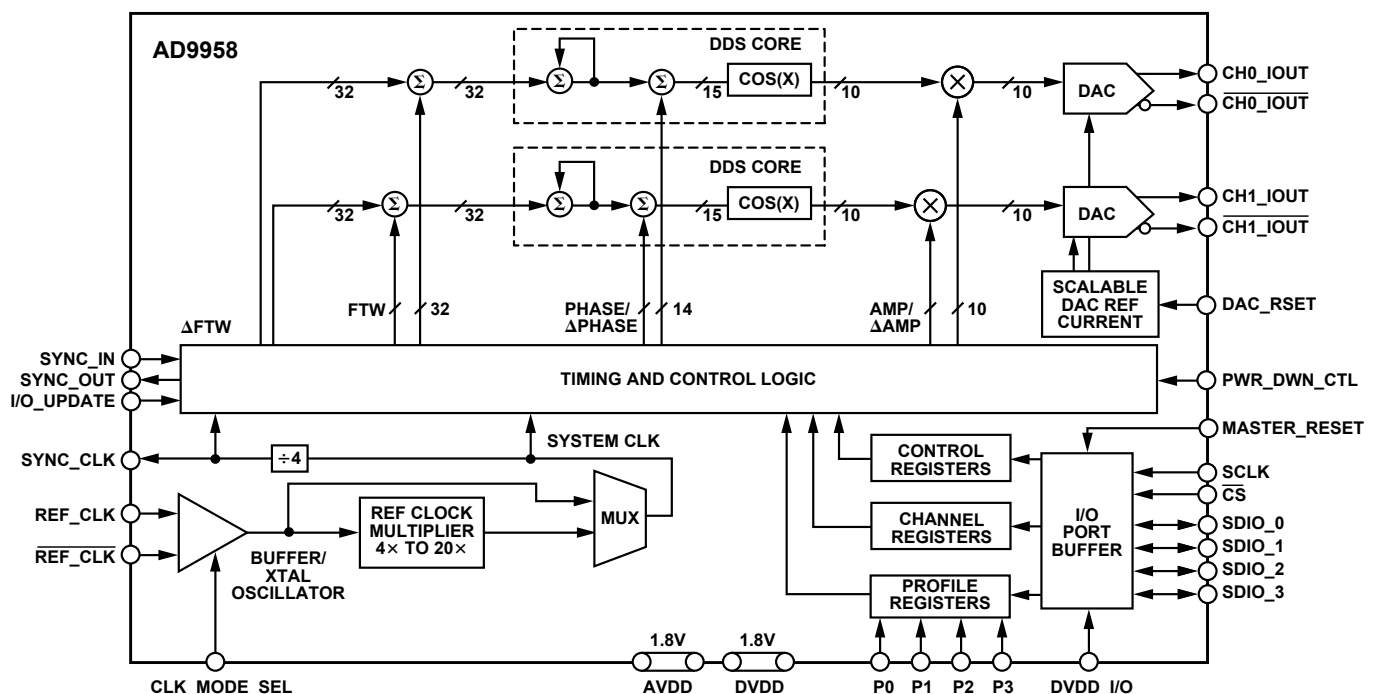


Figure 9. AD9958 block diagram.

Low-Noise, Gain-Selectable Amplifier

By Nathan Carter and Chilann Chan

Data acquisition, sensor signal conditioning, and other applications with input signals that vary over a wide range require gain-selectable amplifiers. Traditional gain-selectable amplifiers use switches in the feedback loop to connect resistors to the inverting input, but the switch resistance degrades the noise performance of the amplifier, adds significant capacitance on the inverting input, and contributes to nonlinear gain error. The additional noise and capacitance are especially bothersome when working with low-noise amplifiers, and the nonlinear gain error is problematic in precision applications.

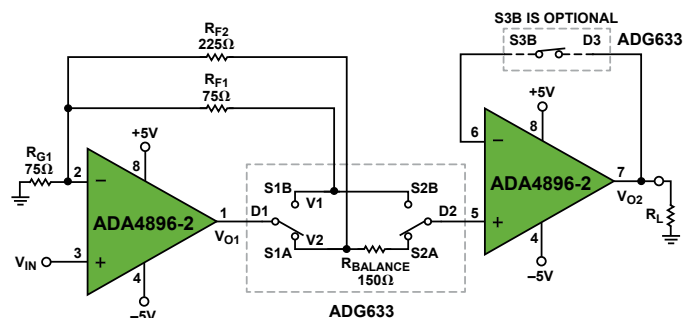


Figure 1. Using the ADA4896-2 and the ADG633 to construct a low-noise, gain-selectable amplifier to drive a low-resistance load.

The gain-selectable amplifier shown in Figure 1 uses an innovative switching technique that preserves the 1-nV/√Hz noise performance of the ADA4896-2 while reducing the nonlinear gain error. With this technique, the user can choose switches with minimal capacitance to maximize the bandwidth of the circuit.

The switches, implemented with an ADG633 triple SPDT CMOS switch, are configured such that either S1A and S2A are on, or S1B and S2B are on. Switch S1 connects to the output end of the feedback resistors, and Switch S2 samples at a point (V1 or V2) where the nonlinear switch resistance does not affect the gain. This reduces the gain error while preserving the noise performance. With the values shown, the first stage amplifier gain is 4 V/V when the “A” switches are on or 2 V/V when the “B” switches are on. The number of switched gains can be extended with additional switch packages or by using a multiplexer such as the 4:1 ADG659 or 8:1 ADG658.

Note that an offset is created by the input bias current of the output buffer flowing through the nonlinear on resistance of the S2 sampling switch. To compensate for this offset, place the unused switch (S3B) in the feedback path of the output buffer.

In addition, the bias current of the input amplifier causes a gain-dependent offset. Because the input amplifier and output buffer are built on the same chip, the relative matching of their bias currents can be used to cancel out the varying offset. Placing a resistor equal to the difference between R_F2 and R_F1, in series with Switch S2A, results in less offset-voltage variation.

The following derivation shows that sampling at V1 yields the desired signal gain without gain error. R_S denotes the switch resistance. V2 can be derived using the same method.

$$V_{O1} = V_{IN} \times \left(1 + \frac{R_{F1} + R_{S1}}{R_{G1}} \right) \quad (1)$$

$$V_1 = V_{O1} \times \left(\frac{R_{F1} + R_{G1}}{R_{F1} + R_{G1} + R_{S1}} \right) \quad (2)$$

Substituting Equation 1 into Equation 2,

$$V_1 = V_{IN} \times \left(1 + \frac{R_{F1}}{R_{G1}} \right) \quad (3)$$

Note that if V_O1 yields the desired signal gain without gain error, the buffered output, V_O2, will also be free from gain error. Figure 2 shows the normalized frequency response of the circuit at V_O2.

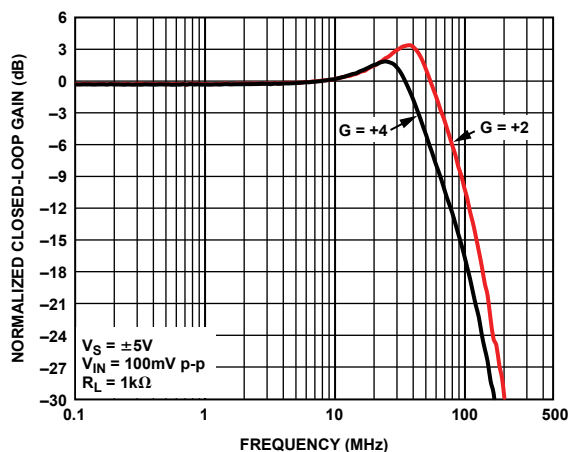


Figure 2. Frequency response of V_O2/V_IN.

Authors

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Designing a Low-Power Toxic Gas Detector

By Luis Orozco

Safety first! Many industrial processes involve toxic compounds, including chlorine for manufacturing plastics, agrochemical, and pharmaceutical products; phosphine and arsine for producing semiconductors; and hydrogen cyanide, released when burning consumer-packaging materials. It is important to know when dangerous concentrations exist.

In the United States, the [National Institute for Occupational Safety and Health](#) (NIOSH) and the [American Conference of Government Industrial Hygienists](#) (ACGIH) have established short- and long-term [exposure limits for many toxic industrial gases](#). The Threshold Limit Value-Time Weighted Average (TLV-TWA) is the TWA concentration to which most workers can be exposed repeatedly in an 8-hour day without adverse effect; the Threshold Limit Value-Short Term Exposure Limit (TLV-STEL) is the concentration to which most workers can be exposed continuously for a short period of time without irritation, damage, or impairment; and the Immediately Dangerous to Life or Health Concentration (IDLHC) is a limiting concentration that poses an immediate or delayed threat to life, that would cause irreversible adverse health effects, or that would interfere with an individual's ability to escape unaided. Table 1 shows limits for a few common gases.

Electrochemical sensors offer several advantages for instruments that detect or measure the concentration of toxic gases. Most sensors are gas-specific, have usable resolutions under one part per million of gas concentration, and operate with very small amounts of current, making them well suited for portable, battery powered instruments. One important characteristic of electrochemical sensors is their slow response: when first powered up, the sensor may take several minutes to settle to its final output value; and when exposed to a mid-scale step in gas concentration, the sensor may take 25 to 40 seconds to reach 90% of its final output value.

This article describes a portable carbon monoxide (CO) detector using an electrochemical sensor. The IDLH concentration for CO is much higher than for most other toxic gases, making it relatively safe to handle. Nevertheless, CO is still lethal, so use extreme care and appropriate ventilation when testing the circuit described here.



Figure 1. CO-AX carbon monoxide sensor.

Figure 1 shows a [CO-AX sensor](#) from [Alphasense](#). Table 2 shows a summary of the CO-AX sensor's specifications.

Table 2. CO-AX Sensor Specifications

Sensitivity	55 nA/ppm to 90 nA/ppm (65 typ)
Response Time (T ₉₀ from 0 ppm to 400 ppm CO)	< 30 s
Range (Guaranteed Performance)	0 ppm to 2,000 ppm
Overgas Limit	4,000 ppm

Achieving the longest possible battery life is the most important goal for portable instruments in this application, so keeping power consumption to a minimum is crucial. In typical low-power systems, the measurement circuitry powers up to make a measurement, then shuts down for a long standby period. In this application, however, the measurement circuit must remain continuously powered due to the electrochemical sensor's long time constants. Fortunately, the slow response allows the use of micropower amplifiers, high value resistors, and low-frequency filters that minimize Johnson noise and 1/f noise. In addition, single-supply operation avoids the wasted power of a bipolar supply.

Figure 2 shows the circuit of the portable gas detector. An [ADA4505-2](#) dual micropower amplifier is used in a [potentiostat](#) configuration (U2-A), and a transimpedance configuration (U2-B). The amplifier is a good choice for both potentiostat and transimpedance sections because its power dissipation and input bias current are extremely low. Consuming only 10 μ A per amplifier, it will permit a very long battery life.

Table 1. Exposure Limits for Some Common Industrial Toxic Gases

Toxic Gas	Long-Term Exposure Limit (TLV-TWA) (ppm)	Short-Term Exposure Limit (TLV-STEL) (ppm)	Immediate Danger to Life and Health Concentration (IDLHC) (ppm)
Carbon Monoxide	50	200	1,200
Carbon Dioxide	5,000	30,000	40,000
Chlorine	0.5	1	10
Phosphine	0.3	1	50
Hydrogen Sulfide	10	20	100

In 3-electrode electrochemical sensors, the target gas diffuses into the sensor through a membrane before interacting with the working electrode (WE). The potentiostat circuit senses the voltage at the reference electrode (RE) and supplies the counter electrode (CE) with the current required to maintain a constant voltage between the RE and WE terminals. No current flows in or out of the RE terminal, so the current flowing out of the CE terminal flows into the WE terminal. This current is directly proportional to the target gas concentration. The current through the WE terminal can be positive or negative, depending on whether reduction or oxidation takes place in the sensor. For carbon monoxide, oxidation occurs, causing the CE terminal current to be negative (current flows into the output of the potentiostat op amp). Resistor R4 is typically very small, so the voltage at the WE terminal is approximately equal to V_{REF} .

The current that flows into the WE terminal results in a negative voltage at the output of U2-A with respect to the WE terminal. This voltage is typically a few hundred millivolts for a carbon monoxide sensor, but can be as high as 1 V for other sensor types. To run from a single supply, an [ADR291](#) micropower reference, U1, raises the entire circuit 2.5 V above ground. The ADR291 consumes only 12 μ A; it can also provide the reference voltage for an analog-to-digital converter to digitize the output of this circuit.

The output voltage of the transimpedance amplifier is simply:

$$V_O = 2.5 \text{ V} + I_{WE} \times R_f \quad (1)$$

where:

I_{WE} is the current into the WE terminal.

R_f is the transimpedance resistor (shown as U4 in Figure 2).

The maximum response of the sensor is 90 nA/ppm, as shown in Table 2, and its maximum input range is 2,000 ppm. This results in a maximum output current of 180 μ A, and a maximum output voltage determined by the transimpedance resistor, as shown in Equation 2.

$$V_O = 2.5 \text{ V} + 2,000 \text{ ppm} \times 90 \text{ nA/ppm} \times R_f = 2.5 \text{ V} + 180 \mu\text{A} \times R_f \quad (2)$$

Sensors for different gases or from different manufacturers will have different current output ranges. Using an [AD5271](#) programmable rheostat for U4 instead of a fixed resistor makes it possible to maintain a single assembly and bill of materials for different gas sensors. In addition, it allows the product to have interchangeable sensors, since a microcontroller can set the AD5271 to the appropriate resistance value for each different gas sensor. The AD5271's 5-ppm/ $^{\circ}$ C temperature coefficient is better than most discrete resistors, and its 1- μ A supply current is a very small contributor to the system power consumption.

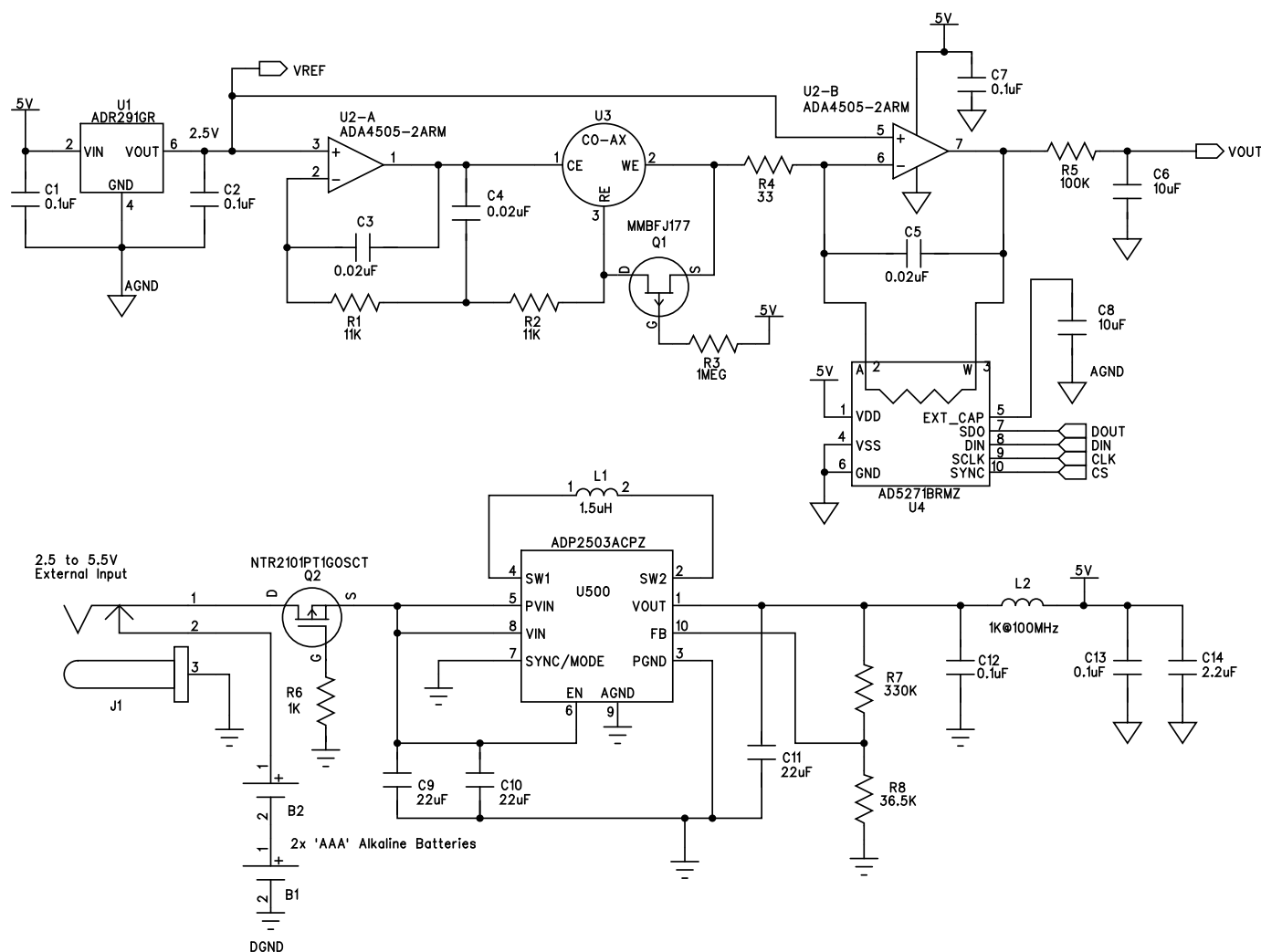


Figure 2. Portable gas detector using an electrochemical sensor.

When operating from a single 5-V supply, a 2.5-V range is available at the output of transimpedance amplifier U2-B, according to Equation 1. Setting the AD5271 to 12.5 k Ω takes advantage of the available range for worst-case sensor sensitivity, and allows for approximately 10% overrange capability.

Using the typical 65-nA/ppm sensor response, the output voltage can be translated to ppm of carbon monoxide as follows:

$$V_O = 2.5 \text{ V} + 813 \text{ } \mu\text{V/ppm} \quad (3)$$

With a differential input ADC, simply connect the 2.5-V reference output to the ADC's A_{IN-} terminal, eliminating the 2.5 V term in Equation 3.

Resistor R4 keeps the transimpedance amplifier's noise gain at reasonable level. The value of R4 is a compromise between the magnitude of the noise gain and the sensor's settling time error when exposed to high concentrations of gas. For this circuit, R4 = 33 Ω , which results in a noise gain of 380, as shown in Equation 4.

$$NG = 1 + \frac{12.5 \text{ k}\Omega}{33 \Omega} = 380 \quad (4)$$

The input noise of the transimpedance amplifier is multiplied by this gain. The ADA4505-2's 0.1 Hz to 10 Hz input voltage noise is 2.95 μV p-p, so the noise seen at the output will be

$$V_{\text{output_noise}} = 2.95 \text{ } \mu\text{V} \times NG = 1.1 \text{ mV p-p} \quad (5)$$

The output noise is equivalent to over 1.3 ppm p-p of gas concentration. This low-frequency noise is difficult to filter out. Fortunately, the sensor response is very slow, so the low-pass filter formed by R5 and C6 can have a cutoff frequency of 0.16 Hz. This filter has a time constant of one second, which is negligible compared to the sensor's 30-second response time.

Q1 is a P-channel JFET. When the circuit turns on, the gate is at V_{CC}, and the transistor is off. When the system powers off, the

gate drops to 0 V, and the JFET turns on to maintain the RE and WE terminals at the same potential. This greatly improves the turn-on settling time of the sensor when the circuit turns on again.

Two AAA batteries power the circuit. Using a diode for reverse-voltage protection would waste precious energy, so this circuit uses a P-channel MOSFET (Q2) instead. The MOSFET protects the circuit by blocking reverse voltages, and turns on when a positive voltage is applied. The MOSFET's on-resistance is less than 100 m Ω , causing a much smaller voltage drop than a diode. The ADP2503 buck-boost regulator allows the use of an external supply of up to 5.5 V as well as the AAA batteries. When operating in power-save mode, the ADP2503 consumes only 38 μA . The filter formed by L2, C12, and C13 removes any switching noise from the analog power rail. Rather than using a circuit to disconnect the batteries when an external power supply is connected, a jack that mechanically disconnects the batteries when plugging in the external power connector avoids waste of power.

The total current drawn from the AAA batteries is approximately 100 μA under normal conditions (no gas detected), and 428 μA under worst-case conditions (2,000 ppm CO detected). When the instrument is connected to a microcontroller that can enter a low-power standby mode while not making measurements, battery life can extend to over one year.

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(continued from Page 6)

Conclusions

In summary, integrated overvoltage protection provides many benefits:

1. Improved robustness and precision in analog signal chains.
2. Reduced time-to-market (TTM), shorter design time, and reduced testing requirements.
3. Reduced bill of materials (BOM) cost.
4. Fewer components required in approved component lists.
5. Reduced PCB footprint/higher density.
6. Lower failure rates.

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