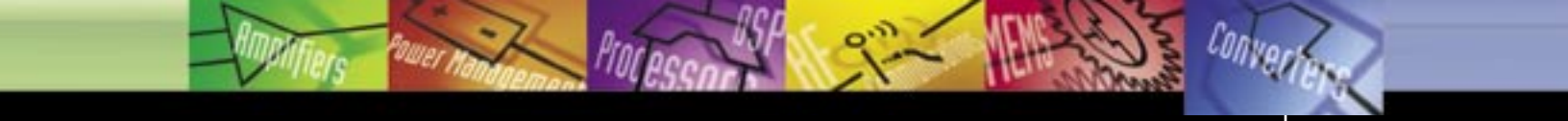
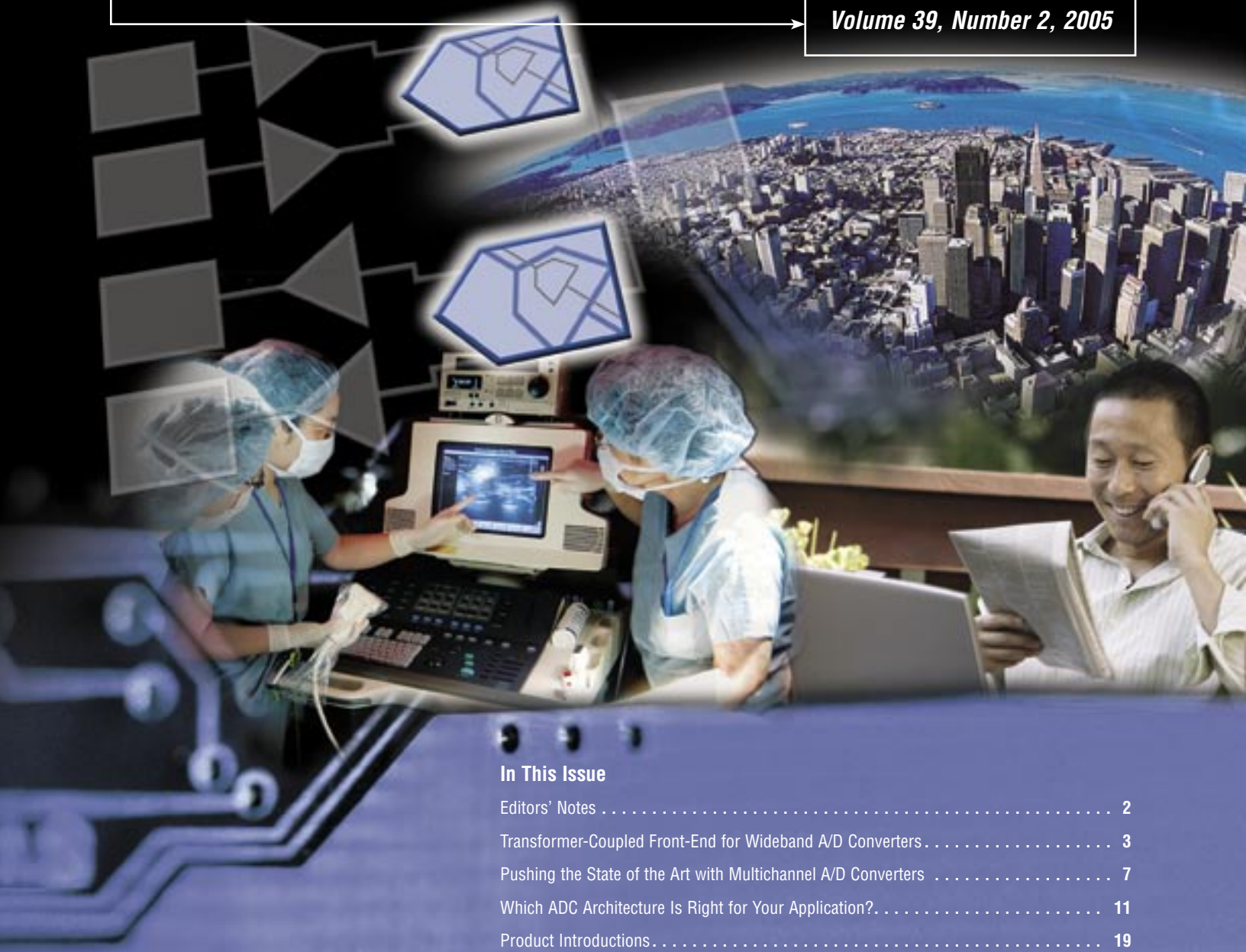


Analog Dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing

Volume 39, Number 2, 2005



In This Issue

ANALOG DEVICES
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Editors' Notes

DATA CONVERTERS

In 1969, the acquisition of Pastoriza Electronics launched ADI into the world of analog-to-digital and digital-to-analog converters. Hot products at the time were the ADC-F 10-bit, 1-μs A/D converter and the MDA-L 12-bit current-output D/A converter. Over the succeeding years, Analog Devices engineers have produced a series of breakthrough products, including the monolithic AD7520 10-bit CMOS DAC in 1974, DAC1138 18-bit modular DAC in 1977, and an endless stream of ICs: AD7541 12-bit multiplying DAC in 1978, AD574 complete 12-bit ADC in 1980, AD7546 16-bit DAC in 1981, AD9000 6-bit, 100-MHz ADC in 1984, AD671 12-bit, 2-MHz ADC in 1990, and AD771x 24-bit sigma-delta ADCs in 1992, to mention but a few of a great many firsts. Today, commanding a 45% share of the worldwide converter market, Analog Devices is the unquestioned leader in data-conversion technology.

To many engineers, op amps were—and data converters still are—a mystery, the latter combining the behavioral quirks of both analog and digital designs. Thus, from the first issue of *Analog Dialogue* in 1967 and the first printing of the *Analog-Digital Conversion Handbook* in 1972, Analog Devices has continually been a champion of education and training, augmenting its state-of-the-art converters with world-class data sheets, handbooks, magazines, and technical seminars. In this issue of *Analog Dialogue*, featuring data conversion, you'll read about some flagship ADCs, such as the multichip 12-bit, 500-MSPS AD12500 and 16-bit, 80-MSPS AD10678; and the monolithic 16-bit, 3-MSPS AD7621 and 18-bit, 2-MSPS AD7641. You'll also read about ADC architectures, learn how to choose an A/D converter to fit your application, and discover some tricks for designing a wideband transformer-coupled ADC front-end.

Scott Wayne [scott.wayne@analog.com]

PREMIUM PERFORMANCE (HUMAN)

At our 2005 General Technical Conference, significant awards were given to three outstanding Analog Devices technologists. Two new Fellows were named, and—in celebration of our 40th anniversary in business (1965-2005)—board chairman and co-founder, Ray Stata, named the recipient of the first Analog Devices Founder's Award. The details of the awards follow below.

Dan Sheingold [dan.sheingold@analog.com]

TWO NEW FELLOWS NAMED

Two ADI senior engineers, *Dr. Michael Coln* and *Dr. Katsu Nakamura*, were named to the distinguished position of ADI Fellow during the company's 2005 General Technology Conference (GTC), which attracted more than 1,500 engineers from the company's design sites worldwide.

The Fellows honor is awarded when an engineer has contributed significantly to ADI's business and demonstrated important qualities, such as innovation, leadership, entrepreneurial ability, and consulting skills. In addition, an ADI Fellow must be a company ambassador, bridging across organizations and demonstrating an unparalleled ability to teach and mentor others within the company. With the latest inductions, Analog Devices has a total of 30 Fellows out of more than 3,000 engineers worldwide.

"A commitment to engineering excellence is the lifeblood of Analog Devices, and the talent and dedication that Mike and Katsu bring to every project they undertake is testimony for that core belief," said Sam Fuller, vice president of research & development for ADI. "But what really singles them out is their constant innovation. It's this drive that solves our customers' problems, generates the revenue that enables ADI to maintain an aggressive R&D schedule, and sets inspirational goals for our employees." Between them, Coln and Nakamura have received 26 patents for inventions created at Analog Devices.

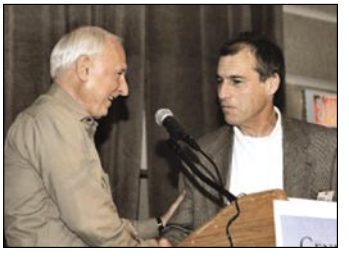
Mike Coln joined Analog Devices in 1988, after earning a Ph.D. from MIT. Since then, he has been involved in design, leadership, and mentoring roles, contributing to all areas of precision data converter development within the company. A holder of 12 patents (with another four in development), Coln was the chief architect of ADI's PulSAR® analog-to-digital-converter (ADC) family, which overcame perceived architectural barriers then boxing-in the specifications of speed, resolution, power consumption, and size of successive-approximation converters. The PulSAR self-calibrating architecture was the first to enable 16-bit ADCs to reach throughput of 1 MSPS (million samples per second), and it resulted in the first SAR ADC to reach 18-bit resolution.

Katsu Nakamura received his Ph.D. in Electrical and Computer Engineering from Carnegie Mellon University in 1994 before joining Analog Devices as a design engineer. He has been a pivotal force and the chief architect of technologies leading ADI to well over 50% share of the market for *analog front-ends* (AFEs) in digital still cameras. Nakamura, who holds 14 patents, guided ADI's migration of AFE technology to deep-submicron CMOS processes, integrating components formerly only available using bipolar manufacturing techniques.

The fifth generation of these products is now available with outstanding performance, integrated with complex digital circuitry. Our AFE customer list has grown to include all major camera manufacturers—among the most demanding in our industry for quality, performance, and price.

PulSAR® is a registered trademark of Analog Devices, Inc.

WINNER OF FIRST FOUNDER'S INNOVATION AWARD



In honor of our 40th anniversary, Analog Devices has established a new award, the *Founder's Innovation Award*. **Steve Sherman** was named as the first recipient of this award, at the 2005 GTC, by Ray Stata, ADI's co-founder (in 1965) and board chairman.

Every day, somewhere in the world, an airbag reliably deploys during a car crash and saves a life—thanks to the vision and determination of a certain Analog Devices employee. To honor the engineer who championed the development of *i*MEMS® (*integrated microelectromechanical systems*) technology and helped pioneer its application to automobile airbags, ADI awarded the first Founder's Innovation Award to Steve Sherman.

Announcing the award, Ray said: "It's really rare that the imagination, dedication, persistence, and innovative skills of a single individual would create an entirely new business—now with profitable sales of over $100 million, would have established ADI as the largest manufacturer of MEMS devices in the world, and would have gained for this company the recognition as a leader in that technology. It simply would not have happened at ADI if Steve did not passionately embrace and champion a vision of opportunity in an area outside of

continued on page 18

Analog Dialogue

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Analog Dialogue is the free technical magazine of Analog Devices, Inc., published continuously for 39 years—starting in 1967. It discusses products, applications, technology, and techniques for analog, digital, and mixed-signal processing. It is currently published in two editions—*online*, monthly at the above URL, and quarterly *in print*, as periodic retrospective collections of articles that have appeared online. In addition to technical articles, the online edition has timely announcements, linking to data sheets of newly released and pre-release products, and "Potpourri"—a universe of links to important and rapidly proliferating sources of relevant information and activity on the Analog Devices website and elsewhere. The *Analog Dialogue* site is, in effect, a "high-pass-filtered" point of entry to the **www.analog.com** site—the virtual world of *Analog Devices*. In addition to all its current information, the *Analog Dialogue* site has archives with all recent editions, starting from Volume 29, Number 2 (1995), plus three special anniversary issues, containing useful articles extracted from earlier editions, going all the way back to Volume 1, Number 1.

If you wish to subscribe to—or receive copies of—the print edition, please go to **www.analog.com/analogdialogue** and click on **<subscribe>**. Your comments are always welcome; please send messages to **dialogue.editor@analog.com** or to these individuals: *Dan Sheingold*, Editor **[dan.sheingold@analog.com]** or *Scott Wayne*, Managing Editor and Publisher **[scott.wayne@analog.com].**

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Transformer-Coupled Front-End for Wideband A/D Converters

By Rob Reeder [rob.reeder@analog.com]

INTRODUCTION

With the push into higher-frequency IF sampling, the analog inputs and overall front-end design of the A/D converter have become crucial elements of receiver design. Many applications are migrating to super-Nyquist sampling in order to eliminate a mix-down stage in the system design. Amplifiers pose a problem at these high frequencies, because high performance isn't as easy to achieve as in the Nyquist applications for which they are typically used. In addition, the amplifier's inherent noise will degrade the ADC's signal-to-noise ratio (SNR), no matter what input frequency is used. A transformer provides the designer with a relatively easy solution that resolves the noise issue, while providing a good coupling mechanism for high-frequency inputs.

The Transformer

Let us look at the basic makeup of a transformer and summarize what it provides to the user. First, the transformer is inherently ac-coupled, since it is galvanically isolated and will not pass dc levels. It provides the designer with basically noise-free gain, which depends on the designer's choice of turns ratio. The transformer also provides a quick and easy way of translating from a single-ended to a differential circuit. Finally, a center-tapped transformer provides the freedom to set the common-mode level arbitrarily. This combination of virtues reduces component count in front-end designs, where it is critical to keep complexity at a minimum.

However, care should be taken when using center-tapped transformers. If the converter circuit presents large imbalances between the differential analog inputs, a large amount of current could flow through the transformer's center tap, possibly saturating the core. For example, instability could result if V_{REF} is used to drive the center tap of the transformer, and a full-scale analog signal overdrives the ADC's input, turning on the protection diodes.

Although simple in appearance, transformers should not be taken lightly. There is much to know about and learn from them. Let's look at a simple model of the transformer and see what is "under the hood." A couple of simple equations relate the currents and voltages occurring at the terminals of an ideal transformer, as shown in Figure 1. When voltage is stepped up by a transformer, its impedance load will be reflected back to the input. The turns ratio, $a = N1/N2$, defines the ratio of primary voltage to secondary voltage; the currents are inversely related ($a = I2/I1$), and the ratio of the impedance seen in the primary reflected from the secondary goes as the square of the turns ratio ($Z1/Z2 = a^2$). The transformer's signal gain is expressed simply as 20 log (V2/V1) = 20 log $\sqrt{(Z2/Z1)}$, so a transformer with a voltage gain of 3 dB would have a 1:2 impedance ratio. That makes for an easy first step of the design.

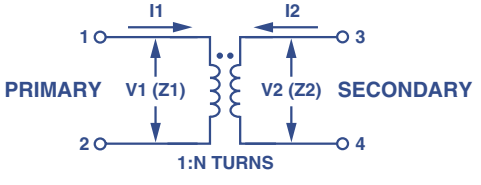

Figure 1a. Transformer input and output variables.

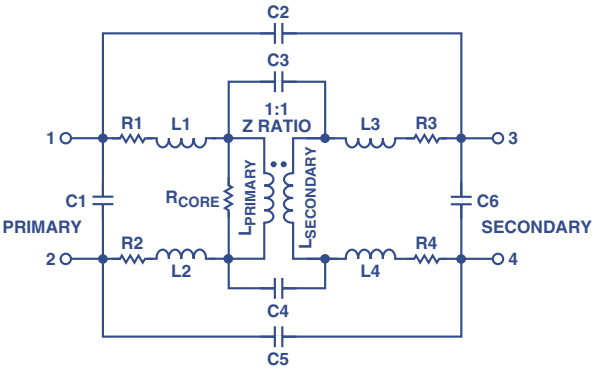

Figure 1b. Typical transformer model.

Figure 1b shows many of the inherent and parasitic departures from the ideal that come into play with a transformer. Each of these has a role in establishing the transformer's frequency response. They can help or hinder performance, depending on the front-end implementation. Figure 1b provides a good way to model a transformer to get first-order expectations. Some manufacturers provide modeling information, either on their website or through a support group. Anyone planning to do the model analysis using the hardware will need a network analyzer and a handful of samples to make all of the measurements properly.

Real transformers have losses and limited bandwidth. As the configuration of parasitics implies, one can think of a transformer as a wideband band-pass filter, which can be defined in terms of its –3-dB points. Most manufacturers will specify transformer frequency response in terms of the 1-, 2-, and 3-dB bandwidth. The amplitude response is accompanied by a phase characteristic. Usually a good transformer will have a 1%-to-2% phase imbalance over its frequency pass band.

Let us now consider some design examples involving a transformer-coupled front-end for an ADC. Since the transformer is used primarily for isolation and center-tapping, these examples will be simplified for discussion by using a unity turns ratio.

Examples

In the first example, shown in Figure 2, an AD6645[1] 14-bit, 80-MSPS ADC, with a differential input impedance of 1 kohm, is used. The 33-ohm series resistors provide isolation from transient currents in the input circuit of the ADC. The 501-ohm terminating resistor is chosen to achieve a 50-ohm input on the primary to match the 50-ohm analog input source. Thus

$$R_{in} = 58\Omega \,\|\, \left(66\Omega + \left(501\Omega \,\|\, 1000\Omega\right)\right) = 50.65\Omega \qquad (1)$$

The resistive combination in the transformer secondary is effectively in parallel with the 58-ohm resistor. The choice of terminating resistor depends on the desired input impedance. For simplicity, it will be assumed that a match to a 50-ohm source is required for all of the examples in this section.

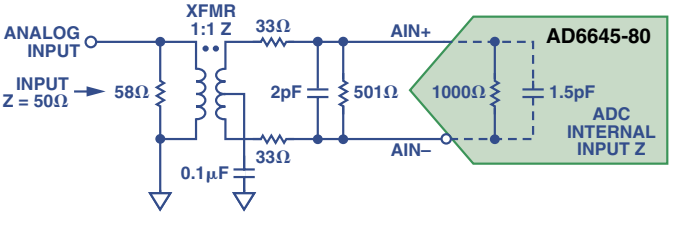

Figure 2. A 1:1 transformer coupling a 50-ohm input source with an ADC having a known input impedance.

This is an easy example because we assume that the input frequency is in baseband or first Nyquist zone. However, the situation is quite different if the front-end design is called on to handle a 100-MHz analog input. What happens in the transformer? With such a high IF frequency applied, any difference in parasitic capacitive coupling (C2–C5 in Figure 1b) unbalances the secondary outputs of the transformer. The resulting asymmetry gives rise to even-order distortions at the converter's analog input, which leads to 2nd-order harmonic distortions in the digital signal.

To illustrate this point, Figure 3 shows the voltages on the secondary when a 2-V p-p sinusoidal input is applied to the primary (100 MHz in Figure 3a and 200 MHz in Figure 3b). The secondary outputs are each expected to produce a 1-V p-p sine wave. But at 100 MHz, their amplitudes deviate by 10.5 mV p-p, with 0.5° phase imbalance. And at 200 MHz, the amplitude difference is 38 mV p-p, or 1.9%.

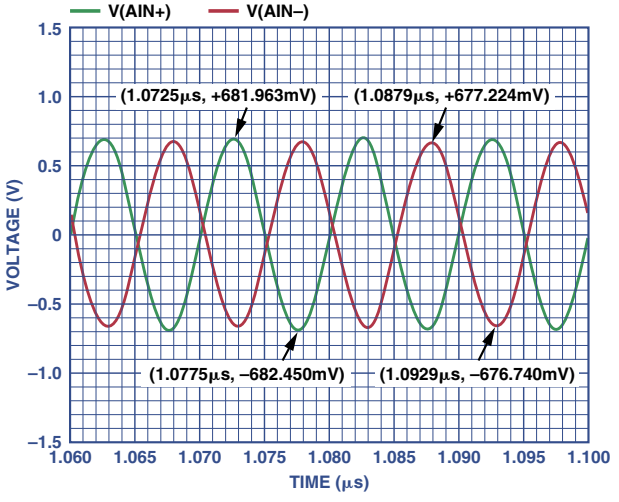

Figure 3a. 100-MHz input. Simulation of the transformer's secondary outputs: AIN+ (green) = 1.364 V p-p, AIN– (red) = 1.354 V p-p, Difference = 10.45 mV p-p.

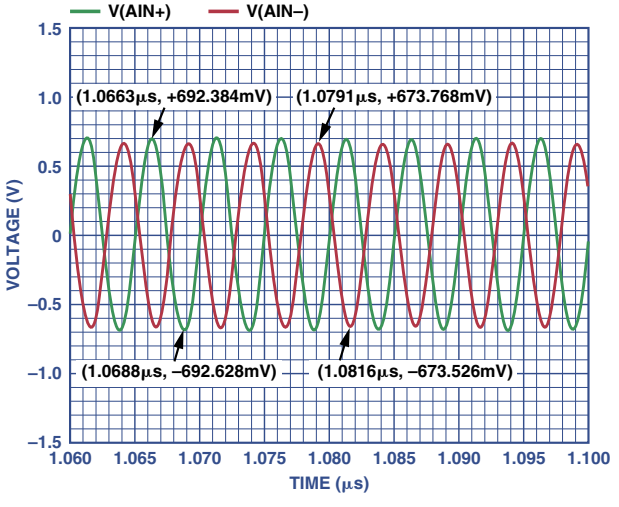

Figure 3b. 200-MHz input. Simulation of the transformer's secondary outputs: AIN+ (green) = 1.385 V p-p, AIN– (red) = 1.347 V p-p, Difference = 37.72 mV p-p.

One way to improve the situation is to apply a second transformer in cascade with the first to provide additional isolation and reduce the unbalanced capacitive feedthrough (Figure 4).

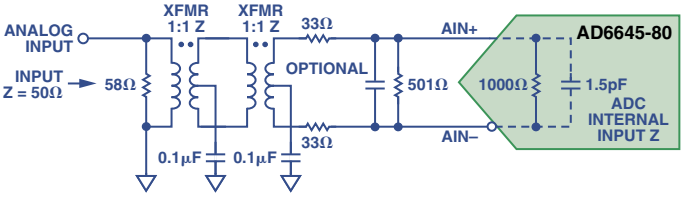

Figure 4. Cascaded transformers.

Using this scheme, the differential voltages applied to the converter are less likely to deviate from one another, particularly at high frequencies where this matters most. Figure 5 illustrates this point: the first transformer's secondary differences in parasitic coupling capacitances, C1 and C2, are reduced. The second transformer in cascade enables a redistribution of the core current lost and provides more equal signals to the primary of the second transformer. The two cascaded transformers in this configuration provide a better balanced solution for high frequencies.

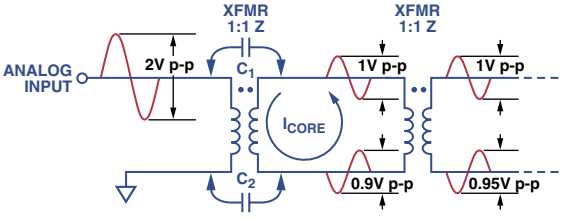

Figure 5. Two transformers in cascade improve signal balance.

The performance benefit can be seen in Figure 6 from the simulation. In Figure 6a, with an analog input of 100 MHz, the deviation drops to 0.25 mV p-p, or 0.013%. And at 200 MHz (Figure 6b), there is only a 0.88 mV p-p difference between the transformer's secondary outputs, or 0.044%. This is a big improvement, attained by adding one extra component.

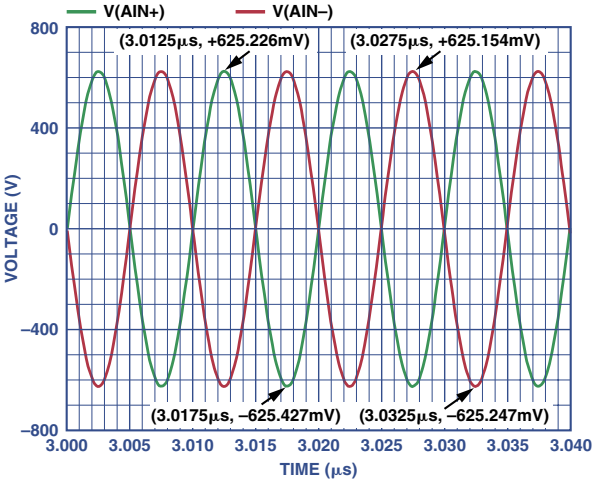

Figure 6a. 100 MHz. Simulation of the transformer's secondary outputs: AIN+ (green) = 1.25 V p-p, AIN– (red) = 1.25 V p-p, Difference = 0.25 mV p-p.

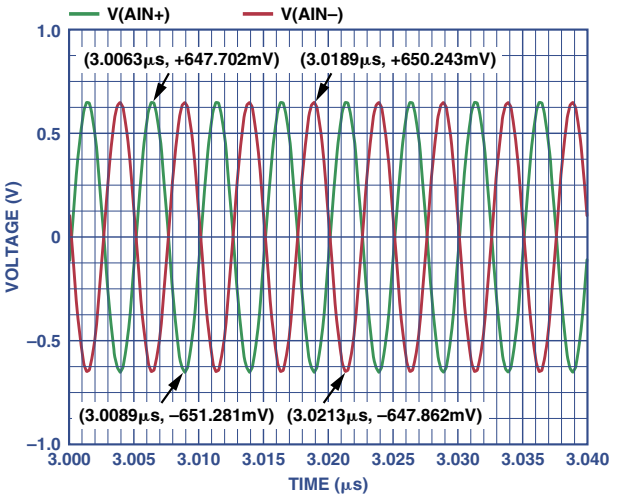

Figure 6b. 200 MHz. Simulation of the transformer's secondary outputs: AIN+ (green) = 1.298 V p-p, AIN– (red) = 1.298 V p-p, Difference = 0.88 mV p-p.

Another way to approach this is to use a two-balun type transformer configuration. A balun (balance-unbalance) acts like a transmission line and usually has greater bandwidth than the standard flux type transformers discussed earlier. They can provide good isolation between the primary and secondary with relatively low loss. However, they require more power to drive because the input impedance is halved from the primary to the secondary. Figure 7a shows a common implementation that is used in order to achieve a wide pass band. In Figure 7b, the balun type transformer is precompensated for the imbalance.

Response Peaking

Figure 8a shows a typical transformer frequency response, essentially that of a wideband filter with bandwidth in excess of 100 MHz. An inductor in series with the transformer's primary can be used to alter the bandwidth response of the transformer, by peaking the gain in the pass band and providing a steeper roll-off outside the pass band (Figure 8b). The inductor has the effect of adding a zero and a pole in the transfer function.

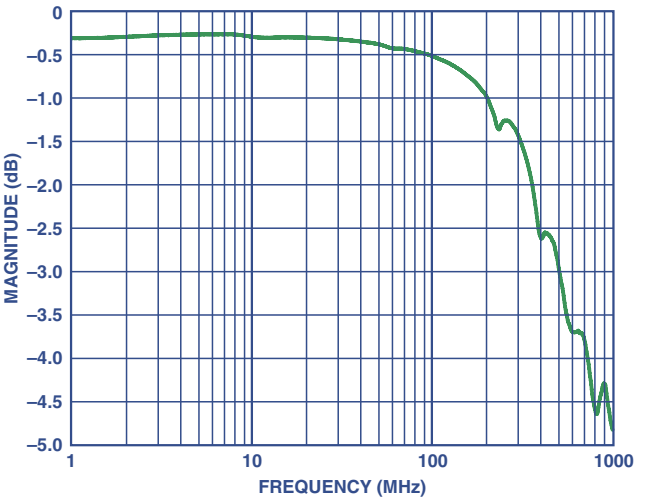

Figure 8a. Frequency response of a typical transformer.

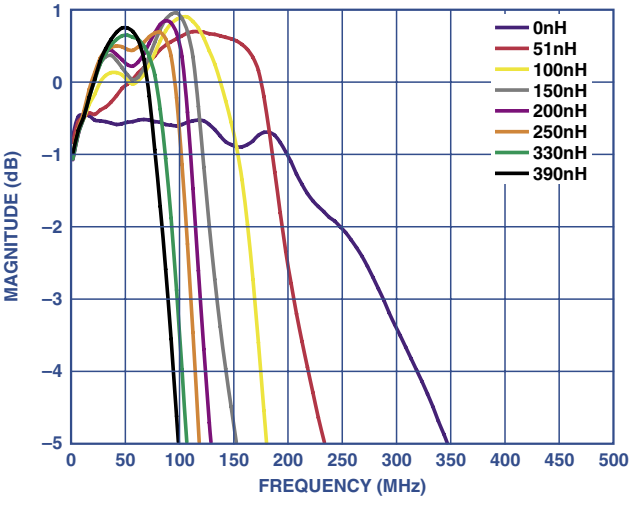

Figure 8b. Frequency response of a typical transformer with an inductor in series.

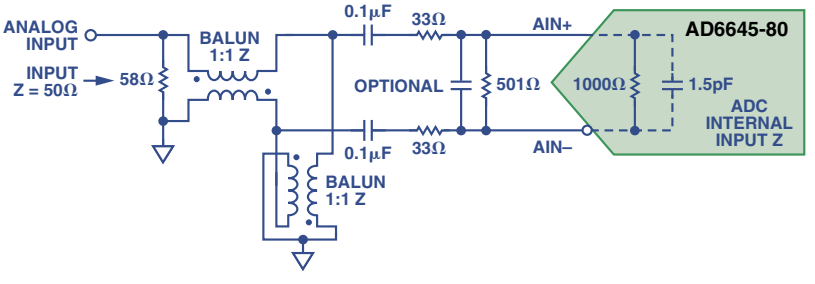

Figure 7a. Transformer-coupled input using a two-balun type transformer configuration.

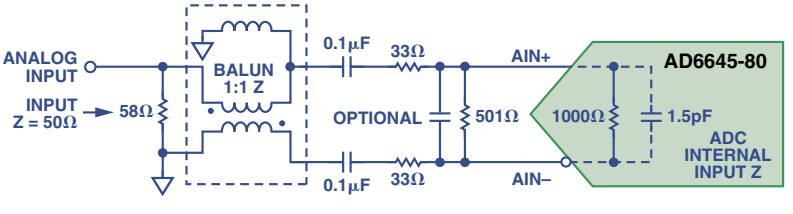

Figure 7b. Transformer-coupled input using a compensated-balun type transformer.

Figure 9 shows the circuit of Figure 2 with a series inductor. The value of inductance depends on the desired amount of peaking and bandwidth. However, the designer should note that this peaking could be undesirable where flatness of response and well-behaved phase response are important criteria.

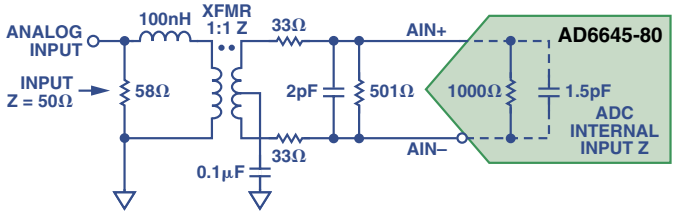

Figure 9. Inductor compensated 50-ohm input impedance with a 1:1 transformer and known ADC input impedance.

Switched-Capacitor ADCs

Up to this point we have only talked about interfacing ADCs with a known input impedance, using as an example the AD6645-80. But what about an ADC that has a switched-capacitor interface? Switched-capacitor ADCs have no internal buffer, so the user is making a connection directly with the internal sampling circuit—which has an impedance that varies widely with applied input frequency. In Figure 10, the A/D converter is the AD9236-80[2] with a 10-MHz analog input. In *track* (sample) mode, the input looks like a 4,135-ohm differential impedance in parallel with a 1.9 pF capacitor. But the *hold* mode will look different. Application Note AN-742[3] provides good information on getting these analog input impedance values. Many of ADI's switched-capacitor ADC values can be downloaded in spreadsheet form at the ADC's product page on the Analog Devices website, giving both *track-and-hold* values from 0.3 MHz to 1 GHz.

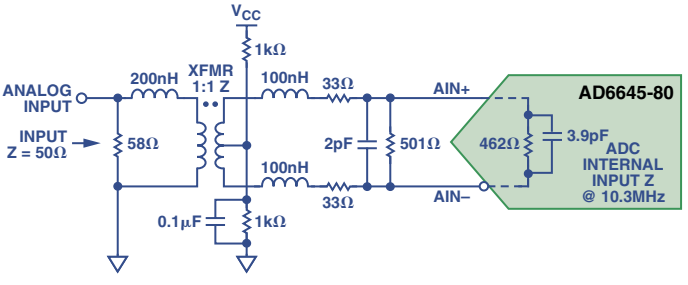

Figure 10. Switched-capacitor front-end implementation.

The 200-nH series inductance is meant to cancel out the reactance of the input capacitor that was reflected back from the ADC's input, making the input look as resistive as possible in order to achieve a good 50-ohm termination in the frequency band of interest. Note that other inductance values might be used to set the bandwidth and gain flatness desired, as seen in Figure 8b.

For all the examples discussed here, a 1:1 turns ratio (impedance ratio) was used. So the transformer provides a nominal voltage gain of 0 dB. This is the easiest type of transformer to configure, because the transformer's parasitics are relatively easy to understand and compensate for. However, some applications may require inherent voltage gain, when the input signals are low. Using a turns ratio of 1:2 or 1:4 (impedance ratio of 4 or 16), the transformer provides respective voltage gains of 6 dB or 12 dB.

The benefit here is that, unlike an amplifier, a transformer generates essentially no noise. However, the parasitics in a 1:2 or 1:4 transformer are much more difficult to compensate for, particularly over a wide range of frequencies. With a 1:2 turns ratio, for example, the capacitive terms quadruple while the inductive and resistive terms go down to one-fourth their original value. For a 1:4 turns ratio, the same terms go up or down by a factor of 16. The challenge is even more difficult when interfacing with a switched-capacitor-input ADC, because the capacitive terms are both large and variable with frequency. Considering the difficulties, the best way to undertake a design such as this is to optimize for the center frequency of interest within the given band.

CONCLUSION

An experienced designer will note that our discussion has focused largely on ideal circuit relationships and, while hinting at the turns-ratio and parasitic issues—and some of the architectural design approaches to dealing with them—we have only skimmed the surface. So what is to be done when tackling a new design? The designer needs to know as much as possible about the transformer selected for the design in relation to the ADC. The best way to do this in any front-end design is to investigate the parasitics that come into play over the frequencies of interest. Proper design and analysis involves the use of a network analyzer. It will show how the front-end design acts over a given frequency range with respect to impedance, VSWR, insertion loss, and differential phase mismatch—thus providing much key information on how the ADC will work in a transformer-coupled application.

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ACKNOWLEDGEMENTS

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[2] ADI website: www.analog.com (Search) AD9236 (GO)

[3] http://www.analog.com/UploadedFiles/Application_Notes/959283464AN742.pdf

Pushing the State of the Art with Multichannel A/D Converters

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Mark Looney [mark.looney@analog.com]
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INTRODUCTION

Like the rabbit decoy at dog races, the most demanding data-acquisition system requirements inherently stay ahead of commercial integrated-circuit analog-to-digital converter (ADC) performance. These extreme requirements have led to development—by both users and manufacturers—of many innovative "performance-enhancement" approaches that fulfill high-end data acquisition system needs while waiting for the next performance breakthrough.

One approach is to substantially increase sampling rate, reduce noise, or extend dynamic range by filling a converter "slot" with a design that uses more than one A/D conversion channel. This approach becomes increasingly practical as individual converter cost, size, and power requirements decrease for a given bandwidth and resolution, and as multiple converters are used (often packaged together) in a growing number of applications.

This article will discuss multichannel approaches using *signal averaging*, for increased resolution without loss of speed—and *time interleaving*, to increase sampling rates without loss of resolution. These approaches have resulted in products with improved specifications that embody these principles, such as the AD10678[1] 16-bit, 80-MSPS ADC—and the AD12500[2] 12-bit, 500-MSPS ADC.

Averaging

Signal-to-noise ratio (SNR), in dB, is a key performance metric for applications such as ultrasound and radar. The ADCs used in these systems can be affected by many external noise sources, including clock noise, power supply noise, and layout-induced digital noise coupling. As long as the square root of the sum of the squares (*root-sum-square*, or RSS) of noncorrelated noise sources is less than the inherent quantization noise of the ADC, output averaging can effectively lower the overall noise floor.

Systems requiring higher SNR often use digital post processors to sum the outputs of multiple ADC channels. The signals add directly, while noise from the individual ADCs—assumed to be uncorrelated—sums as the RSS, so summing improves the overall SNR. Summing the outputs of four ADCs improves the SNR by 6 dB, or 1 LSB. The AD6645[3] 14-bit, 80-MSPS ADC specifies an *effective number of bits* (ENOB) of 12. Figure 1 shows how four AD6645s can be summed to achieve two extra bits of resolution, and one extra bit of performance.

The input to each ADC consists of a signal term (V_S) and a noise term (V_N). Summing four noisy voltage sources results in a total voltage, V_T, which is the linear sum of the four signal voltages plus the RSS of the four noise voltages, i.e.,

$$V_T = V_{S1} + V_{S2} + V_{S3} + V_{S4} + \sqrt{V_{N1}^{\,2} + V_{N2}^{\,2} + V_{N3}^{\,2} + V_{N4}^{\,2}} \quad (1)$$

Since $V_{S1} = V_{S2} = V_{S3} = V_{S4}$, the signal has effectively been multiplied by four, while the converter noise—with equal rms values—has been multiplied by only two, thereby increasing the signal-to-noise ratio by a factor of two, or 6.02 dB. Thus, the 6.02-dB increase (ΔSNR) that results from summing four like signals gives rise to one additional bit of effective resolution. Since $SNR(\text{dB}) = 6.02N + 1.76$, where N is the number of bits,

$$N + \Delta N = \left[\frac{SNR(dB)}{6.02} - \frac{1.76}{6.02}\right] + \frac{6.02\,dB}{6.02} = N + 1 \quad (2)$$

Table I shows the increased SNR that results from summing the outputs of multiple ADCs. From the standpoint of simplicity, summing four ADCs is an obvious choice. Larger numbers may also be of interest in critical cases, but that would depend on other system specifications (including cost) and the amount of board space available.

Table I. Increase in SNR vs. Number of ADCs

Number of ADCs	Increase in SNR (dB)
2	3
4	6
8	9
16	12
32	15

The ideal SNR for a 14-bit ADC is (6.02 × 14) + 1.76 = 86.04 dB. The AD6645 data sheet specifies a typical SNR of only 74 dB, however, yielding an ENOB of 12 bits.

$$ENOB = \frac{(74 - 1.76)}{6.02} = 12\ bits \quad (3)$$

Thus, summing the outputs of four converters together recoups one extra bit, pushing the system-level ENOB to 13 bits (80 dB).

Systems like this require design effort, of course, in addition to system prototyping, qualification, and test development. The AD10678, however, integrates four AD6645s, a clock distribution system, and a complex programmable logic device (CPLD) that has been configured to provide a high-speed addition algorithm.

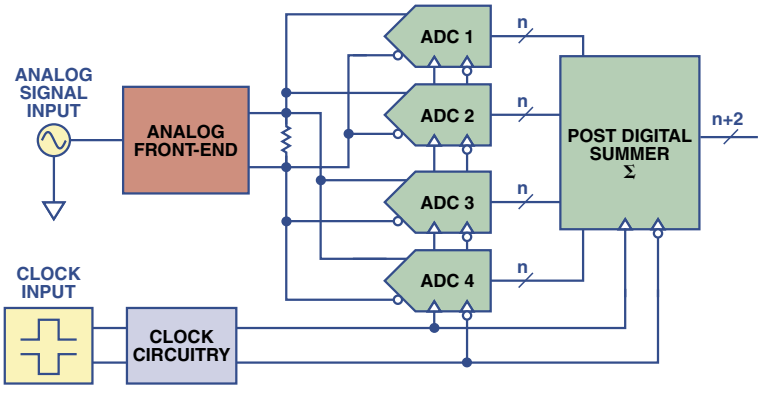

Figure 1. Summing four ADCs in parallel.

Fully tested and specified, the AD10678 is available—at a low cost—in a 2.2 × 2.8-inch PCB package. The FFT (fast Fourier-transform) plot shown in Figure 2 demonstrates the converter's excellent performance, providing 80.22-dB SNR with an 80-MSPS clock and 10-MHz analog input.

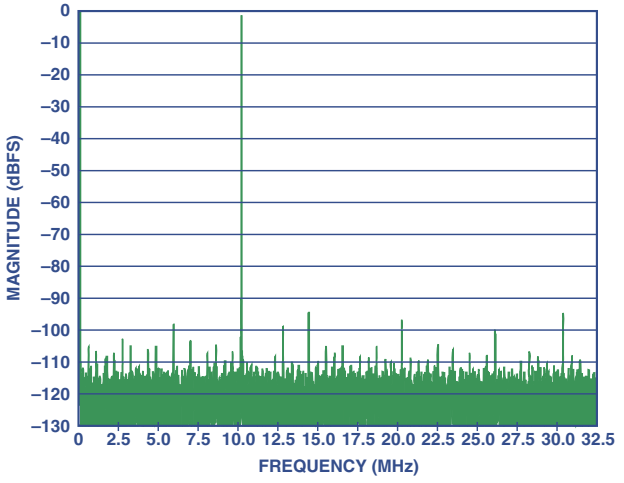

Figure 2. AD10678 FFT plot at an 80-MSPS encode rate and V_S = 10 MHz. SNR = 80.22 dBFS @ –1.33 dBFS.

In addition to the increased SNR, this architecture also provides improved dc accuracy. The offset and gain errors of the four devices are not correlated, so lower system offset and gain errors are achieved in the same way that noise is reduced. There is no improvement in linearity, however, and the *spurious-free dynamic range* (SFDR) of the system is actually dominated by the *worst* ADC.

The hardware for this implementation takes up more space on the PCB and dissipates four times the power, but it may still be advantageous to use this technique, compared to averaging the output of a single ADC that operates at four times the speed. Nevertheless, the increased number of signal samples at the higher speed will also serve to reduce normal-mode noise that arrives with the input signal. As processes improve, newer designs continue to push down the core power of the ADCs. Also, available quad and octal ADCs make multiple-ADC systems easier to implement and less space-intensive. The AD9229[4] quad 12-bit, 50-MSPS/65-MSPS ADC, for example, is available in a 48-LFCSP (7 mm × 7 mm) package. It dissipates only 300 mW per channel.

While it is feasible to improve specified SNR by standardizing on higher-level input voltages, this puts more stress on the design of the drive amplifier, and will degrade the *system-level* SNR, as both signal and noise will be amplified. A subtle benefit of the summing architecture is that the full-scale analog input doesn't have to be any larger than it would be with a single ADC.

Comparing hardware and software costs, the averaging approach may offer some benefits over digital filtering per se, but it can often make the job easier even when filtering is called for by overall system considerations that provide for cost-effective processing hardware and software.

Time Interleaving

Time interleaving of M ADCs allows the sample rate to be increased by the factor, M. By properly phasing each ADC's clock signal, the maximum sample rate of any standard integrated-circuit ADC type can be multiplied by the number of ADCs in the system. The proper clock phase required for each ADC can be calculated using the following relationship:

$$\phi_m = 2\pi\left(\frac{m-1}{M}\right), \text{where} \quad (4)$$

M = the number of ADCs

m is the specific ADC, i.e., $1 \le m \le M$

For example, a 4-channel system that employs the AD9444[5] 14-bit, 80-MSPS ADC, will create a 14-bit, 320-MSPS function when the individual clocks are properly sequenced in 90° (π/2) increments. Figure 3 captures the basic block diagram for this type of system. Time interleaving has already been leveraged for 12-bit integrated solutions in the AD12400[6]/AD12500 product family. Figure 4 displays the AD12500 block diagram, which includes all of the necessary ADCs, clock management, power supply, and digital post-processing functions.

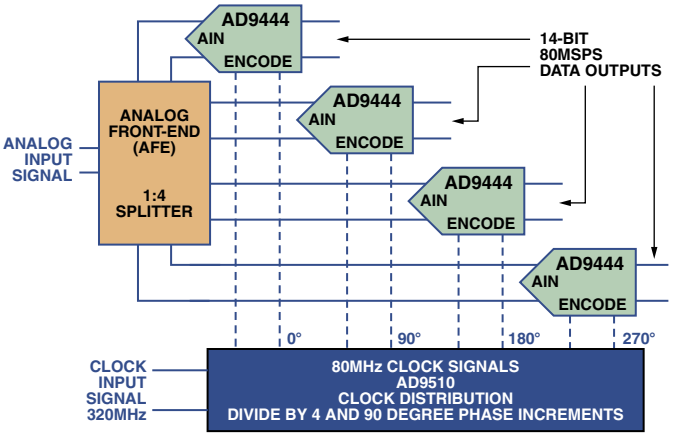

Figure 3. 4-channel time-interleaved ADC.

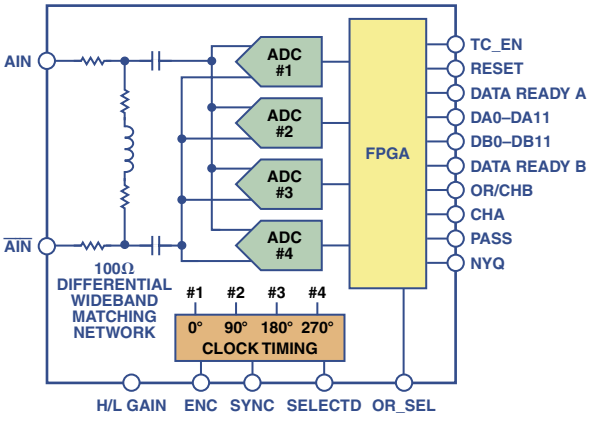

Figure 4. AD12500 block diagram.

The most obvious advantage of increasing the sample rate of an ADC system is the resulting increase in the analog sampling bandwidth, also known as the *Nyquist zone*. Increased Nyquist zones in digitizer systems offer numerous benefits: digital oscilloscopes achieve greater analog input bandwidth; software-defined radio systems increase the number of channels; and radar systems achieve greater spatial resolution. Figure 5 displays a simulated FFT plot for a 22-MHz tone on a 14-bit, 320-MSPS ADC system.

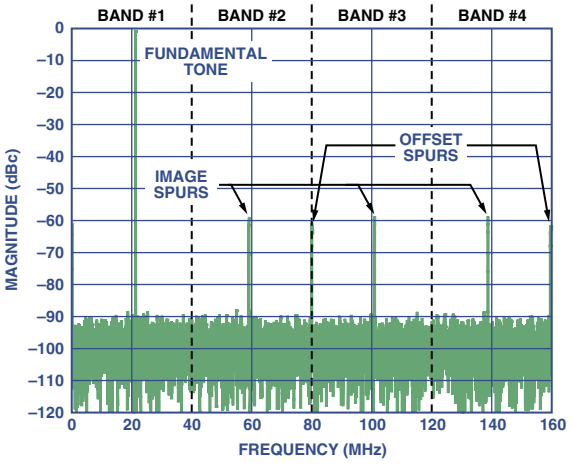

Figure 5. 4-channel time-interleaving FFT.

The FFT spectrum of this ADC system has a Nyquist zone of 160 MHz. For discussion purposes, the 160-MHz Nyquist zone can be split into four separate 40-MHz bands, each of which represents the Nyquist zone of a single AD9444 sampling at a rate of 80 MSPS. The fundamental tone of 22 MHz is in band #1. In addition to the fundamental tone, two types of nonharmonic distortion products can be observed in Figure 5—*offset spurs* and *image spurs*. The locations of these distortion products can be predicted for single-tone input signals with the following relationships:

$$f_{O1} = \frac{f_S}{4} \qquad f_{O2} = \frac{f_S}{2} \tag{5}$$

$$f_{X1} = \frac{f_S}{2} - f_{AIN} \qquad f_{X2,3} = \frac{f_S}{4} \pm f_{AIN} \tag{6}$$

These distortion products present a primary challenge associated with time interleaving. They are a direct result of channel-to-channel gain-, phase-, and offset-matching errors. In fact, the magnitude of these spurs is directly proportional to the magnitude of the errors.[7,8] For example, a 1% gain error in one channel would result in an image spur magnitude of 52 dBc. These spurs become problematic when a system's frequency plan involves the frequency bands in which the distortion resides. In such cases, the channel-to-channel matching behavior must be carefully managed in the development process.

If the system performance goal is 10-bit ENOB and the image spurs are the dominant factor, then the gain matching must be better than 0.1% and the phase matching must be better than 0.07 degrees (2 ps at 100 MHz)! From an implementation standpoint, many different error sources need to be reduced or eliminated to achieve this performance level.

The geometry of the traces from the analog and clock inputs of each ADC needs to be matched to ensure that the propagation delays are within their budgeted levels. While the clock function is relatively simple, it can also introduce errors that threaten these performance levels. Advanced technologies, such as silicon-germanium RSECL (*reduced-swing ECL*), can offer orders-of-magnitude improvement in rise-, fall-, and propagation-delay times when compared with those of their contemporary ECL counterparts. Depending on the input frequency, manual length trims may be used to overcome aperture delay errors as well.

Differences in power-supply-level behavior can create the need to use tight-tolerance supplies, such as linear regulators mounted in close proximity to the ADCs. Also, temperature-related behavior creates the need to manage the mechanical design to ensure tight temperature matching of the ADCs. The ADCs themselves may need to be screened for one or all of the following: gain, offset, aperture delay, and input-capacitance matching. Obviously screening four individual ADCs for tight tolerances in all their key parameters would be very difficult and costly! Such added complexity and increased risk must be weighed against the development and component cost goals of a system design.

For a narrow set of operating conditions, *an analog trim* process can be used to match ADC channels in time-interleaving ADC systems. But *digital post-processing* offers another approach to achieving tight channel-matching over a wider set of operating conditions. High-speed, configurable digital platforms, such as *field-programmable gate arrays* (FPGAs), have provided convenient vehicles for integrating advanced post-processing techniques—such as *Advanced Filter Bank* (AFB™).[9]

The AD12400 12-bit, 400-MSPS ADC comprises two high-speed ADCs, and leverages time interleaving and AFB to attain a level of performance that has not been achieved with individual commercial ADCs as of this writing. Figure 6 captures wide-bandwidth dynamic-range performance data, and compares analog and digital matching techniques. 14-bit matching (86 dBc) was achieved by "hand-tuning" the gain and phase for each channel at 128 MHz, but the performance degrades very quickly: 12-bit (74 dBc) performance is achieved for a bandwidth of only 20 MHz. On the other hand, when the digital matching is enabled, better than 12-bit performance is maintained over the entire 170-MHz test range—outstanding performance resulting from a well-designed digital post-processing technique.

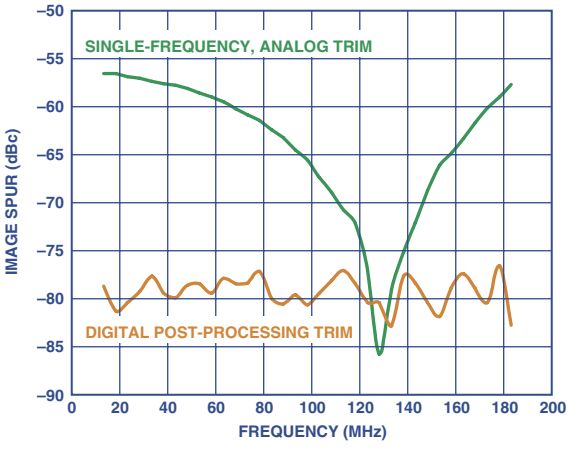

Figure 6. AD12400 wide-band image-spur performance.

Thus, when system designs require sample rates that are higher than commercially-available individual ADCs can handle, time interleaving is worth considering. If 10- to 12-bit performance is required over the entire Nyquist band, integrated solutions such as the AD12400 and AD12500 provide the benefits of time interleaving by successfully managing the difficulties associated with very tight channel-matching requirements.

Averaging vs. Time Interleaving

We have summarized here two techniques for achieving performance beyond the capability of currently available single ADCs. We've also shown examples of available high-performance multichip products achieved by using these techniques. The fact that such standard products are available—with design problems solved and standard specifications provided—may be sufficient for many readers. However, the following comments are for the benefit of users who may wish to further investigate the possibilities of these areas of performance using available standard single or multichannel uncommitted ADCs.

A common metric that can be used to compare topologies is SNR. If the AD9444 is the ADC of choice, and the system design calls for 40-MHz bandwidth and 79-dB typical SNR, one could consider both averaging and time interleaving. Both approaches would require the use of four AD9444 channels to achieve 5-to-6 dB of noise improvement over the AD9444's inherent SNR. Since both approaches can yield similar noise improvement, it's worth considering the secondary trade-offs to illustrate a typical design "trade-space."

First, the averaging approach will be less complex to implement than time interleaving. The clocks for the four ADCs in the averaging circuit can be derived from a resistive splitter, a magnetic splitter, or a simple 1:4 "fan-out" distribution IC. The time-interleaving approach requires the use of at least two D-type flip-flops to achieve the required division by 4 and 90° sequencing functions. In some cases, four additional flip-flops might be used to buffer the timing signal so as to maintain tight timing. In order to achieve the desired 6 dB SNR improvement, the time-interleaving approach is likely to employ a digital filter that requires real-time multipliers and adders (or a portion of processing time if available in the system design). The averaging approach only requires a real-time adder, resulting in a substantial reduction in digital logic.

The effectiveness of each noise-reduction technique must be carefully considered as well. In particular, the level of noise correlation and bandwidth in each channel must be understood. As the channel-to-channel noise correlation increases, the averaging approach becomes less effective. In systems for which the dominant noise source is jitter or phase noise, the noise-correlation risk can degrade the SNR improvement.

Time interleaving essentially spreads the noise over four times the bandwidth, then filters out the unused 120 MHz. In this case, the wideband characteristics of the noise spectrum must be studied and understood. If the spectral content of each channel's noise is uniformly distributed over the 160-MHz Nyquist band, this technique should yield a 6-dB SNR improvement. However, if the noise-energy distribution is more prominent within the 40-MHz band of interest, the SNR improvement goal of 6 dB might not be attainable.

Another important factor to consider when comparing these topologies is frequency planning. If a single-tone system is used, and the input frequency is above one-quarter of a single ADC's sample rate (20 MHz in the example), the 2nd, 3rd, 4th, 5th, and 6th harmonics fall outside of the 40-MHz band of interest. Therefore, they are reduced or removed altogether by the digital noise filter. In addition, the image spurs discussed above also fall outside of the band of interest and are thus filtered. In multitone systems, some of the components also fall out of the band of interest, lowering the total harmonic distortion of the system.

In conclusion, averaging offers a simpler approach to achieving 6 dB of noise improvement, but time interleaving offers several benefits that may warrant consideration when developing system architectures.

Uses of Multichannel Analog-to-Digital Converter Systems

Multichannel ADCs have played a substantial role in advancing data acquisition system performance. Ultrasound systems seeking higher definition sum up to 128 ADC channels for better signature. Digital oscilloscope manufacturers have developed ways to time interleave ADCs to accommodate their high sample rate requirements.[10,11] Other receiver systems have been able to use *frequency-division multiple access* (FDMA), employing multiple ADC channels to segment their frequency bands—reducing the input bandwidth requirements on each ADC and further increasing the dynamic range. As ADCs become increasingly available in multichannel integrated-circuit quad- and octal-type packages to save power and space, multiple-channel system architectures are being developed using them to provide functions or performance not previously available.

FOR FURTHER READING

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ACKNOWLEDGMENTS

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This article can be found at http://www.analog.com/library/analogdialogue/archives/39-05/multichannel.html, with a link to a PDF.

Which ADC Architecture Is Right for Your Application?

By Walt Kester [walt.kester@analog.com]

INTRODUCTION

Selecting the proper ADC for a particular application appears to be a formidable task, considering the thousands of converters currently on the market. A direct approach is to go right to the selection guides and parametric search engines, such as those available[1] on the Analog Devices website. Enter the sampling rate, resolution, power supply voltage, and other important properties, click the "find" button, and hope for the best. But it's usually not enough. How does one deal with a multiplicity of apparent "best choices"? Is there a way to approach the task with greater understanding—and better results?

Most ADC applications today can be classified into four broad market segments: (a) *data acquisition*, (b) *precision industrial measurement*, (c) *voiceband and audio*, and (d) *"high speed" (implying sampling rates greater than about 5 MSPS)*. A very large percentage of these applications can be filled by *successive-approximation* (SAR), *sigma-delta* (Σ-Δ), and *pipelined* ADCs. A basic understanding of these, the three most popular ADC architectures—and their relationship to the market segments—is a useful supplement to the selection guides and search engines.

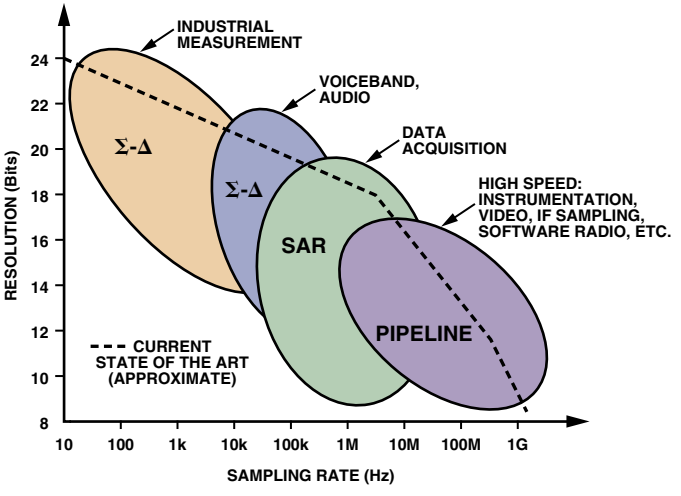

Figure 1. ADC architectures, applications, resolution, and sampling rates.

The classification in Figure 1 shows in a general way how these application segments and the associated typical architectures relate to ADC resolution (vertical axis) and sampling rate (horizontal axis). The dashed lines represent the approximate state of the art in mid-2005. Even though the various architectures have specifications with a good deal of overlap, the applications themselves are key to choosing the specific architecture required.

Successive-Approximation ADCs for Data Acquisition

The successive-approximation ADC is by far the most popular architecture for data-acquisition applications, especially when multiple channels require input multiplexing. From the modular and hybrid devices of the 1970s to today's modern low-power ICs, the successive-approximation ADC has been the workhorse of data-acquisition systems. The architecture was first utilized in experimental *pulse-code-modulation* (PCM) systems by Bell Labs in the 1940s. Bernard Gordon, at Epsco, introduced the first commercial vacuum-tube SAR ADC in 1954—an 11-bit, 50-kSPS ADC that dissipated 500 watts.

Modern IC SAR ADCs are available in resolutions from 8 bits to 18 bits, with sampling rates up to several MHz. At this writing, state-of-the-art performance of available devices is 16 bits at 3 MSPS (AD7621)[2] and 18 bits at 2 MSPS (AD7641)[3]. Output data is generally provided via a standard serial interface (I^2C® or SPI®, for example), but some devices are available with parallel outputs (at the obvious expense of increased pin count and package size).

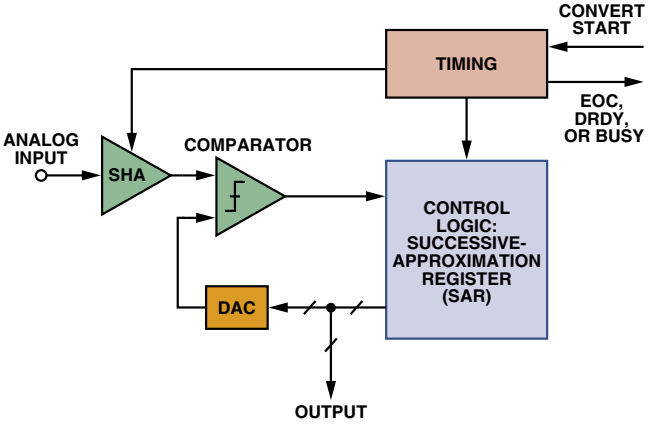

Figure 2. Basic successive-approximation (SAR) ADC.

The basic successive-approximation architecture is shown in Figure 2. In order to process rapidly changing signals, SAR ADCs have an input *sample-and-hold* (SHA) to keep the signal constant during the conversion cycle. The conversion starts with the internal *D/A converter* (DAC) set to midscale. The comparator determines whether the SHA output is greater or less than the DAC output, and the result (the *most-significant bit* (MSB) of the conversion) is stored in the *successive-approximation register* (SAR) as a 1 or a 0. The DAC is then set either to ¼ scale or ¾ scale (depending on the value of the MSB), and the comparator makes the decision for the second bit of the conversion. The result (1 or 0) is stored in the register, and the process continues until all of the bit values have been determined. At the end of the conversion process, a logic signal (EOC, DRDY, BUSY, etc.) is asserted. The acronym, *SAR*, which actually stands for *successive-approximation register*—the logic block that controls the conversion process—is universally understood as an abbreviated name for the entire architecture.

The timing diagram for a typical SAR ADC is shown in Figure 3. The functions shown are generally present in most SAR ADCs, but their exact labels can differ from device to device. Note that the data corresponding to that specific sample is available at the end of the conversion time, with no "pipeline" delay or "latency." This makes the SAR ADC easy to use in single-shot, burst-mode, and multiplexed applications.

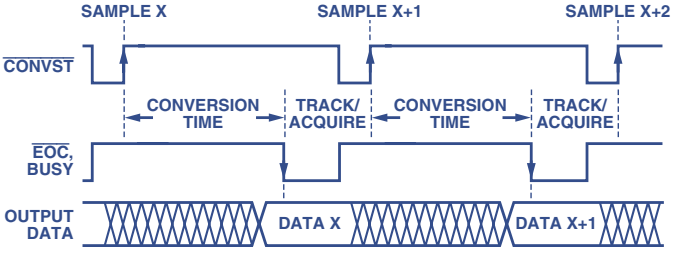

Figure 3. Simplified timing diagram of a SAR A/D converter.

The internal conversion process of most modern IC SAR ADCs is controlled by a high-speed clock (internal or external, depending on the ADC) that does not need to be synchronized to the CONVERT START input.

The basic algorithm used in the successive-approximation ADC conversion process can be traced back to the 1500s. It is related to the solution of a useful mathematical puzzle—the determination of an unknown weight by a minimal sequence of weighing operations (Reference 1). In this problem, as stated, the object is to determine the least number of weights which would serve to weigh an integral number of pounds from 1 lb. to 40 lbs. using a balance scale. One solution put forth by the mathematician Tartaglia in 1556, was to use the binary series of weights 1 lb., 2 lbs., 4 lbs., 8 lbs., 16 lbs., and 32 lbs. (or 2^0, 2^1, 2^2, 2^3, 2^4, and 2^5). The proposed weighing algorithm is the same one that is used in modern successive-approximation ADCs. (It should be noted that this solution will actually measure unknown weights up to 63 lbs. ($2^6 - 1$) rather than 40 lbs. as stated in the problem)*. The binary algorithm, using a balance scale, is shown in Figure 4 with an unknown weight of 45 lbs.

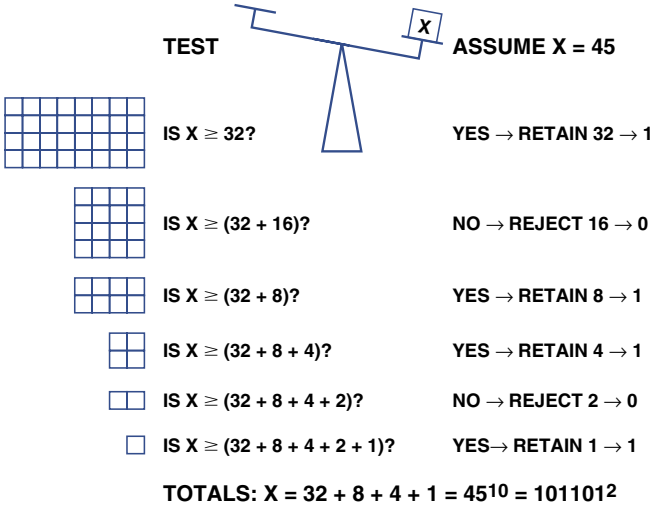

Figure 4. Successive-approximation ADC algorithm using balance scale and binary weights.

The overall accuracy and linearity of the SAR ADC are determined primarily by the internal DAC's characteristics. Early precision SAR ADCs, such as the industry-standard AD574,[4] used DACs with laser-trimmed thin-film resistors to achieve the desired accuracy and linearity. However, the process of depositing and trimming thin-film resistors adds cost, and the thin-film resistor values may be affected after the device is subjected to the mechanical stresses of packaging.

For these reasons, switched-capacitor (or *charge-redistribution*) DACs have become popular in newer CMOS-based SAR ADCs. The principal advantage of the switched-capacitor DAC is that the accuracy and linearity are primarily determined by high-accuracy photolithography, which establishes the capacitor plate area, hence the capacitance and the degree of matching. In addition, small capacitors can be placed in parallel with the main capacitors—to be switched in and out under control of autocalibration routines—to achieve high accuracy and linearity without the need for thin-film laser trimming. Because temperature tracking between the capacitors can be better than 1 ppm/°C, a high degree of temperature stability is achieved.

CMOS, the process of choice for modern SAR ADCs, is also the ideal process for *analog switches*. Therefore, input multiplexing can be added to the basic SAR ADC function relatively straightforwardly, thus allowing the integration of a complete data-acquisition system on a single chip. Additional digital functions are also easy to add to SAR-based ADCs, so features such as multiplexer sequencing, autocalibration circuitry, and more are becoming common.

Figure 5 illustrates the elements of the AD79x8 series of 1-MSPS SAR ADCs. The *sequencer* allows automatic conversion of the selected channels, or channels can be addressed individually if desired. Data is transferred via the serial port. SAR ADCs are popular in multichannel data-acquisition applications because they lack the "pipeline" delays typical in Σ-Δ and pipelined ADC architectures. The SAR ADC's conversion modes include "single-shot," "burst," and "continuous."

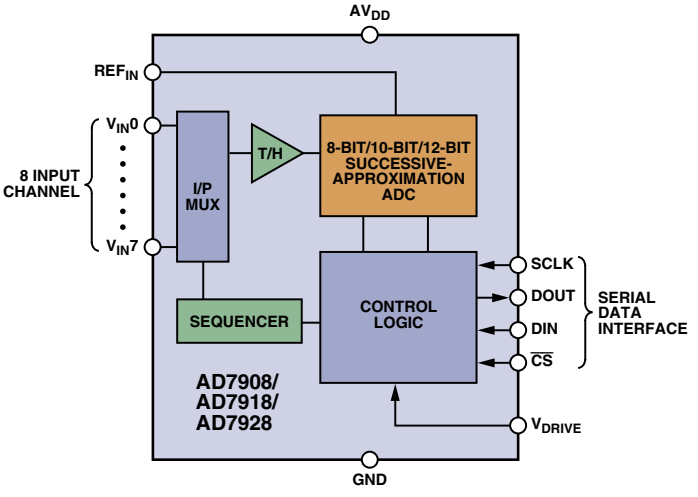

Figure 5. Functional block diagram of a modern 1-MSPS SAR ADC with 8-channel input multiplexer. Its family includes the AD7908[5] (8 bits), AD7918[6] (10 bits), and AD7928[7] (12 bits).

Sigma-Delta (Σ-Δ) *ADCs* for Precision Industrial Measurement and Instrumentation

Modern Σ-Δ ADCs have virtually replaced the integrating-type ADCs (dual-slope, triple-slope, quad-slope, etc.) for applications requiring high resolution (16 bits to 24 bits) and effective sampling rates up to a few hundred hertz. High resolution, together with on-chip programmable-gain amplifiers (PGAs), allows the small output voltages of sensors—such as weigh scales and thermocouples—to be digitized directly. Proper selection of sampling rate and digital filter bandwidth also yields excellent rejection of 50-Hz and 60-Hz power-line frequencies. Σ-Δ ADCs offer an attractive alternative to traditional approaches using an instrumentation amplifier (in-amp) and a SAR ADC.

The basic concepts behind the Σ-Δ ADC architecture originated at Bell Labs in the 1950s—in work done on experimental digital transmission systems utilizing delta modulation and differential PCM. By the end of the 1960s, the Σ-Δ architecture was well understood. However, because digital filters (then a rarity) were

*Note that if *ternary* (base-3: 1,0,–1) logic is permitted, the problem can be solved in four steps, with weights of 1 lb., 3 lbs., 9 lbs., and 27 lbs. applied on either side of the balance. Indeed, 40 lbs. is then maximum with these weights.

an integral part of the architecture, practical IC implementations did not appear until the late 1980s, when signal processing in digital CMOS became widely available. The basic concepts used in Σ-Δ—*oversampling, noise shaping, digital filtering, and decimation*—are illustrated in Figure 6.

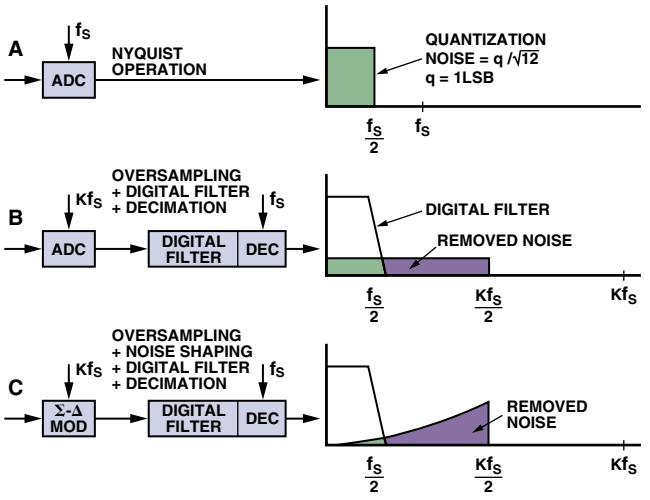

Figure 6. Noise-spectrum effects of the fundamental concepts used in Σ-Δ: oversampling, digital filtering, noise shaping, and decimation.

Figure 6A shows a noise spectrum for traditional "Nyquist" operation, where the ADC input signal falls between dc and $f_S/2$, and the quantization noise is uniformly spread over the same bandwidth. In Figure 6B, the sampling frequency has been increased by a factor, *K*, (the *oversampling* ratio), but the input signal bandwidth is unchanged. The quantization noise falling outside the signal bandwidth is then removed with a digital filter. The output data rate can now be reduced (*decimated*) back to the original sampling rate, f_S. This process of oversampling, followed by digital filtering and decimation, increases the SNR within the Nyquist bandwidth (dc to $f_S/2$). For each doubling of *K*, the SNR within the dc-to-$f_S/2$ bandwidth increases by 3 dB. Figure 6C shows the basic Σ-Δ architecture, where the traditional ADC is replaced by a Σ-Δ modulator. The effect of the modulator is to shape the quantization noise so that most of it occurs outside the bandwidth of interest, thereby greatly increasing the SNR in the dc-to-$f_S/2$ region.

The basic first-order Σ-Δ ADC is shown in Figure 7, with the Σ-Δ modulator shown in some detail.

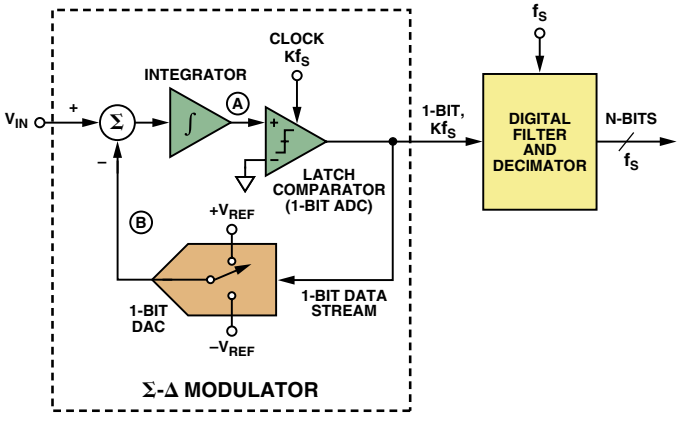

Figure 7. First-order sigma-delta ADC.

The heart of this basic modulator is a 1-bit ADC (comparator) and a 1-bit DAC (switch). Although there are a number of multibit Σ-Δ ADCs, those using the single-bit modulator have the obvious advantage of inherently excellent differential linearity.

The output of the modulator is a 1-bit stream of data. Because of negative feedback around the integrator, the average value of the signal at B must equal V_{IN}. If V_{IN} is zero (i.e., midscale), there are an equal number of 1s and 0s in the output data stream. As the input signal goes more positive, the number of 1s increases, and the number of 0s decreases. Likewise, as the input signal goes more negative, the number of 1s decreases, and the number of 0s increases. The ratio of the 1s in the output stream to the total number of samples in the same interval—the *ones density*—must therefore be proportional to the dc value of the input.

The modulator also accomplishes the *noise-shaping* function by acting as a low-pass filter for the signal and a high-pass filter for the quantization noise. Note that the digital filter is an integral part of the Σ-Δ ADC, and it can be optimized to give excellent 50-Hz/60-Hz power-frequency rejection. However, the digital filter does introduce inherent *pipeline delay*, which definitely must be considered in multiplexed and servo applications. If signals are multiplexed into a Σ-Δ ADC, the digital filter must be allowed to settle to the new value before the output data is valid. Several output clock cycles are generally required for this settling. Because of the pipeline delay of the digital filter, the Σ-Δ converter cannot be operated in a "single-shot" or "burst" mode.

Although the simple first-order single-bit Σ-Δ ADC is inherently linear and monotonic because of the 1-bit ADC and 1-bit DAC, it does not provide sufficient noise shaping for high-resolution applications. Increasing the number of integrators in the modulator (similar to adding poles to a filter) provides more noise shaping at the expense of a more complex design—as shown in Figure 8 for a second-order 1-bit modulator. Note the improvement in the noise shaping characteristic compared to a first-order modulator. Higher-order modulators (greater than third order) are difficult to stabilize and present significant design challenges.

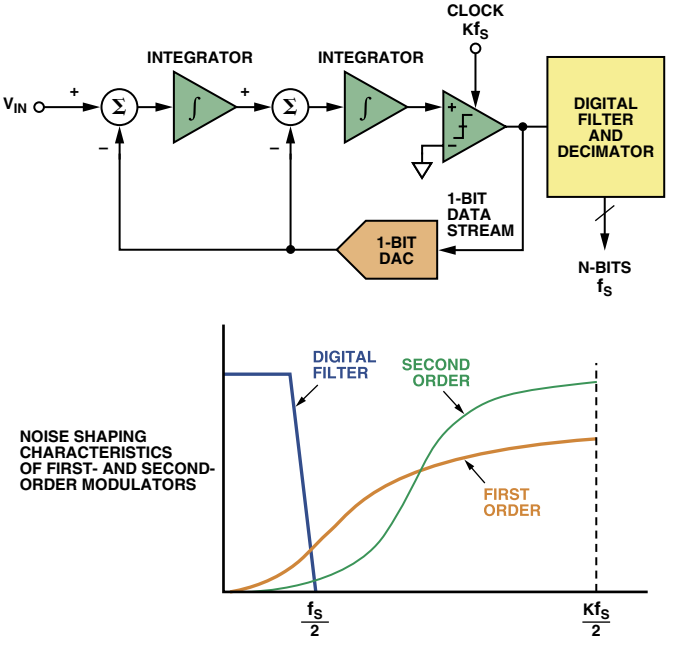

Figure 8. Second-order Σ-Δ modulator.

A popular alternative to higher-order modulators is to use a *multibit* architecture, where the 1-bit ADC (comparator) is replaced with an *N*-bit flash converter, and the single-bit DAC (switch) is replaced with a highly linear *N*-bit DAC. Expensive laser trimming in multibit Σ-Δ ADCs can be avoided by using techniques such as data scrambling to achieve the required linearity of the internal ADC and DAC.

While integrating architectures (dual-slope, triple-slope, etc.) are still used in applications such as digital voltmeters, the CMOS Σ-Δ ADC is the dominant converter for today's industrial measurement applications. These converters offer excellent power-line common-mode rejection and resolutions up to 24 bits as well as digital conveniences such as on-chip calibration. Many have programmable-gain amplifiers (PGAs), which allow small signals from bridge- and thermocouple transducers to be directly digitized without the need for additional external signal conditioning circuits and in-amps.

Figure 9 shows a simplified diagram of a precision load cell. This particular load cell produces 10-mV full-scale output voltage for a load of 2 kg with 5-V excitation.

The bridge's common-mode output voltage is 2.5 V. The diagram shows the bridge resistance values for a 2-kg load. The output voltage for any given load is directly proportional to the excitation voltage, i.e., it is ratiometric with the supply voltage.

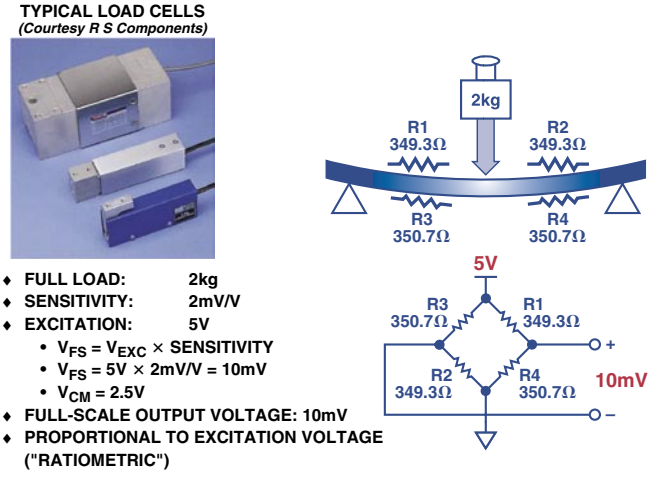

Figure 9. Load-cell signal-conditioning application.

A traditional approach to digitizing this low-level output would be to use an instrumentation amplifier to provide the necessary gain to drive a conventional SAR ADC of 14-bit to 18-bit resolution. Because of offset and drift considerations, an "auto-zero" in-amp such as the AD5555[8] or AD8230[9] is required. Appropriate filtering circuitry is needed due to the noise of the auto-zero in-amp. In addition, the output data from the SAR ADC is often averaged for further noise reduction.

An attractive alternative to the traditional in-amp/SAR ADC approach is shown in Figure 10, which uses a direct connection between the load cell and the AD7799[10] high resolution Σ-Δ ADC. The full-scale bridge output of 10 mV is digitized to approximately 16 "noise-free" bits by the ADC at a throughput rate of 4.7 Hz. (For more discussion on input-referred noise and noise-free code resolution see Further Reading #1). Ratiometric operation eliminates the need for a precision voltage reference.

The Σ-Δ ADC is an attractive alternative when very low-level signals must be digitized to high resolution—but the user should understand that the Σ-Δ ADC is more digitally intensive than the SAR ADC and may therefore require a somewhat longer development cycle. Evaluation boards and software can greatly assist in this process. Nevertheless, there are still many instrumentation and sensor signal-conditioning applications that can be efficiently solved with a traditional in-amp (for signal amplification and common-mode rejection) followed by a multiplexer and a SAR ADC.

Sigma-Delta ADCs for Voiceband and Audio

In addition to providing attractive solutions for a variety of industrial measurement applications—precision measurement, sensor monitoring, energy metering, and motor control—the Σ-Δ converter dominates modern voiceband and audio applications. A major benefit of the high oversampling rate inherent in Σ-Δ converters is that they simplify the input antialiasing filter for the ADC and the output anti-imaging filter for the DAC. In addition, the ease of adding digital functions to a CMOS-based converter makes features such as digital-filter programmability practical with only small increases in overall die area, power, and cost.

Digital techniques for voiceband audio began in the early days of PCM telecommunications applications in the 1940s. The early T-carrier systems used 8-bit companding ADCs and expanding DACs, and a sampling frequency of 8 kSPS became the early standard.

Modern digital cellular systems utilize higher-resolution oversampled linear Σ-Δ ADCs and DACs rather than the lower-resolution companding technique. Typical SNR requirements are 60 dB to 70 dB. If companding/expanding is required for compatibility with older systems, it is done in the DSP hardware or software. Voiceband "codecs"[11] (coder/decoders) having many applications other than PCM, such as speech processing, encryption, etc., are available in a variety of types.

Sigma-delta ADCs and DACs also dominate the more demanding audio markets, including, for example, FM stereo, computer audio, stereo compact disc (CD), digital audio tape (DAT), and DVD audio. *Total harmonic distortion plus noise* (THD + N) requirements range from 60 dB to greater than 100 dB, and sampling rates range from 48 kSPS to 192 kSPS. Modern CMOS Σ-Δ ADCs and DACs can meet these requirements and also provide the additional digital functions usually associated with such applications.

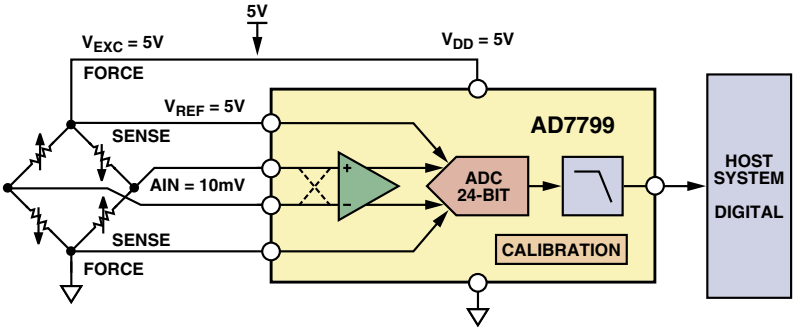

Figure 10. Load-cell signal conditioning using the AD7799 high-resolution Σ-Δ ADC.

Pipelined ADCs for High-Speed Applications (Sampling Rates Greater than 5 MSPS)

In this article, we arbitrarily define any application requiring a sampling rate of greater than 5 MSPS as "high speed." Figure 1 shows that there is an area of overlap between SAR and pipelined ADCs for sampling rates between approximately 1 MSPS and 5 MSPS. Except for this small region, the applications considered *high speed* are most often served by a pipelined ADC. Today, the low-power CMOS pipelined converter is the ADC of choice, not only for the video market but for many others as well. This contrasts strongly with the 1980s, when these markets were served by either the IC flash converter (which dominated the 8-bit video market with sampling rates between 15 MSPS and 100 MSPS) or the higher-resolution, more expensive modular/hybrid solutions. Although low-resolution flash converters remain an important building block for the pipelined ADC, they are rarely used by themselves, except at extremely high sampling rates—generally greater than 1 GHz or 2 GHz—requiring resolutions no greater than 6 bits to 8 bits.

Today, markets that require "high-speed" ADCs include many types of *instrumentation* applications (digital oscilloscopes, spectrum analyzers, and medical imaging). Also requiring high-speed converters are video, radar, *communications* (IF sampling, software radio, base stations, set-top boxes, etc.), and *consumer electronics* (digital cameras, display electronics, DVD, enhanced-definition TV, and high-definition TV).

The pipelined ADC has its origins in the *subranging* architecture, first used in the 1950s. A block diagram of a simple 6-bit, two-stage subranging ADC is shown in Figure 11.

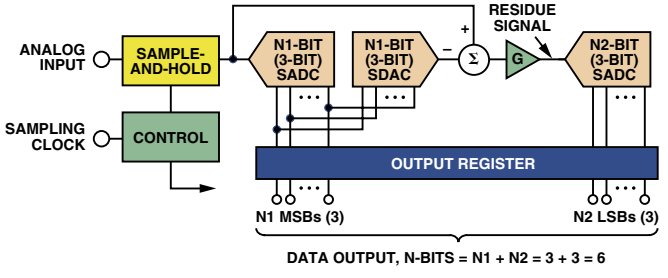

Figure 11. 6-bit, two-stage subranging ADC.

The output of the SHA is digitized by the first-stage 3-bit sub-ADC (SADC)—usually a flash converter. The coarse 3-bit MSB conversion is converted back to an analog signal using a 3-bit sub-DAC (SDAC). Then the SDAC output is subtracted from the SHA output, the difference is amplified, and this "residue signal" is digitized by a second-stage 3-bit SADC to generate the three LSBs of the total 6-bit output word.

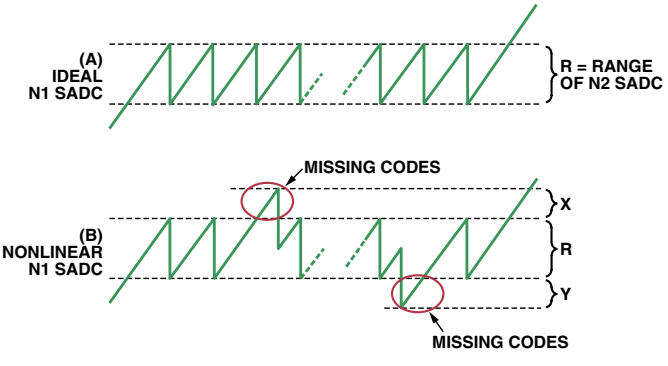

Figure 12. Residue waveform at input of second-stage SADC.

This subranging ADC can best be evaluated by examining the "residue" waveform at the input to the second-stage ADC, as shown in Figure 12. This waveform is typical for a low-frequency ramp signal applied to the analog input of the ADC. In order for there to be no missing codes, the residue waveform must not exceed the input range of the second-stage ADC, as shown in the ideal case of Figure 12A. This implies that both the N1-bit SADC and the N1-bit SDAC must be accurate to better than N1 + N2 bits. In the example shown, N1 = 3, N2 = 3, and N1 + N2 = 6. The situation shown in Figure 12B will result in missing codes when the residue waveform goes outside the range of the N2 SADC, "R," and falls within the "X" or "Y" regions—which might be caused by a nonlinear N1 SADC or a mismatch of interstage gain and/or offset. The ADC output under such conditions might appear as in Figure 13.

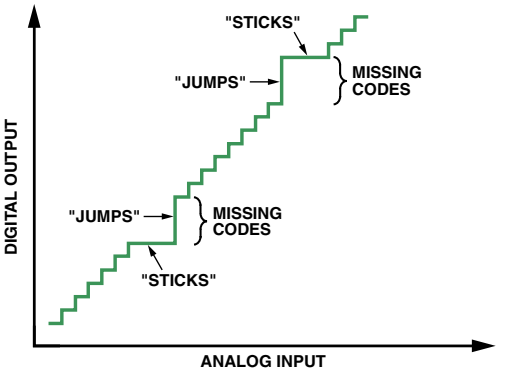

Figure 13. Missing codes due to MSB ADC nonlinearity or interstage misalignment.

This architecture, as shown, is useful for resolutions up to about 8 bits (N1 = N2 = 4); however maintaining better than 8-bit alignment between the two stages (over temperature variations, in particular) can be difficult. At this point it is worth noting that there is no particular requirement—other than certain design issues beyond the scope of this discussion—for an equal number of bits per stage in the subranging architecture. In addition, there can be more than two stages. Nevertheless, the architecture as shown in Figure 11 is limited to approximately 8-bit resolution unless some form of error correction is added.

The *error-corrected subranging* ADC architecture appeared in the mid-1960s as an efficient means to achieve higher resolutions, while still utilizing the basic subranging architecture. In the two-stage, 6-bit subranging ADC, for example, an extra bit is added to the second-stage ADC which allows the digitization of the regions shown as "X" and "Y" in Figure 12. The extra range in the second-stage ADC allows the residue waveform to deviate from its ideal value—provided it does not exceed the range of the second-stage ADC. However, the internal SDAC must still be accurate to more than the overall resolution, N1 + N2.

A basic 6-bit subranging ADC with error correction is shown in Figure 14, with the second-stage resolution increased to 4 bits, rather than the original 3 bits. Additional logic, required to modify the results of the N1 SADC when the residue waveform falls in the "X" or "Y" overrange regions, is implemented with a simple adder in conjunction with a dc offset voltage added to the residue waveform. In this arrangement, the MSB of the second-stage SADC controls whether the MSBs are incremented by 001 or passed through unmodified.

It's worth noting that more than one correction bit can be used in the second-stage ADC, a trade-off—part of the converter design process—beyond the scope of this discussion.

The *error-corrected subranging* ADC shown in Figure 14 does not have a pipeline delay. The input SHA remains in the *hold* mode during the time required for the following events to occur: the first-stage SADC makes its decision, its output is reconstructed by the first-stage SDAC, the SDAC output is subtracted from the SHA output, amplified, and digitized by the second-stage SADC. After the digital data passes through the error correction logic and output registers, it is ready for use; and the converter is ready for another sampling-clock input.

In order to increase the speed of the basic subranging ADC, the "pipelined" architecture shown in Figure 15 has become very popular. This pipelined ADC has a *digitally corrected subranging* architecture—in which each of the two stages operates on the data for one-half of the conversion cycle, and then passes its residue output to the next stage in the "pipeline" prior to the next phase of the sampling clock. The interstage track-and-hold (T/H) serves as an analog delay line—it is timed to enter the hold mode when the first-stage conversion is complete. This allows more settling time for the internal SADCs, SDACs, and amplifiers, and allows the pipelined converter to operate at a much higher overall sampling rate than a nonpipelined version.

There are many design trade-offs that can be made in the design of a pipelined ADC, such as the number of stages, the number of bits per stage, number of correction bits, and the timing. In order to ensure that the digital data from the individual stages corresponding to a particular sample arrives at the error correction logic simultaneously, the appropriate number of shift registers must be added to each of the outputs of the pipelined stages. For example, if the first stage requires seven shift-register delays, the next stage will require six, the next five, etc. This adds the digital pipeline delay to the final output data, as shown in Figure 16, the timing for a typical pipelined ADC, the AD9235.[12]

For the 12-bit, 65-MSPS AD9235, there are seven clock cycles of pipeline delay (sometimes referred to as *latency*). This latency may or may not be a problem, depending upon the application. If the ADC is within a feedback control loop, latency may be a problem—in the overlap area, the successive-approximation architecture would be a better choice. Latency also makes pipelined ADCs difficult to use in multiplexed applications. However, in the bulk of applications for which frequency response is more important than settling time, the latency issue is not a real problem.

A subtle issue relating to most CMOS-pipelined ADCs is their performance at *low* sampling rates. Because the internal timing generally is controlled by the external sampling clock, very low sampling rates extend the *hold* times for the internal track-and-holds to the point where excessive droop causes conversion errors. Therefore, most pipelined ADCs have a specification for *minimum* as well as *maximum* sampling rate. Obviously, this precludes operation in single-shot or burst-mode applications—where the SAR ADC architecture is more appropriate.

Finally, it is important to clarify the distinction between *subranging* and *pipelined* ADCs. From the discussions above, it can be seen that, although pipelined ADCs are generally subranging (with error correction, of course), subranging ADCs are not necessarily pipelined. As a matter of fact, the pipelined subranging architecture is predominant because of the demands for high sampling rates, where internal settling time is of utmost importance.

Pipelined ADCs are available today with resolutions of up to 14 bits and sampling rates over 100 MHz. They are ideal for many applications that require not only high sampling rates but high *signal-to-noise ratio* (SNR) and *spurious-free dynamic range* (SFDR). A popular application for these converters today is in software-defined radios (SDR) that are used in modern cellular telephone base stations.

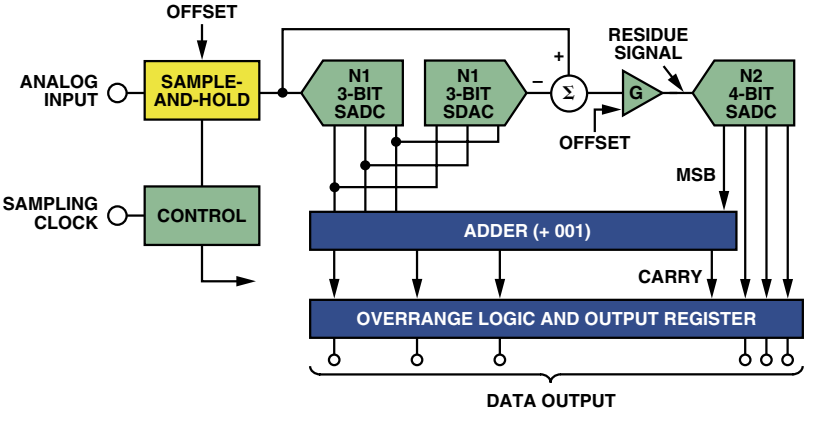

Figure 14. 6-bit subranging error-corrected ADC, N1 = 3, N2 = 4.

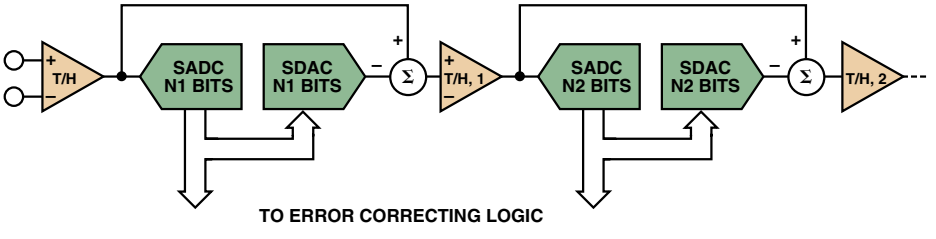

Figure 15. Generalized pipeline stages in a subranging ADC with error correction.

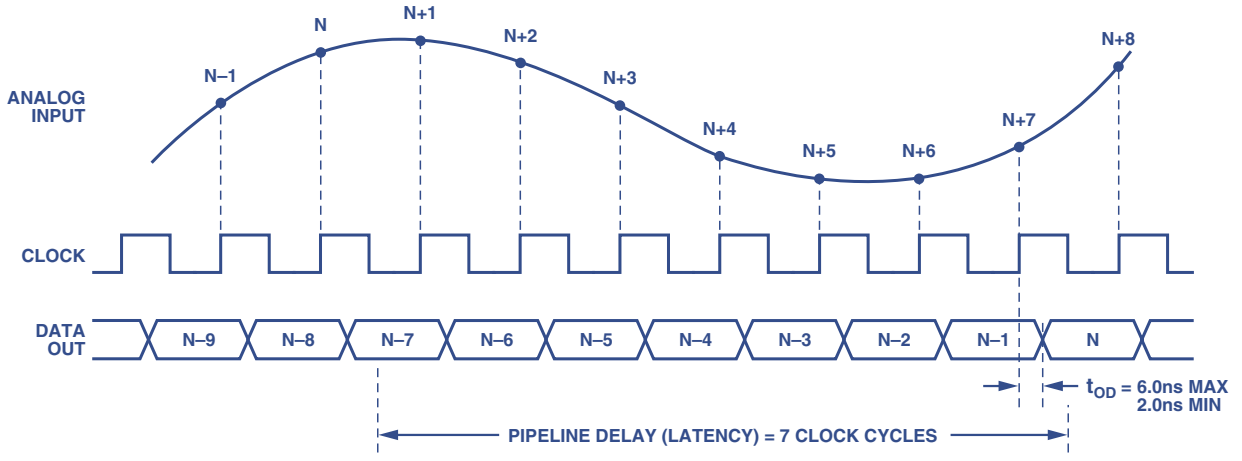

Figure 16. Timing of a typical pipelined ADC, the 12-bit, 65-MSPS AD9235.

Figure 17 shows a simplified diagram of a generic software radio receiver and transmitter. An essential feature is this: rather than digitize each channel separately in the receiver, the entire bandwidth containing many channels is digitized directly by the ADC. The total bandwidth can be as high as 20 MHz, depending on the air standard. The channel-filtering, tuning, and separation are performed digitally in the receive-signal processor (RSP) by a high-performance *digital-signal processor* (DSP).

Digitizing the frequency band at a relatively high intermediate frequency (IF) eliminates several stages of down-conversion. This leads to a lower-cost, more flexible solution in which most of the signal processing is performed digitally—rather than in the more complex analog circuitry associated with standard analog superheterodyne radio receivers. In addition, various air standards (GSM, CDMA, EDGE, etc.) can be processed by the same hardware simply by making appropriate changes in the software. Note that the transmitter in the software radio uses a transmit-signal processor (TSP) and DSP to format the individual channels for transmission via the upstream DAC.

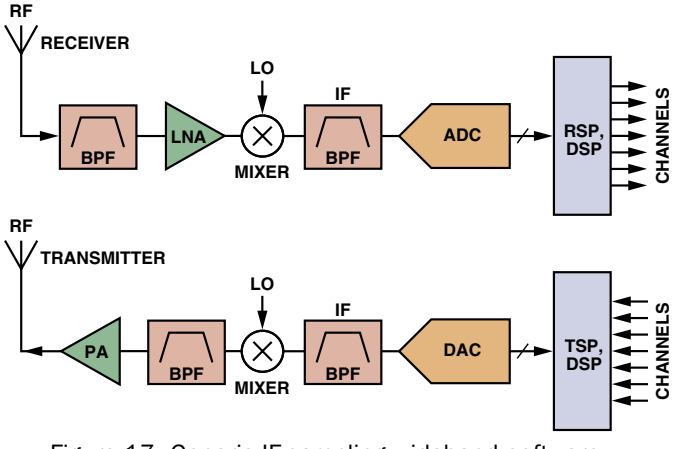

Figure 17. Generic IF-sampling wideband software radio receiver and transmitter.

The ADC requirements for the receiver are determined by the particular air standards the receiver must process. The frequencies in the bandwidth presented to the ADC consist of the desired signals as well as large-amplitude "interferers" or "blockers." The ADC must not generate *intermodulation products* due to the blockers, because these unwanted products can mask smaller desired signals. The ratio of the largest expected blocker to the smallest expected signal basically determines the required SFDR. In addition to high SFDR, the ADC must have an SNR compatible with the required receiver sensitivity.

Another requirement is that the ADC meet the SFDR and SNR specifications at the desired IF frequency. The basic concept of IF sampling is shown in Figure 18, where a 20-MHz band of signals is digitized at a rate of 60 MSPS. Note how the IF sampling process shifts the signal from the third Nyquist zone to baseband without the need for analog down-conversion. The signal bandwidth of interest is centered in the third Nyquist zone at an IF frequency of 75 MHz. The numbers chosen in this example are somewhat arbitrary, but they serve to illustrate the concept of undersampling. These applications place severe requirements on the ADC performance, especially with respect to SNR and SFDR. Modern pipelined ADCs, such as the 14-bit, 80-MSPS AD9444,[13] can meet these demanding requirements. For instance, the AD9444 has an SFDR of 97 dBc and an SNR of 73 dB with a 70-MHz IF input. The input bandwidth of the AD9444 is 650 MHz. Other 14-bit ADCs optimized for SFDR and/or SNR are the AD9445[14] and AD9446.[15]

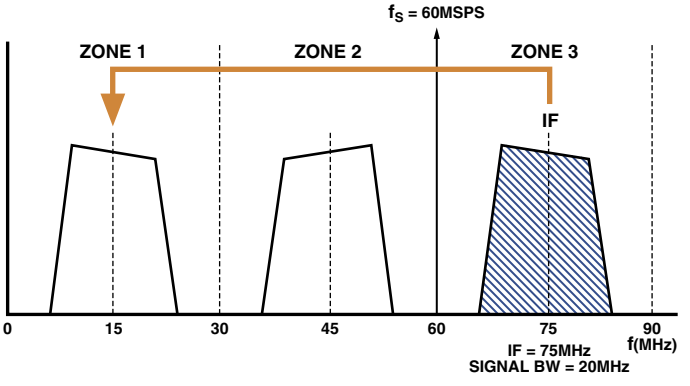

Figure 18. Sampling a 20-MHz BW signal with an IF frequency of 75 MHz at a sampling rate of 60 MSPS.

CONCLUSION

We have discussed here the successive-approximation, Σ-Δ, and pipelined architectures—those most widely used in modern integrated circuit ADCs.

Successive-approximation is the architecture of choice for nearly all multiplexed data acquisition systems, as well as many instrumentation applications. The SAR ADC is relatively easy to use, has no pipeline delay, and is available with resolutions to 18 bits and sampling rates up to 3 MSPS.

For a wide variety of industrial measurement applications, the *sigma-delta* ADC is ideal; it is available in resolutions from 12 bits to 24 bits. Sigma-delta ADCs are suitable for a wide variety of sensor-conditioning, energy-monitoring, and motor-control applications. In many cases, the high resolution and the addition of on-chip PGAs allow a direct connection between the sensor and the ADC without the need for an instrumentation amplifier or other conditioning circuitry.

The Σ-Δ ADC and DAC, easily integrated into ICs containing a high degree of digital functionality, also dominate the voiceband and audio markets. The inherent oversampling in these converters greatly relaxes the requirements on the ADC antialiasing filter and the DAC reconstruction filter.

For sampling rates greater than approximately 5 MSPS, the *pipelined architecture* dominates. These applications typically require resolutions up to 14 bits with high SFDR and SNR at sampling frequencies ranging from 5 MSPS to greater than 100 MSPS. This class of ADCs is used in many types of instrumentation, including digital oscilloscopes, spectrum analyzers, and medical imaging. Other applications are video, radar, and communications applications—including IF sampling, software radio, base stations, and set-top boxes—and consumer electronics equipment, such as digital cameras, display electronics, DVDs, enhanced definition TVs, and high-definition TVs.

The use of manufacturers' selection guides and parametric search engines, coupled with a fundamental knowledge of the three basic architectures, should help the designer select the proper ADC for the application. The use of manufacturers' evaluation boards[16] makes the process much easier. The Analog Devices ADIsimADC® program[17] allows the customer to evaluate the dynamic performance of the ADC without the need for any hardware. The required software and the ADC models (and many other analog and digital design aids) are free downloads at http://www.analog.com.[18] This tool can be extremely valuable in the selection process.

Not to be overlooked is the proper design of the ADC input-, output-, and sampling-clock circuitry. Data sheets and application notes should be consulted regarding these important issues. Finally, and equally critical to achieving a successful mixed-signal design, are layout, grounding, and decoupling. For a detailed treatment of these and other design issues, the reader is encouraged to consult the two comprehensive texts listed in Further Reading as well as the Analog Devices website, http://www.analog.com.

FURTHER READING

1. Walt Kester, Editor, *Data Conversion Handbook*, Published by Newnes, an imprint of Elsevier, 2005, ISBN: 0-7506-7841-0. See, in particular, Chapter 3, "Data Converter Architectures." In addition to detailed discussions of the various ADC and DAC architectures themselves, the chapter also includes historical aspects.
2. Walt Jung, Editor, *Op Amp Applications Handbook*, Published by Newnes, an imprint of Elsevier, 2005, ISBN: 0-7506-7844-5.
3. For more information on products or applications, please visit the Analog Devices website: http://www.analog.com.

REFERENCES—VALID AS OF JUNE 2005

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This article can be found at http://www.analog.com/library/analogdialogue/archives/39-06/architecture.html, with a link to a PDF.

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continued from page 2

his responsibilities—one which had nothing to do with the business of the company."

The path leading up to the launch of the ADXL50 accelerometer was not an easy one, recalled Ray. "It started during a 'brown bag seminar' (which Steve had organized), when a professor from Boston University spoke about his work with micromachined devices. Afterwards, Steve was inspired to think about the possibility of integrating signal-conditioning circuits with sensors to produce the world's first fully integrated accelerometers—a vision that ultimately launched ADI into micromachining and, within ten years, a market-leading position in airbag crash sensors."

> "Quite simply, Analog is the kind of a place that will roll the dice. Ours was an ideal culture for the accelerometer to take shape in. We were the right size, in that there were tons of people with technical expertise that we could draw in to get the job done," said Sherman during his acceptance speech. Turning to Stata, he acknowledged the magnitude of the financial risk, "Ray, you ... stayed with the project long past when other people would have folded. And, I appreciated how resources would magically appear."

Sherman, who works in the Micromachined Products Division in Cambridge, joined ADI in 1978 as one of the company's earliest IC designers. He has a bachelor's degree in electrical engineering from the University of Rhode Island, and a Master's degree in engineering from Case Western Reserve University in Ohio. *EDN Magazine* recently named the ADXL50 accelerometer as one of the six most important electronic innovations in the last 15 years, the only nondigital product so recognized.

ADI, which owns the largest share of the world's air-bag crash sensor market, shipped its milestone two-hundred-millionth inertial sensor in March, as a result of wide market acceptance of its *i*MEMS Motion Signal Processing™ technology. In the automotive industry, *i*MEMS technology is used in over 160 car platforms worldwide for safety-critical applications. and it is starting to gain wide use in the consumer products industry.

Future ADI Founder's Innovation Awards will be given to persons judged to have been responsible for initiating and following through on the development of outstanding, innovative, and commercially successful products.

PRODUCT INTRODUCTIONS: VOLUME 39, NUMBER 2

Data sheets for all ADI products can be found by entering the model number in the Search Box at www.analog.com

April

ADCs, Successive-Approximation, 4-channel, 12-/10-bit, 1.5-MSPS, parallel, with sequencer **AD7933/AD7934**
ADC, Successive-Approximation, 4-channel, 12-bit, 625-kSPS, with sequencer **AD7934-6**
ADC, Successive-Approximation, 2-channel, 12-bit, with I²C-compatible interface **AD7992**
ADC, Successive-Approximation, 14-bit, 250-kSPS, with pseudo-differential inputs **AD7942**
ADC, Pipelined, dual, 14-bit, 20-/40-/65-MSPS **AD9248**
Amplifier, Operational, dual, low-power, precision, JFET-input, rail-to-rail-output **AD8642**
Amplifier, Operational, low-cost, low-noise, CMOS-input, rail-to-rail-output **AD8691**
Amplifier, Operational, dual, high-speed, with rail-to-rail outputs and ultralow power-down current **ADA4850-2**
Decimating LCD Driver, 10-bit, 12-channel, with level shifters **AD8385**
Digital Potentiometers, 64-/256-position, with nonvolatile memory, I²C-compatible interface **AD5258/AD5259**
Display Interfaces, 8-/10-bit, high-performance **AD9980/AD9981**
Display Interface, dual, for flat-panel LCD **AD9882A**
Embedded Processor, Blackfin®, 750-MHz, with 3000 MMACs, 328-kbyte RAM **ADSP-BF561**
Laser-Diode Driver, 4-channel, dual-output, for DVD±R/RW drives **AD9665**
Power Supply Sequencer, with margining control, supervises up to 8 supplies **ADM1069**
Switching Converter, step-up, dc-to-dc, operates at 1.2 MHz **ADP1611**
Switch/Multiplexer, CMOS, dual 2-channel, can route USB 1.1 signals **ADG787**
Video Encoder, 11-bit, multiformat, HDTV **ADV7322**
Video Encoder, 14-bit, multiformat, noise-shaped video, supports 625p CGMS-A **ADV7324**

May

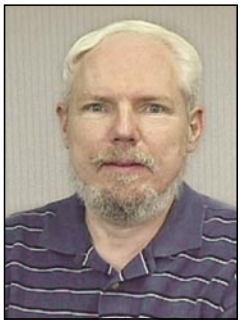
ADC, Pipelined, quad, 12-bit, 50-/65-MSPS, with LVDS outputs .. **AD9229**
Amplifier, Operational, quad, low-power, precision, JFET-input, rail-to-rail-output **AD8643**
Amplifier, Operational, low-noise, precision, CMOS-input, with rail-to-rail inputs and output **AD8655**
Amplifier, Limiting, 3.2-Gbps **ADN2891**
Clock-Distribution IC, 1.2-GHz, includes PLL **AD9510**
DAC, Voltage-Output, 32-channel, 14-bit, with bipolar outputs **AD5378**
Laser-Diode Driver, 10.7-Gbps **ADN2525**
Power Supply Sequencer, with margining control, temperature monitor, supervises up to 10 supplies **ADM1062**
Power Supply Sequencer, with temperature monitor, supervises up to 10 supplies **ADM1063**
Transmitter IC, VHF remote control **ADF7901**

June

Active Mixer, *receive*-channel, LF to 500 MHz **AD8342**
ADCs, Successive-Approximation, dual 12-bit, 1-/2-MSPS **AD7265/AD7266**
ADC, Successive-Approximation, 16-bit, 500-kSPS, with pseudo-differential input **AD7686**
ADCs, Successive-Approximation, 16-bit, 250-/500-kSPS, with true-differential inputs **AD7687/AD7688**
Amplifier, Operational, quad, low-cost, low-noise, CMOS-input, rail-to-rail-output **AD8694**
Amplifier, Operational, with high-speed, rail-to-rail output, ultralow power-down current **ADA4850-1**
Amplifier, Operational, dual, low-cost, high-speed, with rail-to-rail outputs **ADA4851-2**
Amplifier, Variable-Gain, 10-MHz to 3-GHz, with 60-dB gain-control range **ADL5330**
Amplifier, Limiting, 4.25-Gbps **ADN2892**
Audio Processor, 28-bit, multichannel, SigmaDSP™ **AD1941**
Capacitance-to-Digital Converter, 24-bit, with temperature sensor **AD7745/AD7746**
Clock Distribution ICs, 1.2-GHz **AD9511/AD9512**
Comparators, ultrafast, SiGe, single, for 3.3-V/5.2-V supply **ADCMP572/ADCMP573**
DAC, Voltage-Output, 16-bit, *nano*DAC™, with SPI interface **AD5063**
DAC, Current-Output, 10-/12-/14-bit, 1200-MSPS **AD9734/AD9735/AD9736**
IF-to-Baseband Receiver, 14-bit, 92.16-MSPS, 4-/6-channel **AD6654**
MOSFET Driver, dual, 12-V, bootstrapped, with output *disable* **ADP3118**
PLL Frequency Synthesizer, 3.5-GHz, fractional-N, low-phase-noise, fast-settling **ADF4193**
RF Detector, measures power from 50 MHz to 3.5 GHz **AD8312**
Voltage References, low-noise, low-power, in tiny TSOT-23 packages **ADR36x**

AUTHORS

Jim Hand (page 7) is a Senior Staff Design Engineer for the Analog Devices High-Speed Converter-MCP group. He has been with ADI for over 23 years and worked primarily in the area of high-speed data conversion. His recent focus has been on developing an expertise in time-interleaving ADC architectures. He earned a Bachelor of Science degree in Physics from Guilford College in 1986 and a Master of Science degree from National Technical University in 1996. He currently resides in Greensboro, NC.



Walt Kester (page 11) is a Corporate Staff Applications Engineer at Analog Devices. In his 35 years at ADI, he has designed, developed, and given applications support for high-speed ADCs, DACs, SHAs, op amps, and analog multiplexers. An author of many papers and articles, he prepared and edited eleven major applications books for ADI's global technical seminar series; topics include op amps, data conversion, power management, sensor signal conditioning, mixed-signal circuits, and practical analog design techniques. His latest book, *Data Conversion Handbook*, (Newnes) is a nearly 1,000-page comprehensive guide to data conversion. Walt has a BSEE from NC State University and an MSEE from Duke University. He enjoys carpentry and travel.

Mark Looney (page 7) is a Senior Design Engineer at Analog Devices in Greensboro, NC. Joining ADI in 1998, he has designed military-qualified dc-to-dc converters and high-speed A/D converter modules. He earned BS (1994) and MS (1995) degrees in Electrical Engineering from the University of Nevada, Reno, and has published several articles. Prior to joining ADI, he helped start IMATS, a vehicle electronics and traffic-solutions company—and designed dc-to-dc converters and EMI filters for hostile (including radiation) space-level environments at Interpoint Corporation.

Rob Reeder (page 3, 7) has been working with high-speed ADCs at ADI for over seven years in test development, module design, and—more recently—in applications engineering. He graduated in 1998 from Northern Illinois University with a Master's Degree in Electrical Engineering. In his spare time he enjoys music, art, and playing baseball with his two boys.

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